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VV6501

VGA CMOS Color Image Sensor

Features

- **640 x 480 VGA resolution**
- **1/4 inch format lens compatible**
- **On board 10 bit ADC**
- **On board voltage regulators**
- **Automatic dark calibration**
- **On board audio amplifier**
- **I^2C interface**
- **Low power suspend mode**
- **4 or 5 wire nibble output**
- **Framegrabber signals: QCK and FST**

Description

This image sensor based on STMicroelectronics CMOS technology is Bayer colorised.

The sensor provides a raw digital video output which also contains embedded codes to facilitate external synchronisation.

The sensor interfaces to a range of STMicroelectronics companion processors for applications such as USB webcams and digital stills cameras.

An I^2C interface allows an external processor to configure the device and control exposure and gain settings.

A low-power pin-driven suspend mode simplifies USB-based designs.

On board voltage regulators operate from a 5V USB supply and generate 3V3 and 1V8 power supplies for external processors.

Technical Specifications

Image Size	640 x 480 (VGA)	
Pixel size	5.6 µm x 5.6 µm	
Array size	3.6 mm x 2.7 mm	
Analogue gain	x1 to x16	
Sensitivity (typ.)	2.05 V/lux-sec	
Maximum frame rate	30 fps (with 24MHz clock)	
Supply voltage	5V (USB)	
	3V3 direct drive	
Power consumption	Active (30fps)	< 30 mA
	Suspend	< 100 µA
Operating temperature	0°C - 40°C	
Package type	36 pin CLCC	

Ordering Details

Part Number	Description
VV6501C001	36pin CLCC, colorised sensor

Table of Contents

1 Overview

1.1 Sensor overview

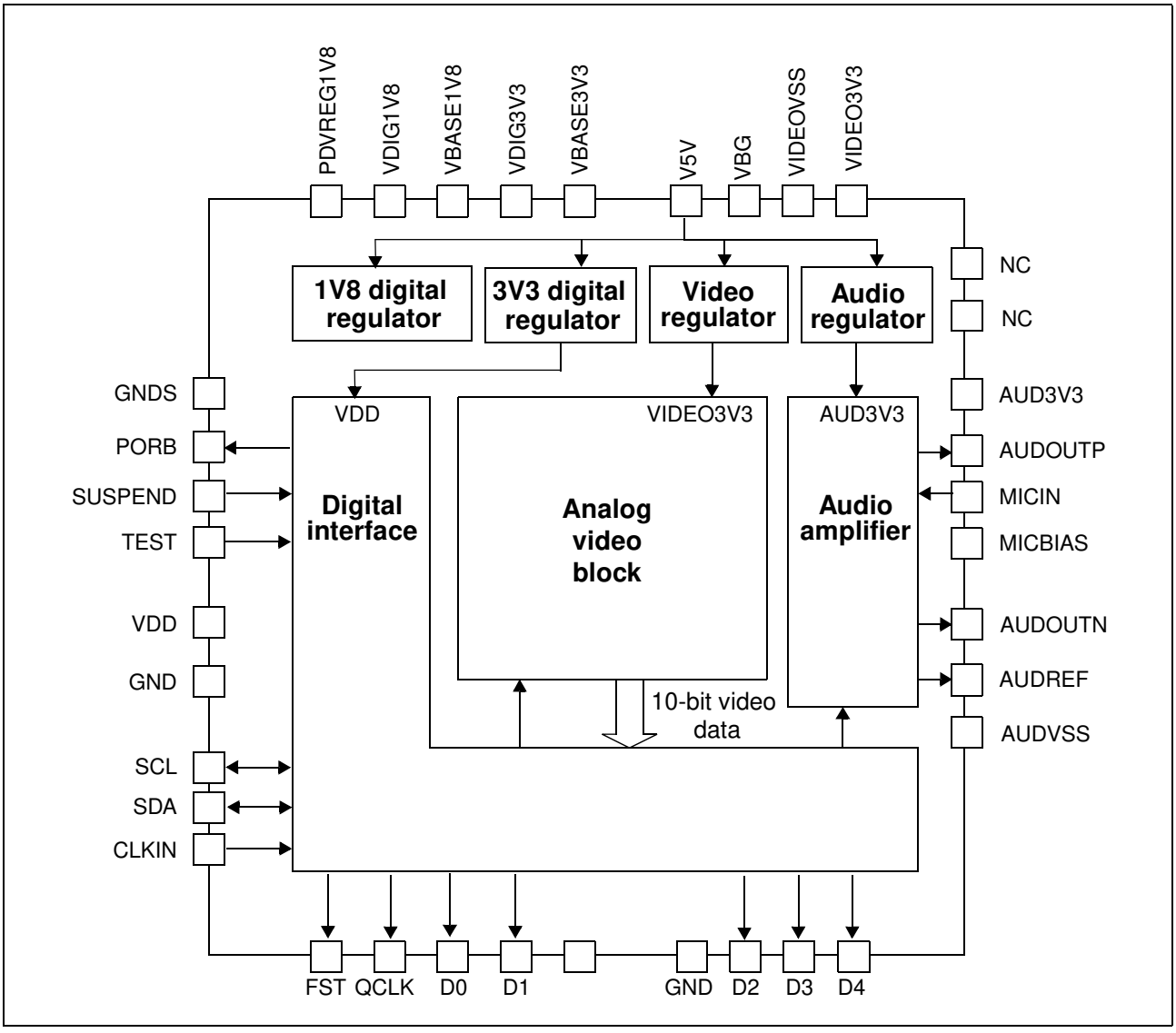
The VV6501 VGA image sensor produces raw digital video data at up to 30 frames per second. The image data is digitised using an internal 10-bit column ADC. The resulting 10-bit output data includes embedded codes for synchronization. The data is formatted as 5-bit nibbles. A separate data qualification clock (qck) and frame start (fst) signals are also provided.

The sensor is fully configurable using an I^2C interface.

The sensor also contains an audio low-noise preamplifier for use with an external microphone.

The sensor is optimized for USB applications and contains voltage regulators which drive external pass transistors to produce 3V3 and 1V8 supplies. These supplies may be used by external processors. A dedicated SUSPEND input pin may be used to force the device into a low power state while maintaining the device configuration. A power-on reset signal (PORB) may be used to reset external devices.

Figure 1: VV6501 block diagram



1.2 Typical application

1.2.1 USB webcam

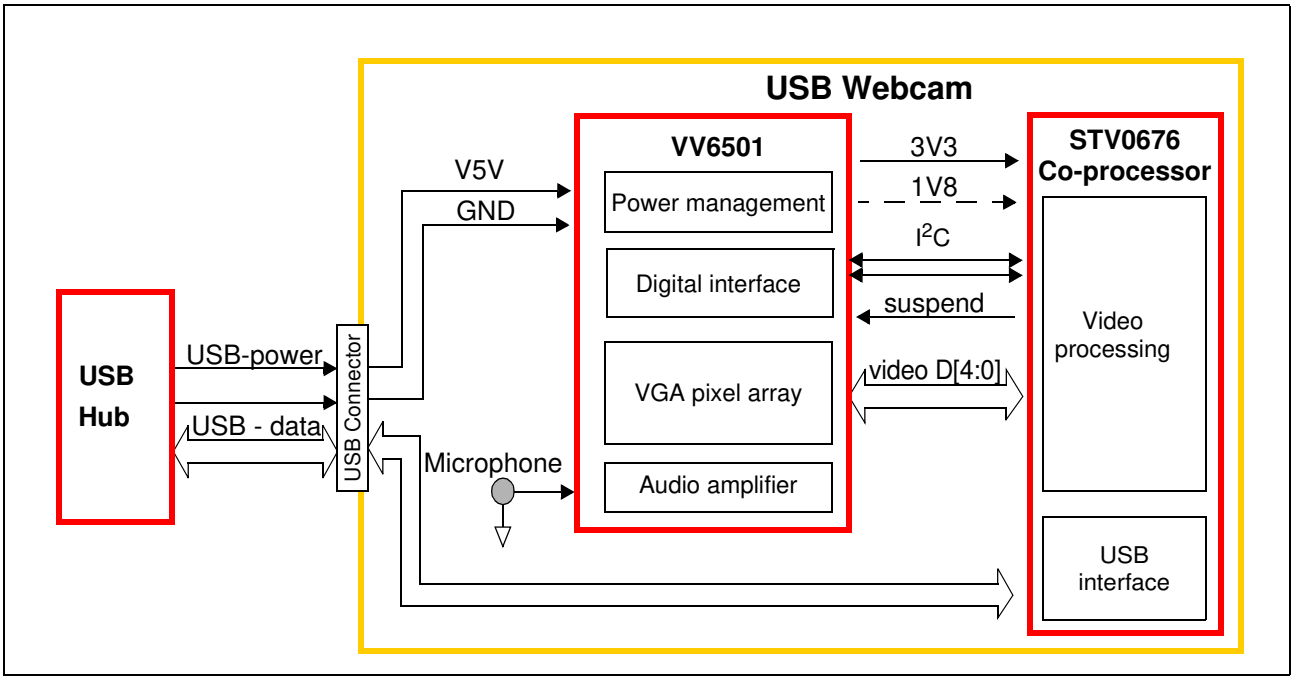
This sensor may be used in conjunction with the STMicroelectronics STV0676 co-processor to produce a low cost USB webcam.

In this application the co-processor supplies the sensor clock and uses the embedded control sequences to synchronise with the frame and line level timings. It then performs the colour processing on the raw image data from the sensor before supplying the final image data to the host using the USB interface.

The voltage regulators on-board the sensor are used to control external bipolar transistors to derive the supplies for the sensor and co-processor from the 5V USB supply. This approach eliminates the requirement for more costly external voltage regulation circuitry.

Figure 2 below illustrates a typical system using VV6501.

Figure 2: USB camera system using STV0676

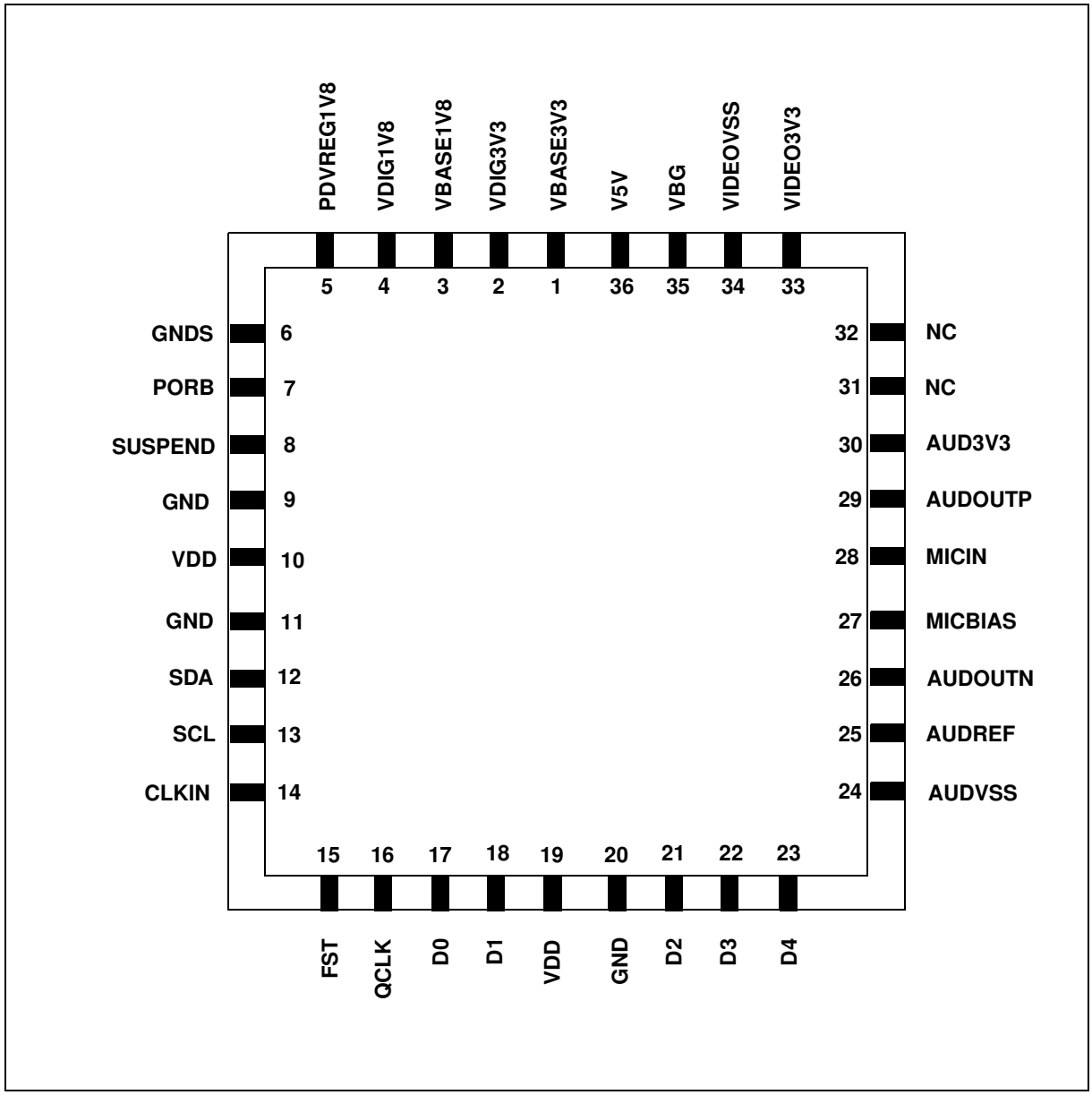


The input USB supply is 5 V. The 3V3 digital regulator generates the supply for the sensor digital part and the co-processor IOs. The 1V8 regulator generates the core supply for the co-processor.

2 Device Pinout

2.1 Pin position

Figure 3: Pin position



2.2 Pin description

Table 1: Pin description

Pin Number	Pin Name	Pin Type	Description
Digital regulators			
1	VBASE3V3	PWR	3.3 V digital regulator (connect to external PNP base)
2	VDIG3V3	PWR	3.3 V digital regulator (connect to external PNP collector)
3	VBASE1V8	PWR	1.8 V digital regulator (connect to external PNP base)
4	VDIG1V8	PWR	1.8 V digital regulator (connect to external PNP collector)
Digital inputs/outputs			
5	PDVREG1V8	PWR	1.8 V reg power down signal 1 - Regulator powered down 0 - Regulator powered up
6	GNDS	PWR	Connect to GND
7	PORB	O	Power on reset signal (active low)
8	SUSPEND	I	Sensor suspend input signal (active high) with Schmitt buffer
9	TEST	I	Input pin with Schmitt buffer. Connect to GND
10	VDD	PWR	Digital IO supply 3.3 V
11	GND	PWR	Digital ground
12	SDA	IO	Bidirectional I^2C pin
13	SCL	IO	Bidirectional I^2C pin. I^2C clock line
14	CLKIN	I	Input clock pin with Schmitt buffer
15	FST	O	FST signal (active high). 2 mA output pad
16	QCLK	O	Sensor data qualifying clock. 4 mA output pad
17	D0	O	D0 signal (data bus, bit 0). 4 mA output pad
18	D1	O	D1 signal (data bus, bit 1). 4 mA output pad
19	VDD	PWR	Digital IO supply 3.3V
20	GND	PWR	Digital IO/core source ground
21	D2	O	D2 signal (data bus, bit 2). 4 mA output pad
22	D3	O	D3 signal (data bus, bit 3). 4 mA output pad
23	D4	O	D4 signal (data bus, bit 4). 4 mA output pad

Table 1: Pin description

Pin Number	Pin Name	Pin Type	Description
Audio amplifier			
24	AUDVSS	PWR	Audio ground
25	AUDREF	PWR	Audio reference voltage (requires external decoupling capacitor)
26	AUDOUTN	O	Audio negative output
27	MICBIAS	PWR	Audio microphone bias voltage
28	MICIN	I	Audio microphone input signal
29	AUDOUTP	O	Audio positive output
30	AUD3V3	PWR	3.3 V audio analogue supply (requires external decoupling capacitor)
Video regulator			
33	VIDEO3V3	PWR	Analogue video 3.3 V
34	VIDEOVSS	PWR	Analogue video ground
35	VBG	PWR	5 V BandGap voltage (requires external decoupling capacitor)
36	V5V	PWR	USB power supply (4 - 5.5 V)
Not connected			
31,32	-	-	Not connected

3 Functional Description

The first three sections of this chapter detail the main blocks in the device:

- Video
- Audio
- Power management

The final section describes the device level operating modes including suspend.

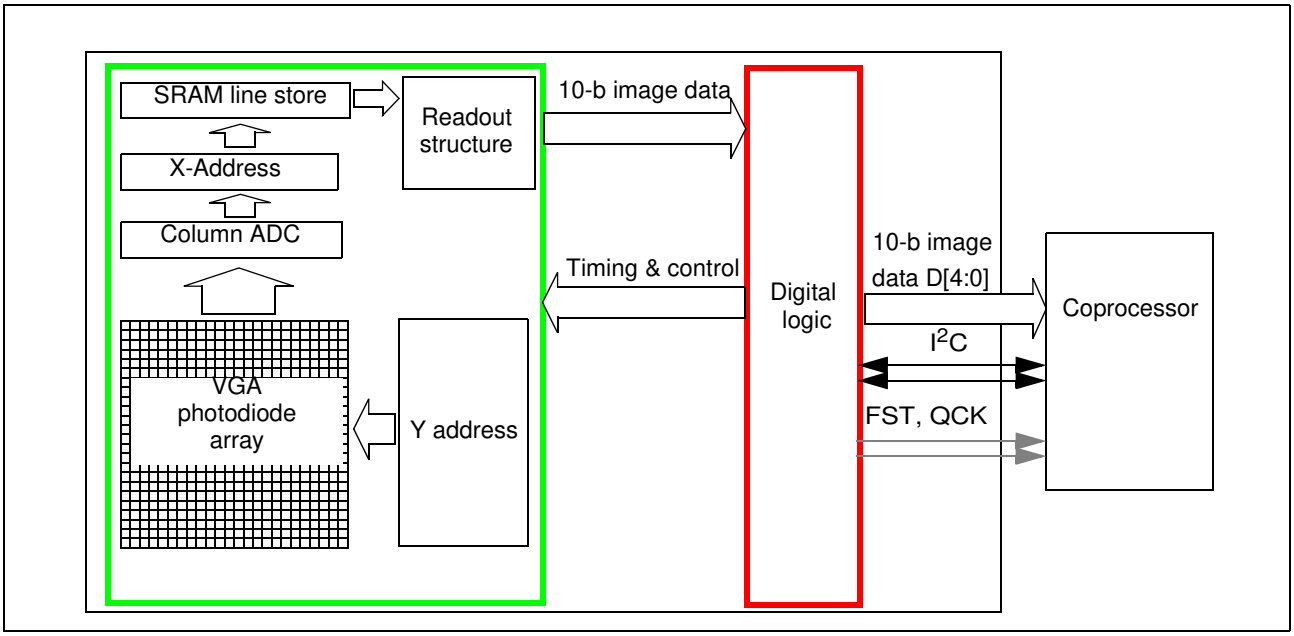
3.1 Video block

3.1.1 Overview

The analog core of the video block contains a VGA sized pixel array. The integration time and access for a row of pixels is controlled by the Y-address block. The row of pixels being read is converted using a 10-bit in-column ADC. The digitised data is readout into the digital block for formatting. The 10-b data is transferred to the co-processor over a 5-wire digital bus as two 5-b nibbles.

The exposure or integration time for the pixel array is calculated by the external co-processor and delivered to the sensor using the I2C interface.

Figure 4: Overview of video block

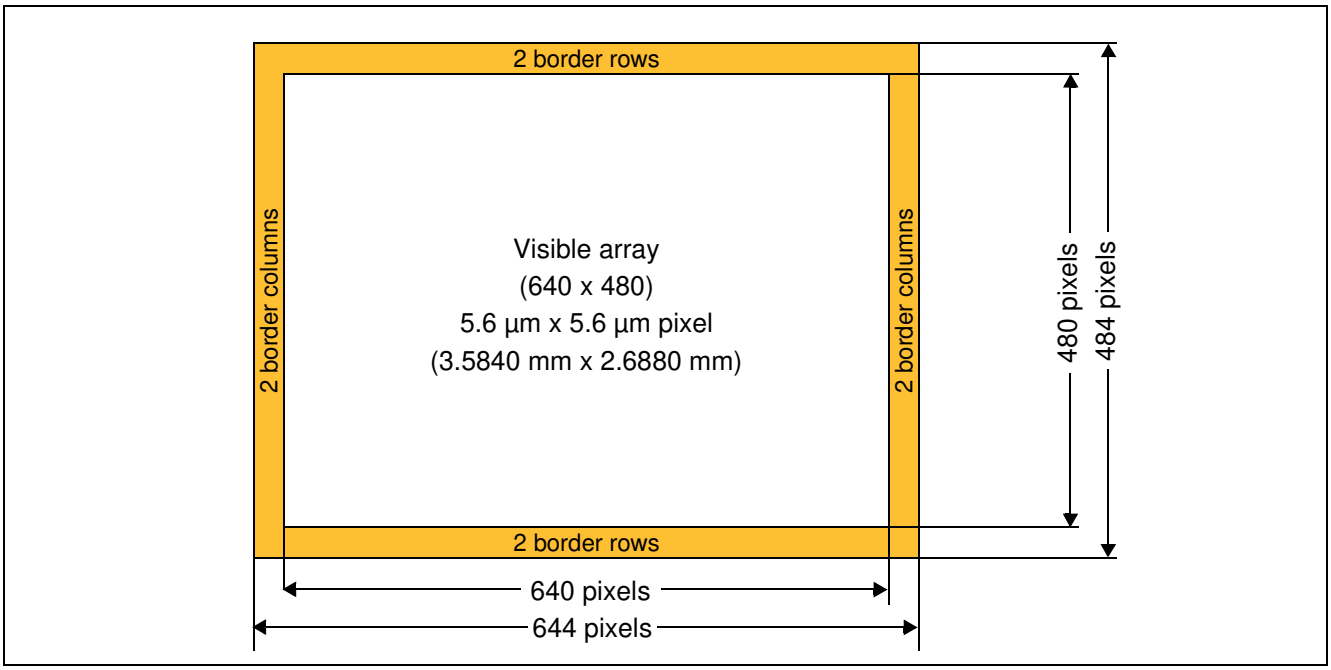


Data synchronization can be achieved either by using the embedded codes within the data stream or by making use of the dedicated FST and QCK pins.

3.1.2 Imaging array

The physical pixel array is 656 x 496 pixels. The pixel size is 5.6 µm by 5.6 µm.

Figure 5: Pixel array



The additional border columns and rows are included to enable complete color reconstruction of the final 640 by 480 sized array.

Microlens

Microlenses placed above the visible pixels improve light gathering capability hence improving sensitivity.

3.1.3 Sensor data overview

Sensor data is output on a 5-wire bus. As well as pixel data there are embedded codes at the start and end of every video line. These codes are always preceded by an escape sequence which is guaranteed not to appear in the video data itself.

Table 2: Video data values

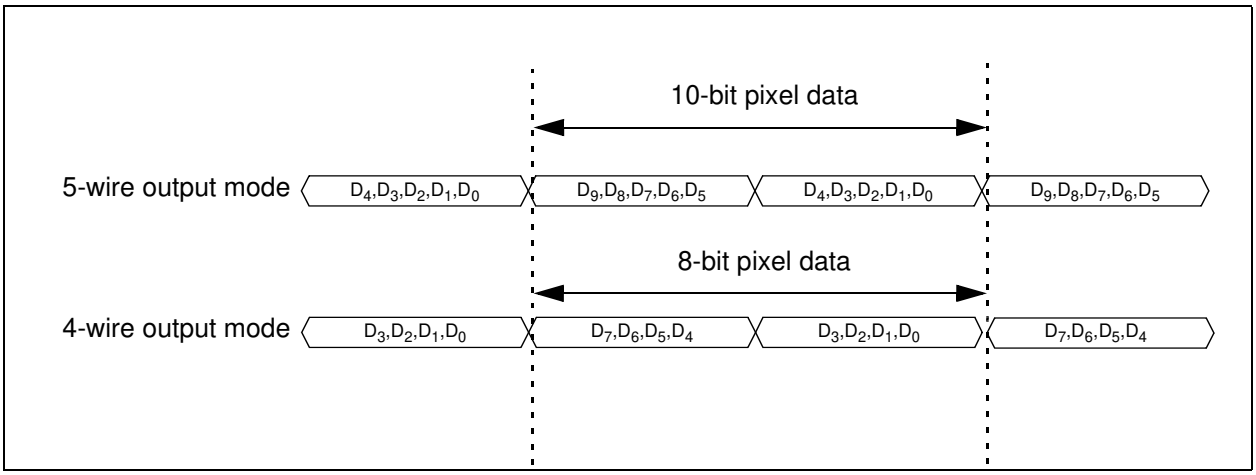
Read-out order	Progressive scan (non-interlaced)	
Form of encoding	Uniformly quantized, PCM, 8/10 bits per sample	
	8 bit mode	**10 bit mode**
Video pixel range	1 to 254	1 to 1022
Black level value	16	64
Escape sequence	FF, FF, 00	3FC, 3FC, 00

3.1.4 Digital data bus: D[4:0]

Sensor data may be either 8 or 10 bits per pixel and is transmitted as follows:

- **10-bit data:** A pair of 5-bit nibbles, most significant nibble first, on 5 wires.
- **8-bit data:** A pair of 4-bit nibbles, most significant nibble first, on 4 wires.

Figure 6: Digital data output modes



In 5-wire mode, the embedded control codes occupy only the most significant 8-bits, the least significant 2-bits are always zero.

Output tri-state using SIF

Register 23 bit[5] can be used to tri-state all 5 data lines, QCK and FST.

Output pad drive strength

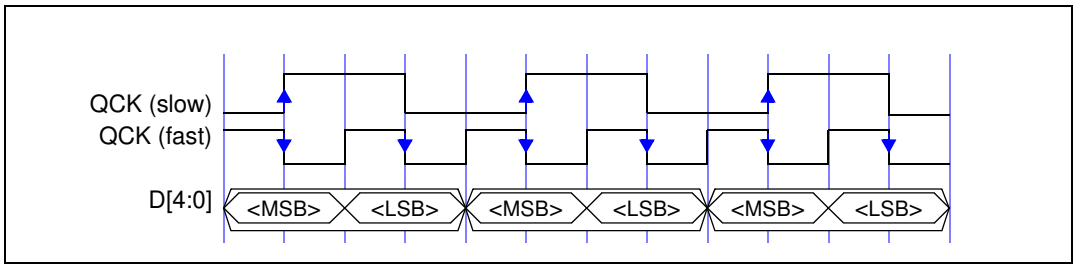
The data and QCK output pads are tri-stateable with 4 mA drive.

3.1.5 Data qualification clock (QCK)

A data qualification clock (QCK) is available and complements the embedded control sequences. This clock runs continuously when enabled and consists of:

- **Fast QCK**: the falling edge of the clock qualifies every 5 or 4-bit data blocks that constitute a pixel value.
- **Slow QCK**: the rising edge qualifies 1st, 3rd, 5th, etc. blocks of data that constitute a pixel value while the falling edge qualifies the 2nd, 4th, 6th etc. blocks of data. For example in 4-wire mode, the rising edge of the clock qualifies the most significant nibbles while the falling edge of the clock qualifies the least significant nibbles.

Figure 7: QCK modes

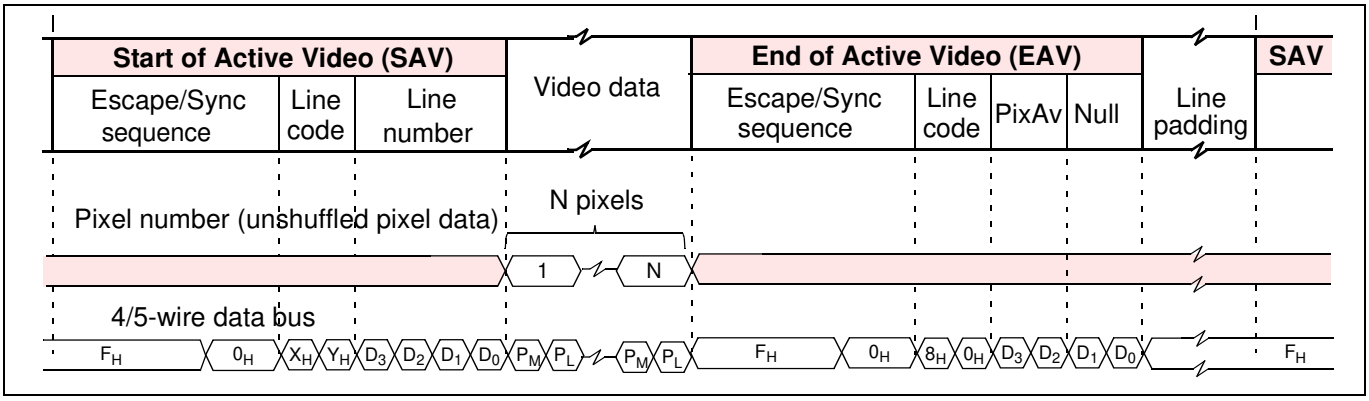


3.1.6 Line formats

Each line of data from the sensor starts with an escape sequence followed by a line code that identifies the line type. The line code is then followed by two bytes that contain a coded line number.

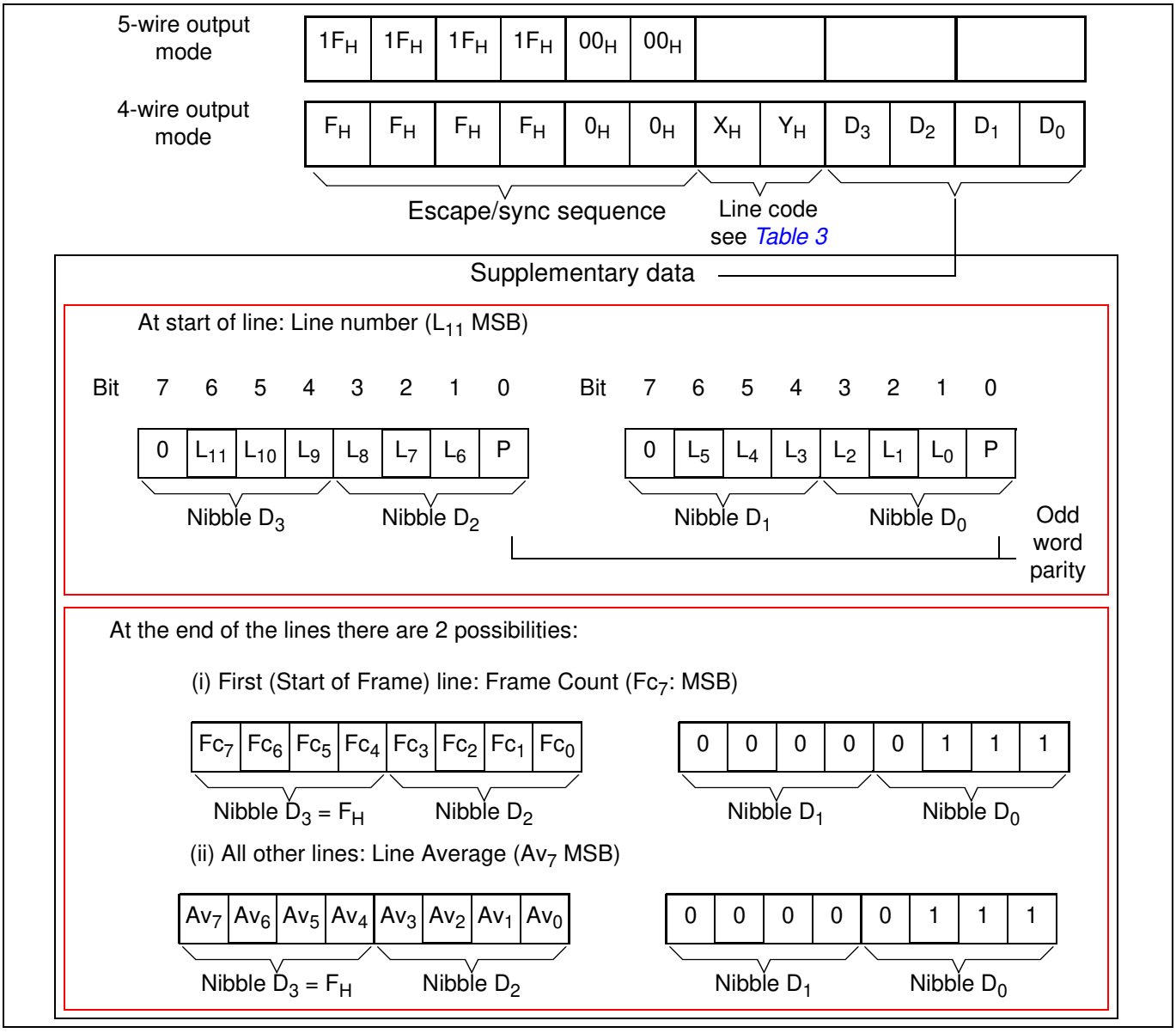
Each line is terminated with an end-of-line code followed by a line average. The one exception to this is the first line in the frame where the end of line code is followed by a frame count.

Figure 8: Line data format



The line code formats are detailed in *Figure 9*.

Figure 9: Line code format



The line code absolute value depends on whether 5-wire or 4-wire output mode has been selected, as shown in *Table 3*.

Table 3: Line codes

Line code	5-b Nibbles	4-b Nibbles
Line codes at beginning of line		
Start of Frame	$31C_H$ (796_{10})	$C7_H$ (199_{10})
Blank Line (BL)	274_H (628_{10})	$9D_H$ (157_{10})
Black or Dark line (BK)	$2AC_H$ (684_{10})	AB_H (171_{10})
Visible Line (VL)	$2D8_H$ (728_{10})	$B6_H$ (182_{10})
Last line in Frame	368_H (872_{10})	DA_H (218_{10})
Line Code at end of line		
End of Line	200_H (512_{10})	80_H (128_{10})

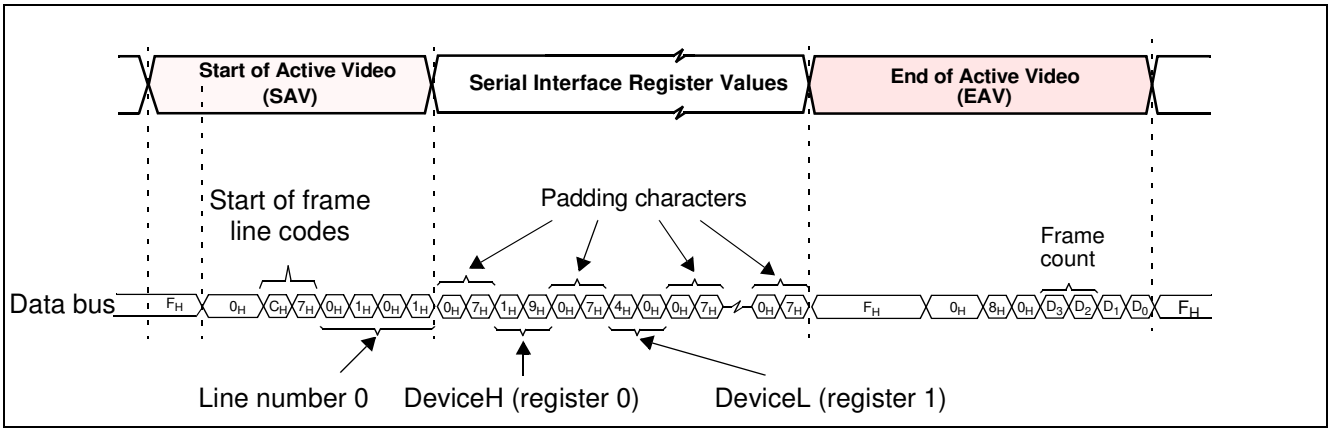
Start of frame line format

The start of frame line contains the contents of the first 16 serial interface registers rather than any video data. This information immediately follows the line code at the beginning of the line. The code 07_H is output after each serial interface value.

It takes 32 pixel clock periods to output these 16 serial interface register values. The remaining pixel periods of the video portion of the line are padded out using 07_H values. The first two pixel locations are also padded with 07_H characters (*Figure 10*). If a serial interface register location is unused then the value from register 0 is output.

Following the escape sequence and line code at the end of active video, a frame count is output.

Figure 10: Start of frame line format



Active video line format

All video data is contained on active video lines. The pixel data appears as a continuous stream of bytes within the active lines.

Black line format

The black lines contain information from the sensor black lines (held in zero exposure). This information may be used by certain co-processors.

Dark line format

The dark lines contain information from the sensor dark lines (shielded from light by metal). The information from these lines is used by the sensor to calculate a dark average offset value which is then applied to the video data to ensure a known ‘black’ level for image data.

Blank line format

To reduce the frame rate it is possible to extend the frame length by adding blank data lines. These contain no video or black line data. In default VGA mode there are no blank lines.

End of frame line format

The end of frame line sole purpose is to indicate the end of a frame, it contains no video data.

Line Duration

Table 4 shows the image duration and interline intervals with default setup.

Table 4: Line timing

Sensor Clock	Pixel Clock	Image		Interline		Line Total	
		QCKs	µs	QCKs	µs	QCKs	µs
24MHz	12MHz	644	53.6	118	9.8	762	63.5

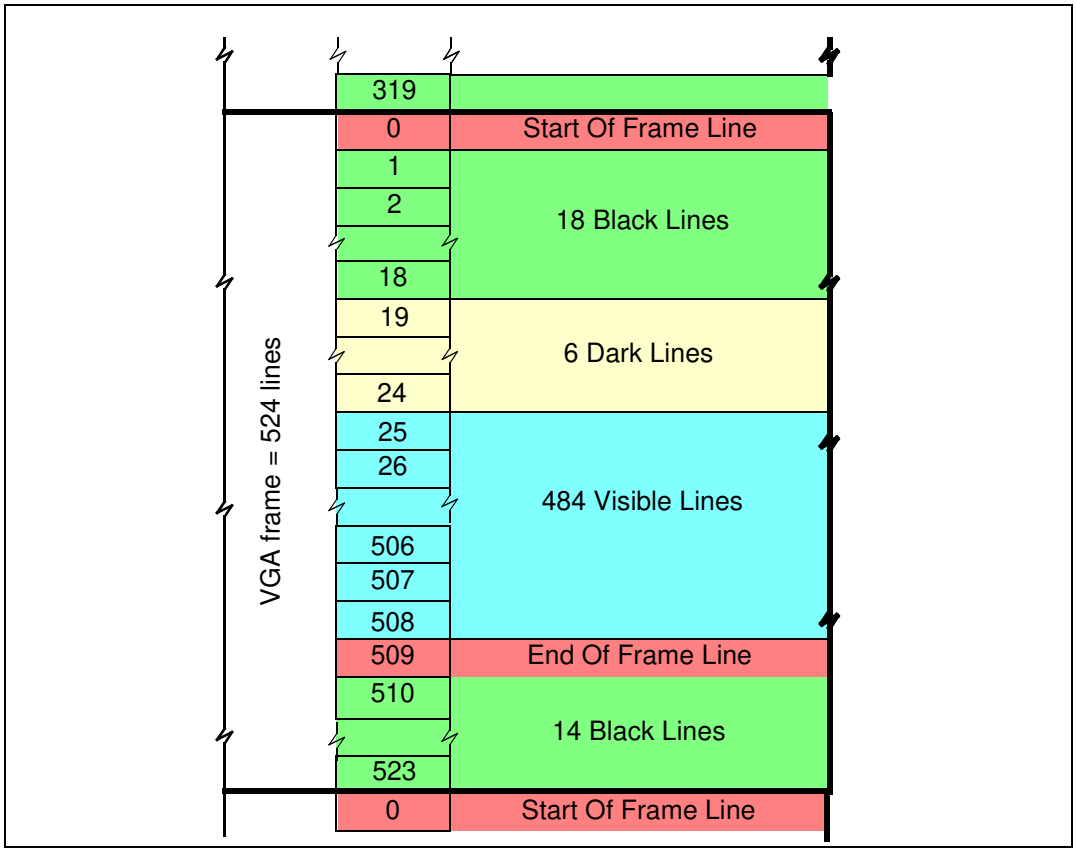
Extending line lengths

The user can extend the line length by writing to serial registers 82 and 83. The line length padding is inserted after the EAV sequence, ensuring that the distance between the SAV and EAV sequences remains constant.

3.1.7 Frame format

Each video frame is composed of a sequence of data lines as illustrated in *Figure 11*.

Figure 11: VGA frame format



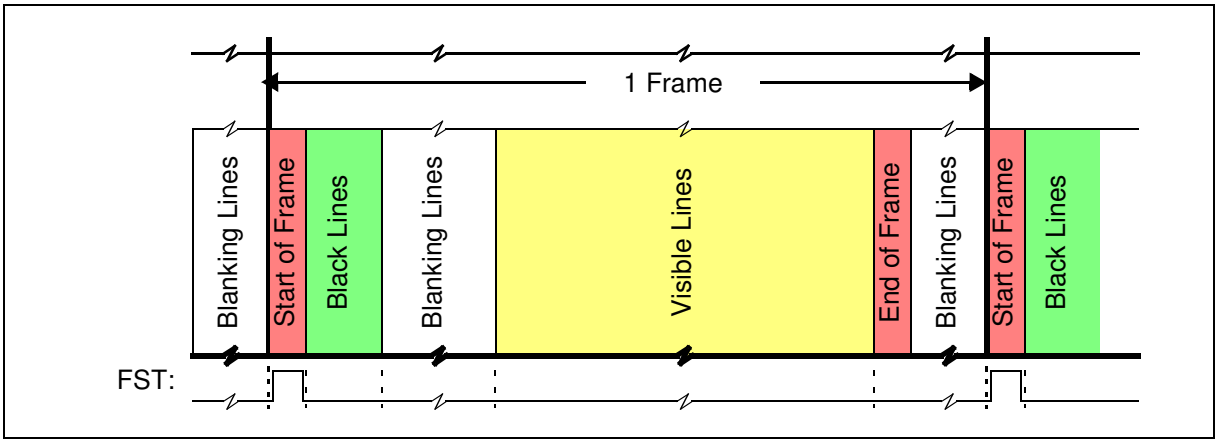
Extending the inter-frame period

The user may choose to extend the inter-frame period by increasing the frame length by writing to serial registers 97 and 98. In this event, the appropriate number of additional blank lines is inserted between the End Of Frame (EOF) line and the Start Of Frame (SOF) line. This means that the distance between SOF and EOF remains constant.

Timing of Frame Start signal (FST)

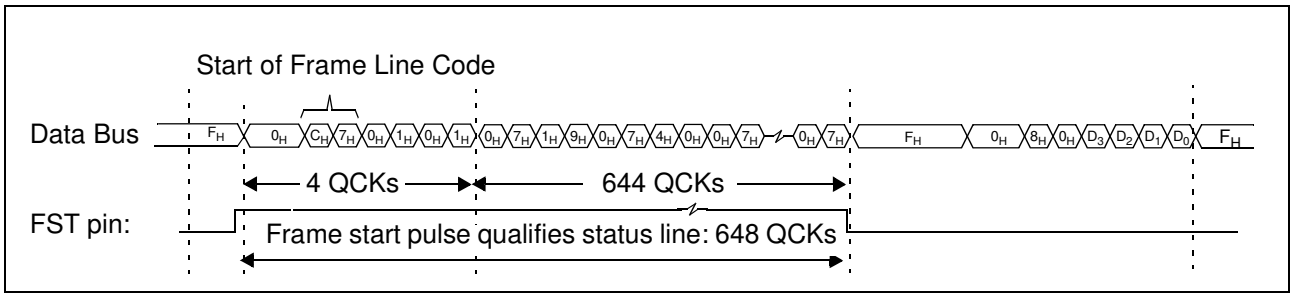
The frame-level position of FST is illustrated in *Figure 12*.

Figure 12: FST timing overview



The FST pulse qualifies the Status Line information and is 648 QCKs (slow) long.

Figure 13: Detailed FST timing

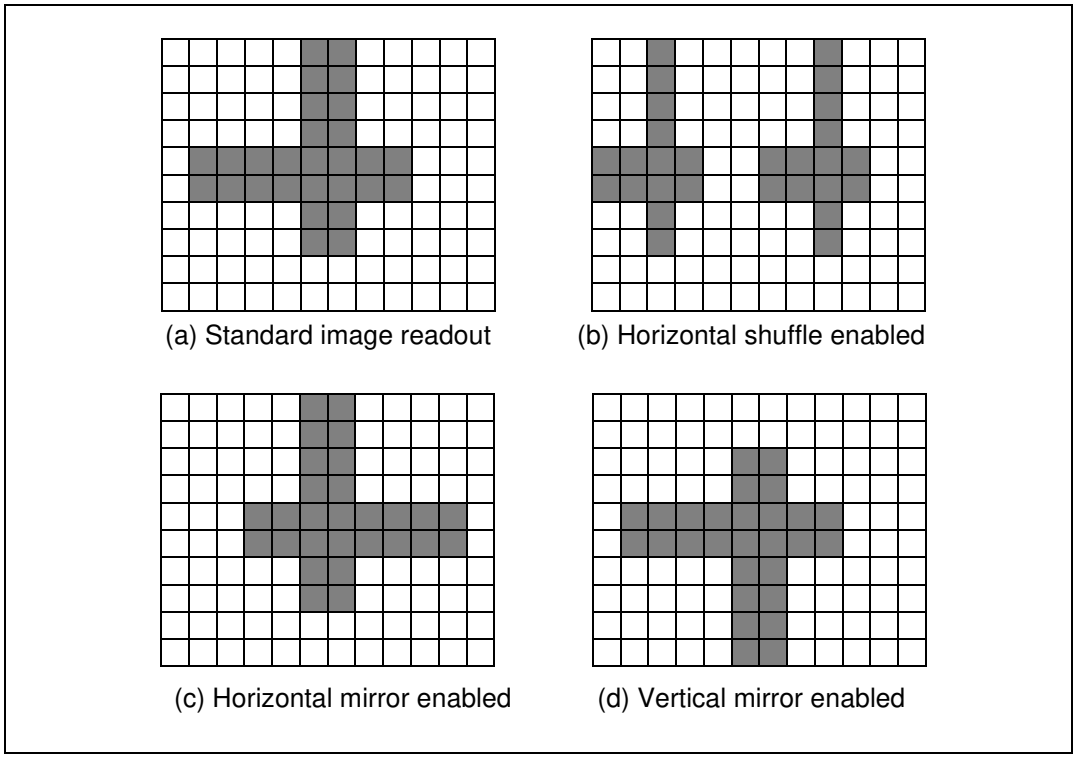


3.1.8 Image translations

The imaging array can be readout with different modes as described here below:

- Shuffle horizontal readout, bit [7] of serial register [17]. Even columns (2,4,6.) are readout first.
- Mirror horizontal readout, bit [3] of serial register [22]. Columns are readout in reverse order.
- Mirror vertical readout, enabled by setting [4] of serial register [22]. Rows are readout in reverse order.

Figure 14: Image readout modes



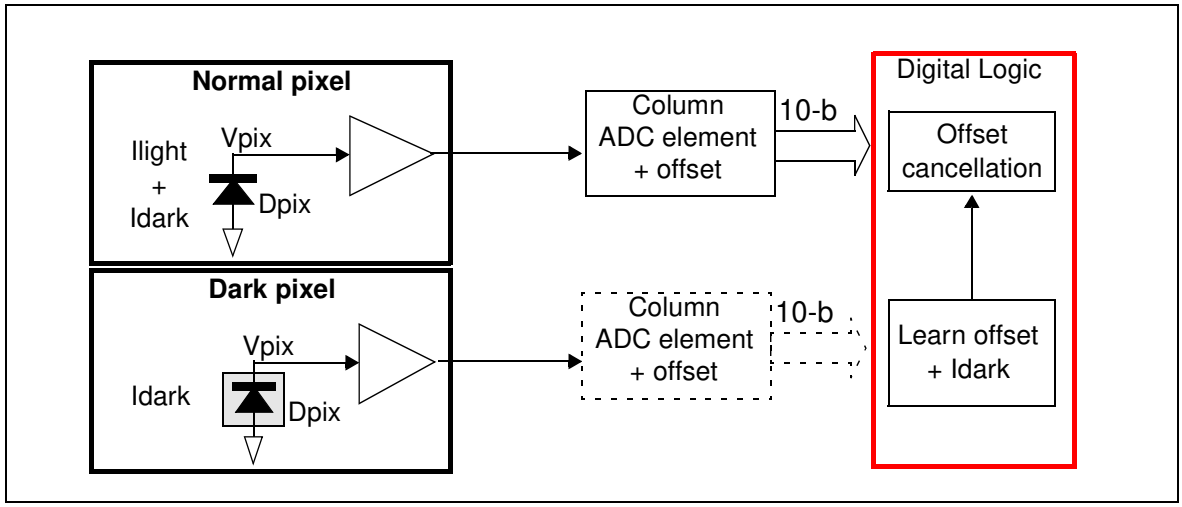
3.1.9 Dark calibration

In order to produce a high quality output image from the VV6501, it is necessary to accurately control the black level of the video signal. There are two main sources of error:

- Dark current
- Offsets in the output path.

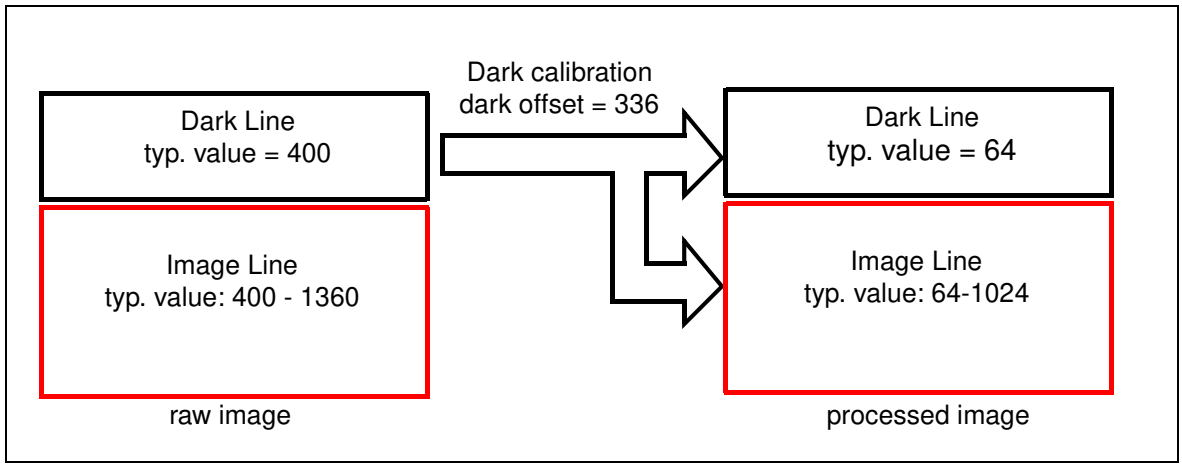
The black level is corrected by using dark pixel rows to “learn” the offset so that it can then be subtracted from the image data. Dark rows have the same exposure setting as the visible lines but are shielded from incident light.

Figure 15: Overview of dark offset cancellation



For 10-b data the ideal “black” code is set to be 64 (when viewing 8-b data the ‘black’ code should be 16). The aim of the dark calibration algorithm is to “learn” the offset required such that “black” image lines have code 64.

Figure 16: Role of dark offset calibration



Dark calibration algorithm

The dark line monitoring logic accumulates a number of dark pixels, calculates an average and then compares this average with the appropriate black level. There is a bit in serial register 45 which determines whether the offset applied is the user-programmable value from serial register 44, or the value calculated by the offset cancellation processor.

The dark offset cancellation algorithm accumulates data from the dark lines which is input to a leaky integrator and an appropriate offset is calculated.

Following an exposure/gain change, on power up or when going out of suspend mode, the history in the dark calibration leaky integrator is reset to the incoming value as the previously stored value will be out of date.

User control

The serial interface allows the user the following additional controls:

- Accumulate dark pixels, calculate dark pixel average and report, but do not apply anything to data stream
- Accumulate dark pixels, calculate dark pixel average, report and apply internally calculated offset to data stream
- Accumulate dark pixels, calculate dark pixel average and report, but apply a SIF supplied offset

3.1.10 Sensor clock and frame rate control

The frame rate is determined by both the input sensor clock and some additional registers under user control.

Sensor clock

The sensor requires a single-ended clock input. A 24MHz clock is required to generate 30 frames per second VGA images. The results is a pixel rate of 12MHz.

Slower frame rates

In order to achieve slower frame-rates the user has a number of options:

- increase the inter-frame time by adding blank line (via SIF register)
- apply a slower external clock
- divide down the external clock using the sensor internal clock divider (via SIF register)

Clock divider

The sensor contains a 4-bit register with which the user selects the clock divider setting (N). *Table 5* gives the mapping between the clk_div value and the divider ratio.

Table 5: User programmable clock divider values

clk_div[3:0]	divide by
0000 [default]	1
0001	2
001X	4
010X	6
011X	8
100X	10

Table 5: User programmable clock divider values

clk_div[3:0]	divide by
101X	12
110X	14
111X	16

3.1.11 Exposure/gain control

The sensor does not contain any form of automatic exposure or gain control. To produce a correctly exposed image, exposure and gain values must be calculated externally and written to the sensor via the serial interface.

Exposure calculation

The exposure time for a pixel and the ADC range (therefore the gain) are programmable via the serial interface. The explanation below assumes that the gain and exposure values are updated together as part of a 5 byte serial interface auto-increment sequence.

Exposure time combines coarse, fine exposure, pixel rate also related to frame and line lengths, all defined in *Table 6*.

Table 6: Definitions related to exposure

Frame length	Number of lines per frame [default=524] The frame length may be increased to 1023 by writing to the frame length register.
Line length	Number of pixels in a line [default = 762] The line length may be increased to 1023 by writing to the line length register.
Exposure	The pixel exposure time is determined by the course and fine exposure values
Coarse exposure value	The number of lines a pixel exposes for. Limited by frame length. Coarse exposure value is in the range [0 - (frame length -2)].
Fine exposure value	Number of additional pixel periods a pixel exposes for. Limited by line length. Fine exposure value is in the range [11 - (line length)].
Pixel period	Determined by the input clock frequency (Fclkin) and user clk_div setting. PixPeriod=(2*N)/Fclkin where N = clock divider ratio
Exposure time	PixPeriod x [($Coarse_{num\_lines}$ x $Line\_Length_{num\_pixels}$) + $Fine_{pixels}$]

Example of exposure calculation in default VGA video mode

coarse exposure = 522

fine exposure = 762

Input clock frequency - Fclkin = 24MHz,

Pixel period = $2/(24 \times 10^6) = 8.33 \times 10^{-8}$ s

Calculation: exposure time = $8.33 \times 10^{-8} \times [(522 \times 762) + 762] = 33.2$ ms

The available range of exposure (without using clock division) is shown in *Table 7*.

Table 7: Exposure ranges [24MHz system clock]

Range	Coarse (no. lines)	Line length (no. pixels)	Fine (no. pixels)	Exposure	
				No. pixels	Time
Min.	0	762	11	0	0.92 µs
Max (default-VGA)	522	762	762	400,050	33.2 ms
Max (available)	1023	1023	1023	$1023^2 + 1023$	87.3 ms

3.1.12 Gain timing and exposure updates

Exposure and gain values are re-timed within the sensor to ensure that a new set of values is only applied to the sensor array at the start of each frame. Bit 0 of the status register is set high when a new exposure value is written via the serial interface but has not yet been applied to the sensor array.

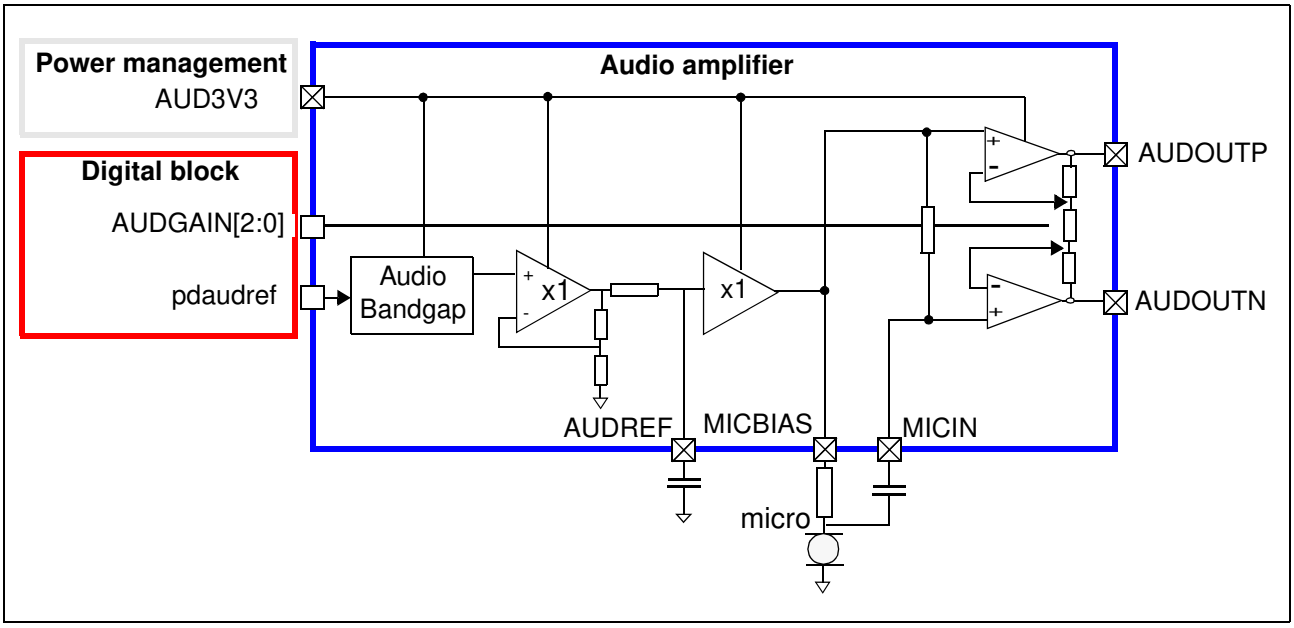
There is a 1 frame latency between a new exposure value being applied to the sensor array and the results of the new exposure value being read-out. The same latency does not exist for the gain value. To ensure that the new exposure and gain values are aligned up correctly the sensor delays the application of the new gain value by one frame relative to the application of the new exposure value.

To eliminate the possibility of the sensor array seeing only part of the new exposure and gain settings, if the serial interface communication extends over a frame boundary, the internal re-timing of exposure and gain data is disabled while writing data to any location in the exposure page of the serial interface register map. Thus, if the 5 bytes of exposure and gain data is sent as an auto-increment sequence, it is not possible for the sensor to consume only part of the new exposure and gain data.

3.2 Audio block

The audio amplifier is designed to drive an external ADC, possibly in the co-processor, with an amplified audio signal taken from a FET microphone input. The 3-bit gain control and power down for the reference are controlled via the I^2C interface.

Figure 17: VV6501 audio amplifier overview



3.2.1 Co-processor support for audio

Table 8 below summarizes the audio capability of the different co-processors the VV6501 is intended to work with.

Table 8: Co-processor support for audio

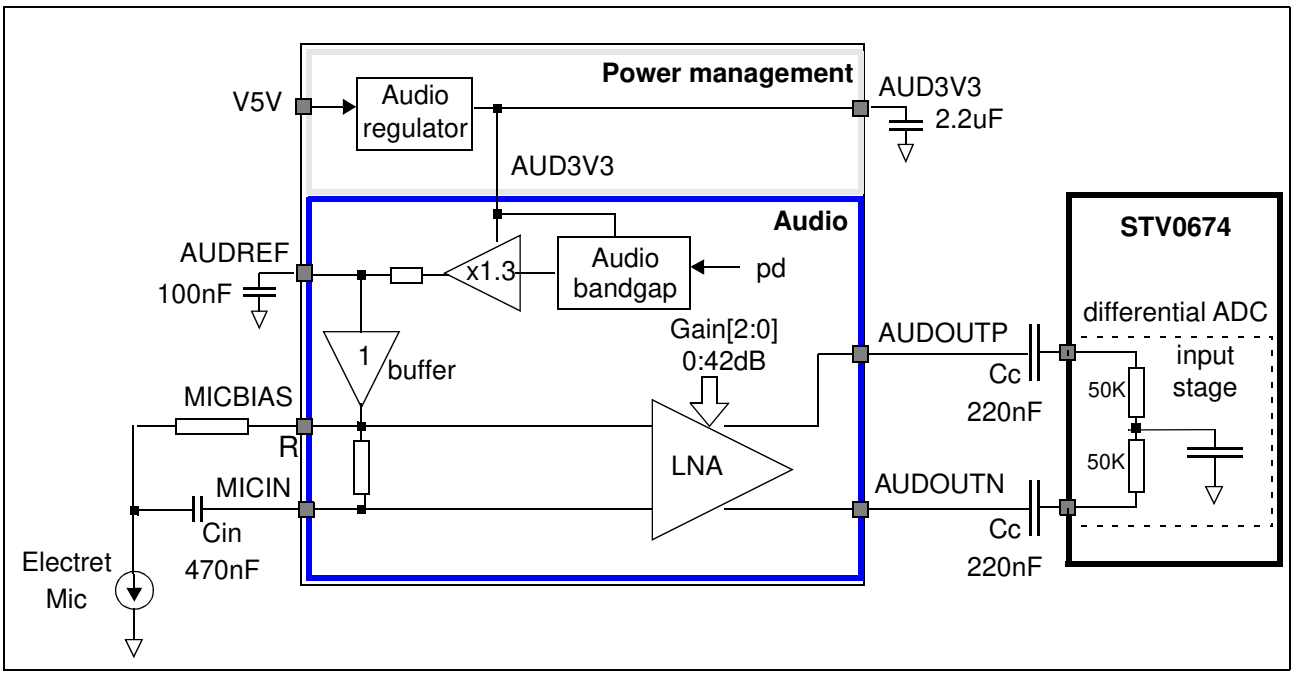
Co-processor	Audio support	Comment
STV0676	Audio 8-b digital endpoint	External ADC needed
STV0674	16 bit Sigma-Delta	501 audio output is directly AC coupled to STV0674 differential audio inputs. STV0674 includes digital ALC and noise gate
STV0680/1	Successive approximation ADC	Low quality audio recording support

3.2.2 Audio amplifier key features

- Very high PSRR micro bias reference due to bandgap from the 3.3V regulated supply, as well as RC network for LF filtering in the audio bandwidth.
- Fully differential low-noise amplifier with gain control via serial IF (0dB to +42dB in 6dB steps).

Up to 1.8Vpp dynamic range on AUDOUTP and AUDOUTN

Figure 18: VV6501 audio amplifier in typical application



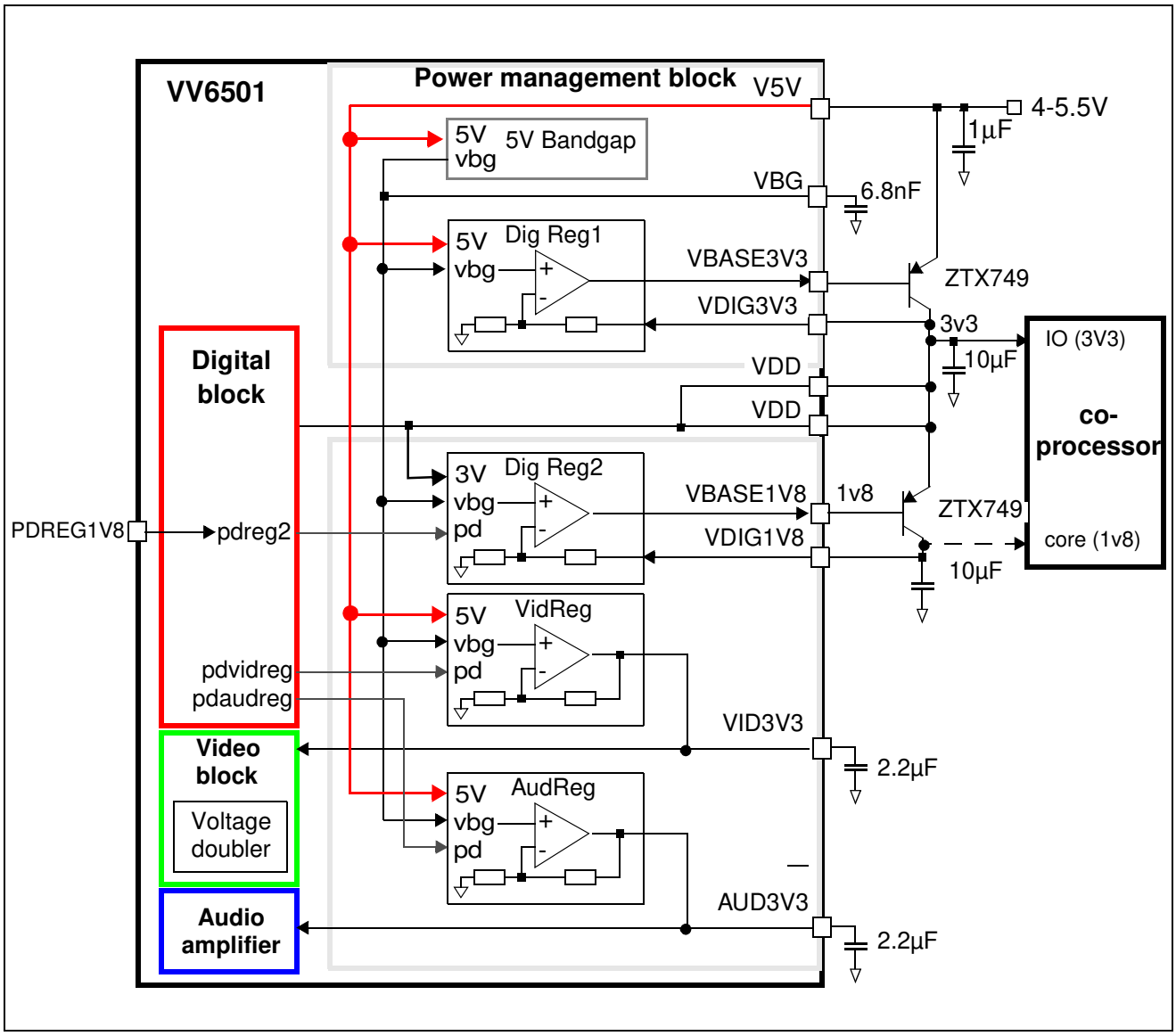
3.3 Power management

3.3.1 Voltage regulators

The power management block on the device avoids the requirement for any external system regulators in a 5 V based camera product. The scheme is shown in *Figure 19*.

- Digital Regulator 1 - This 5 V to 3.3 V regulator uses an external bipolar transistor to supply loads up to 200 mA. It is typically used to power the sensor digital logic and may also be used to supply an external co-processor if required. This regulator is **always** on.
- Digital Regulator2 - This 3.3 V to 1.8 V regulator uses an external bipolar transistor to supply loads up to 100 mA. This supply may be used for an external co-processor if required. This regulator is controlled by the PDREG1V8 pin and must be switched off if not required.
- Audio Amp Regulator - This 5 V to 3.3 V regulator supplies the audio amplifier and the buffer amplifier used to supply the reference to the microphone (Load 5 mA). It should be externally decoupled with a 2.2 µF capacitor. For applications without audio this regulator may be powered down via the SIF registers.
- Video Regulator - This 5 V to 3.3 V regulator supplies the analogue video circuitry. It should be externally decoupled with a 2.2 µF capacitor.

Figure 19: Voltage regulator block diagram



3.3.2 Power-on reset cell

The power-on reset cell generates a low going pulse whenever the digital power supplies are below their lower limits. The power-on reset signal resets the sensor internally and is also available on the PORB pin and may be used to reset a co-processor.

The PORB cell monitors both the 3V3 and 1V8 supplies. If the 1V8 supply is not required then PDVREG1V8 must be tied high.

Figure 20: Power-on reset block