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W25M02GV

Featuring

3V 2G-BIT (2 x 1G-BIT) SERIAL SLC NAND FLASH MEMORY WITH

DUAL/QUAD SPI BUFFER READ & CONTINUOUS READ CONCURRENT OPERATIONS

Publication Release Date: May 09, 2018
Revision F

winbond

Table of Contents

Table of Figures

1. GENERAL DESCRIPTIONS

The W25M02GV (2 x 1G-bit) Serial MCP (Multi Chip Package) Flash memory is based on the W25N Serial SLC NAND ***SpiFlash®*** series by stacking two individual W25N01GV die into a standard 8-pin package. It offers the highest memory density for the low pin-count package, as well as Concurrent Operations in Serial Flash memory for the first time. The W25M ***SpiStack®*** series is ideal for small form factor system designs, and applications that demand high Program/Erase data throughput. All W25N SpiFlash family devices are offered in space-saving packages which were impossible to use in the past for the typical NAND flash memory.

The ***SpiStack®*** product series introduces a new "Software Die Select (C2h)" instruction, and a factory assigned "Die ID#" for each stacked die. Each W25N01GV die can be accessed independently even though the interface is shared. The ***SpiStack®*** feature only allows a single die to be Active and have control of the SPI interface at any given time to avoid bus contention.

The W25M02GV supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz (104MHz x 2) for Dual I/O and 416MHz (104MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O instructions.

The W25M02GV provides a new Continuous Read Mode that allows for efficient access to the entire memory array with a single Read command. This feature is ideal for code shadowing applications. Additionally, the device supports JEDEC standard manufacturer and device ID, one 2,048-Byte Unique ID page, one 2,048-Byte parameter page and ten 2,048-Byte OTP pages. To provide better NAND flash memory manageability, user configurable internal ECC, bad block management are also available in W25M02GV.

2. FEATURES

- **New Family of SpiFlash Memories**
  - W25M02GV: 2x1G-bit / 2x128M-byte
  - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  - Dual SPI: CLK, /CS, IO_0, IO_1, /WP, /Hold
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - Compatible SPI serial flash commands
- **Highest Performance Serial NAND Flash**
  - 104MHz Standard/Dual/Quad SPI clocks
  - 208/416MHz equivalent Dual/Quad SPI
  - 50MB/S continuous data transfer rate
  - Fast Program/Erase performance
  - More than 100,000 erase/program cycles(4)
  - More than 10-year data retention
- **Efficient "Continuous Read Mode"(1)**
  - Alternative method to the Buffer Read Mode
  - No need to issue "Page Data Read" between Read commands
  - Allows direct read access to the entire array
- **Flexible "Concurrent Operations"**
  - Independent single die access
  - Allows "Read while Program/Erase"
  - Allows "Multi Die Program/Erase"
  - Improves Program/Erase throughput
- **Low Power, Wide Temperature Range**
  - Single 2.7 to 3.6V supply
  - 25mA active, 20µA standby current
  - -40°C to +85°C operating range
- **Flexible Architecture with 128KB blocks**
  - Uniform 128K-Byte Block Erase
  - Flexible page data load methods
- **Advanced Features**
  - On chip 1-Bit ECC for memory array
  - ECC status bits indicate ECC results
  - bad block management and LUT(2) access
  - Software and Hardware Write-Protect
  - Power Supply Lock-Down and OTP protection
  - 2KB Unique ID and 2KB parameter pages
  - Ten 2KB OTP pages(3)
- **Space Efficient Packaging**
  - 8-pad WSON 8x6-mm
  - 16-pin SOIC 300-mil
  - 24-ball TFBGA 8x6-mm
  - Contact Winbond for other package options

Notes:

1. Only the Read command structures are different between the "Continuous Read Mode" and the "Buffer Read Mode", all other commands are identical.
2. LUT stands for Look-Up Table.
3. OTP pages can only be programmed.
4. Endurance specification is based on the on-chip ECC or 1bit/528 byte ECC(Error Correcting Code)

3. PACKAGE TYPES AND PIN CONFIGURATIONS

W25M02GV is offered in an 8-pad WSON 8x6-mm (package code ZE), a 16-pin SOIC 300-mil (package code SF), and two 24-ball 8x6-mm TFBGA (package code TB & TC) packages as shown in Figure 1a-c respectively. Package diagrams and dimensions are illustrated at the end of this datasheet.

3.1 Pad Configuration WSON 8x6-mm

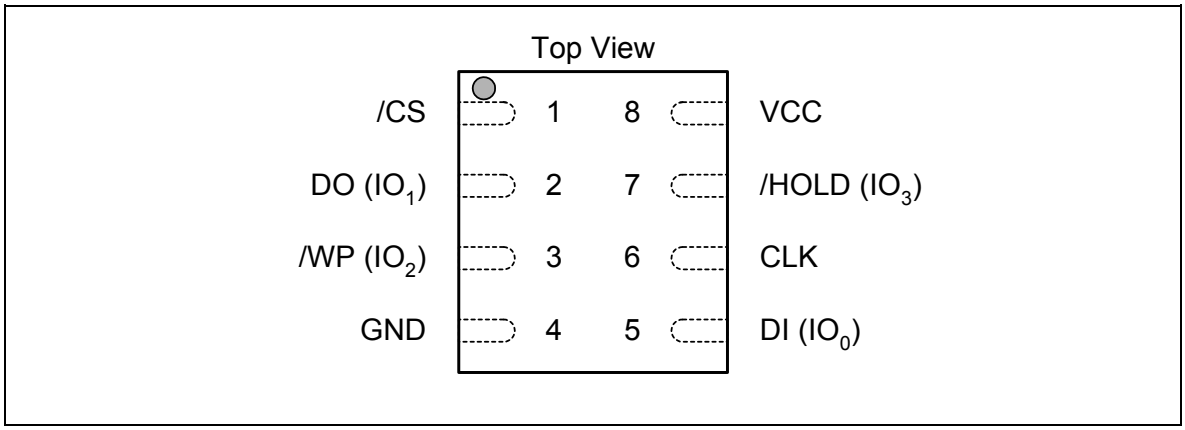


Figure 1a. W25M02GV Pad Assignments, 8-pad WSON 8x6-mm (Package Code ZE)

3.2 Pad Description WSON 8x6-mm

PAD NO.	PAD NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)(2)
8	VCC		Power Supply

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD functions are only available for Standard/Dual SPI.

3.3 Pin Configuration SOIC 300-mil

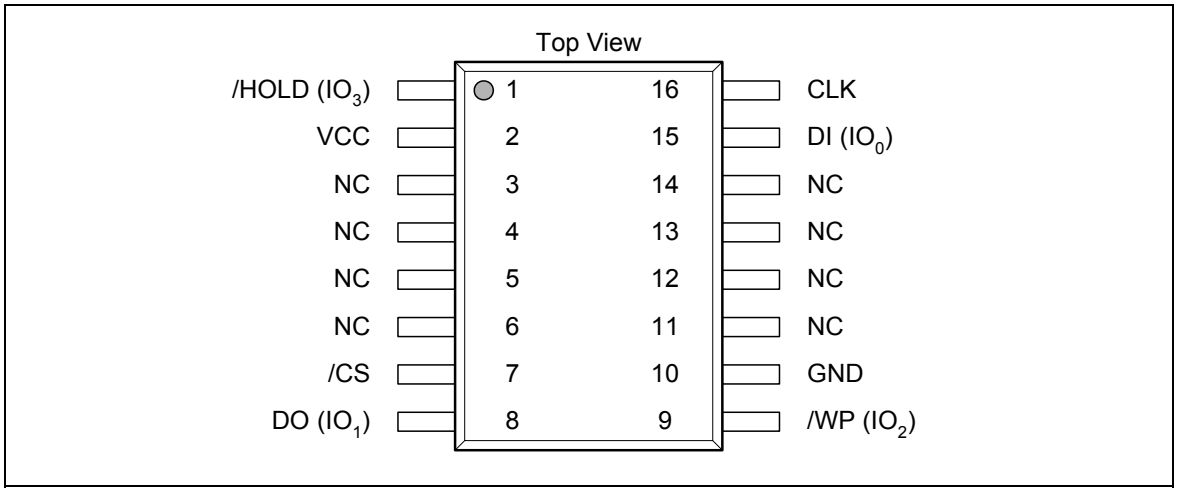


Figure 1b. W25M02GV Pin Assignments, 16-pin SOIC 300-mil (Package Code SF)

3.4 Pin Description SOIC 300-mil

PIN NO.	PIN NAME	I/O	FUNCTION
1	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)(2)
2	VCC		Power Supply
3	N/C		No Connect
4	N/C		No Connect
5	N/C		No Connect
6	N/C		No Connect
7	/CS	I	Chip Select Input
8	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
9	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
10	GND		Ground
11	N/C		No Connect
12	N/C		No Connect
13	N/C		No Connect
14	N/C		No Connect
15	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
16	CLK	I	Serial Clock Input

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD functions are only available for Standard/Dual SPI.

3.5 Ball Configuration TFBGA 8x6-mm (5x5 or 6x4 Ball Array)

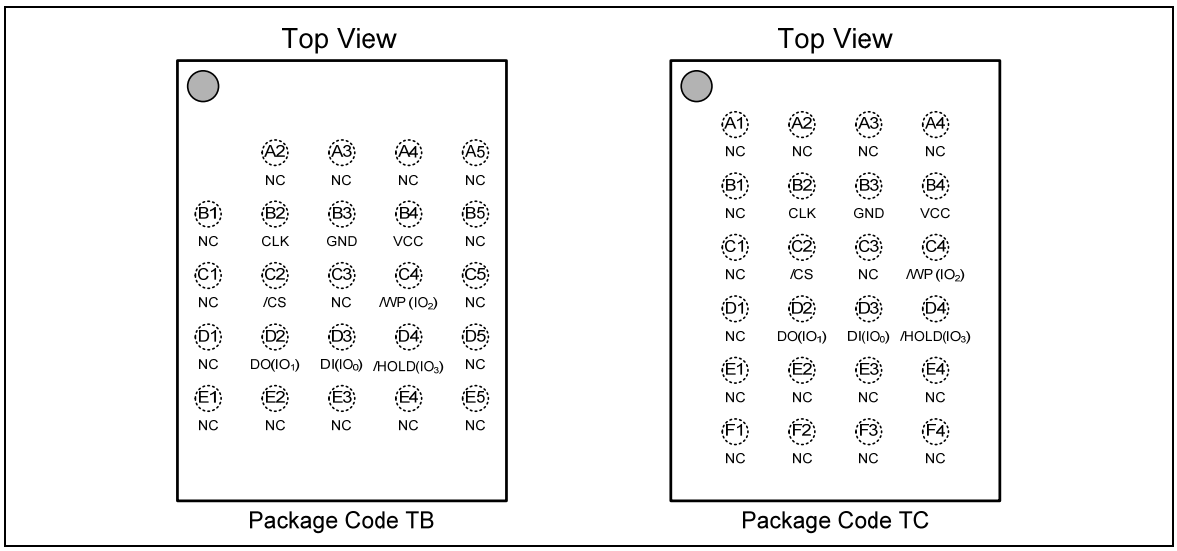


Figure 1c. W25M02GV Ball Assignments, 24-ball TFBGA 8x6-mm (Package Code TB & TC)

3.6 Ball Description TFBGA 8x6-mm

BALL NO.	PIN NAME	I/O	FUNCTION
B2	CLK	I	Serial Clock Input
B3	GND		Ground
B4	VCC		Power Supply
C2	/CS	I	Chip Select Input
C4	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
D2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
D3	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
D4	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)(2)
Multiple	NC		No Connect

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD functions are only available for Standard/Dual SPI.

4. PIN DESCRIPTIONS

4.1 Serial MCP (SpiStack®) Device Configuration

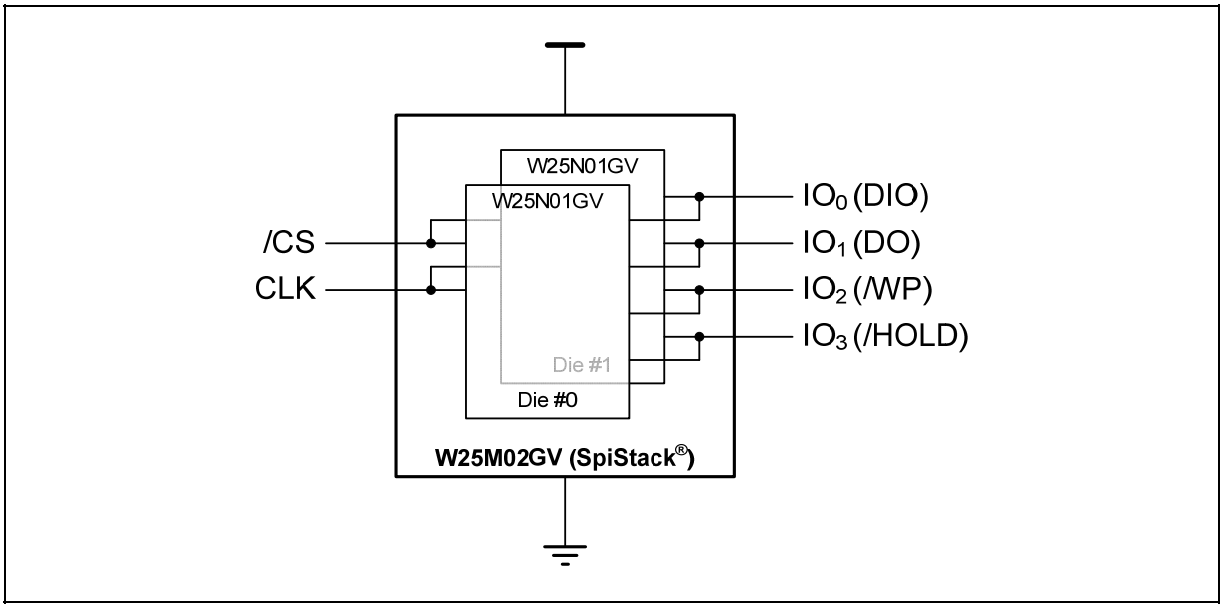


Figure 2a. W25M02GV Device Configuration

All signal pins are shared by the stacked dies within the package. Each die is assigned a “Die ID#” in the factory. Only a single die is active at any given time, and have the control of the SPI bus to communicate with the external SPI controller. However, all the dies will accept two instructions regardless their Active or Idle status: 1) “Software Die Select (C2h)” instruction; it is used to set any single die to be active according to the 8-bit Die ID following the instruction. 2) “Device Reset (FFh)” instruction; it is used to reset all the stacked dies to their power-up state. Die #0 will always be Active after power-up or Device Reset.

4.2 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down (see “Write Protection” and Figure 30b). If needed, a pull-up resistor on the /CS pin can be used to accomplish this.

4.3 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The W25M02GV supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.

4.4 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect bits BP[3:0] and Status Register Protect SRP bits SRP[1:0], a portion as small as 256K-Byte (2x128KB blocks) or up to the entire memory array can be hardware protected. The WP-E bit in the Protection Register (SR-1) controls the functions of the /WP pin.

When WP-E=0, the device is in the Software Protection mode that only SR-1 can be protected. The /WP pin functions as a data I/O pin for the Quad SPI operations, as well as an active low input pin for the Write Protection function for SR-1. Refer to section 7.1.3 for detail information.

When WP-E=1, the device is in the Hardware Protection mode that /WP becomes a dedicated active low input pin for the Write Protection of the entire device. If /WP is tied to GND, all "Write/Program/Erase" functions are disabled. The entire device (including all registers, memory array, OTP pages) will become read-only. Quad SPI read operations are also disabled when WP-E is set to 1.

4.5 HOLD (/HOLD)

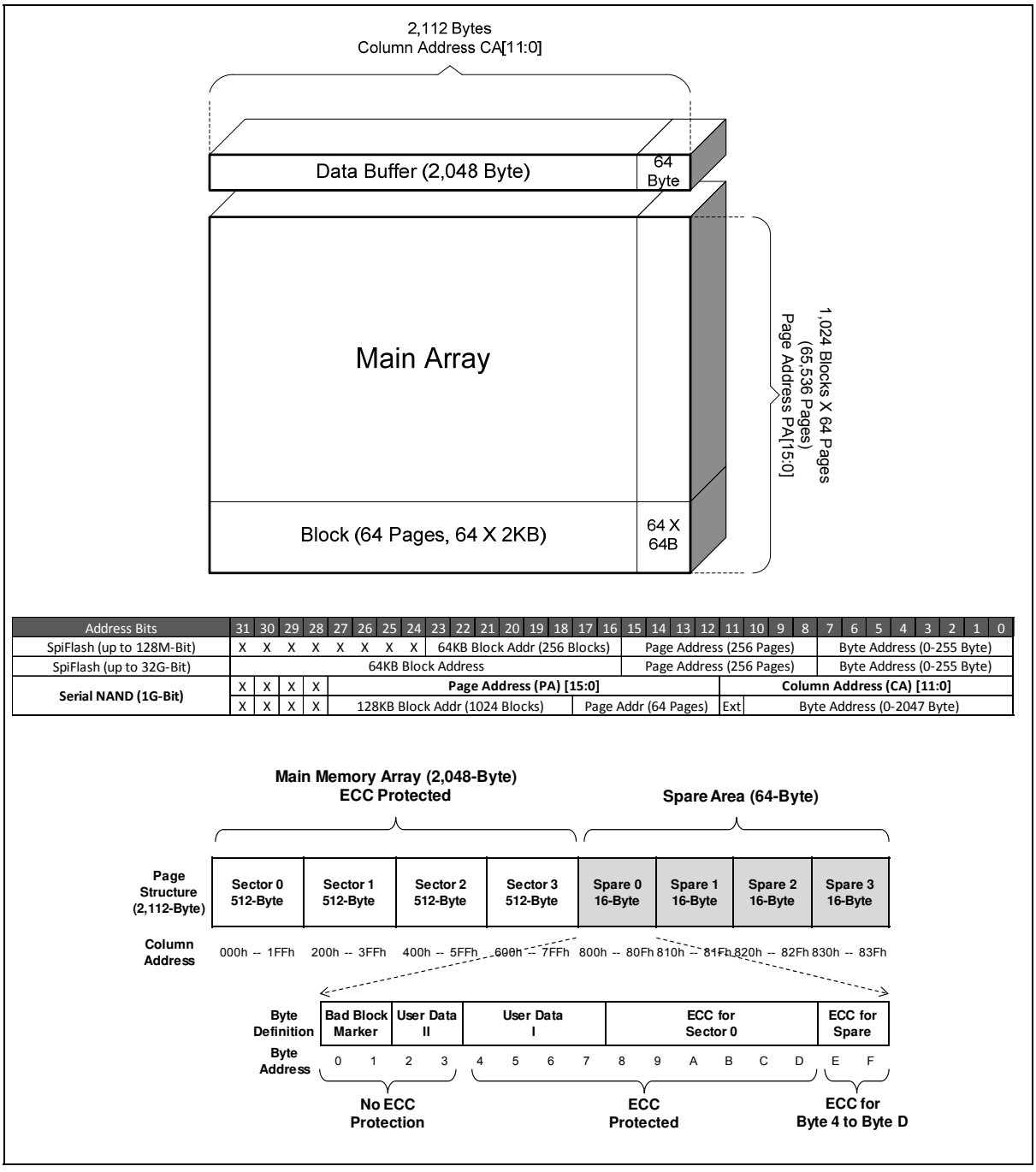
During Standard and Dual SPI operations, the /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low.

When a Quad SPI Read/Buffer Load command is issued, /HOLD pin will become a data I/O pin for the Quad operations and no HOLD function is available until the current Quad operation finishes. /HOLD (IO3) must be driven high by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the /HOLD input to float.

4.6 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

5. SINGLE DIE (W25N01GV) BLOCK DIAGRAM



Address Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SpiFlash (up to 128M-Bit)	X	X	X	X	X	X	X	X	64KB Block Addr (256 Blocks)								Page Address (256 Pages)								Byte Address (0-255 Byte)							
SpiFlash (up to 32G-Bit)	64KB Block Address																Page Address (256 Pages)								Byte Address (0-255 Byte)							
Serial NAND (1G-Bit)	X	X	X	X	**Page Address (PA) [15:0]**																**Column Address (CA) [11:0]**											
	X	X	X	X	128KB Block Addr (1024 Blocks)												Page Addr (64 Pages)				Ext	Byte Address (0-2047 Byte)										

Figure 2b. Single Die W25N01GV Flash Memory Architecture and Addressing

6. FUNCTIONAL DESCRIPTIONS

6.1 Device Operation Flow

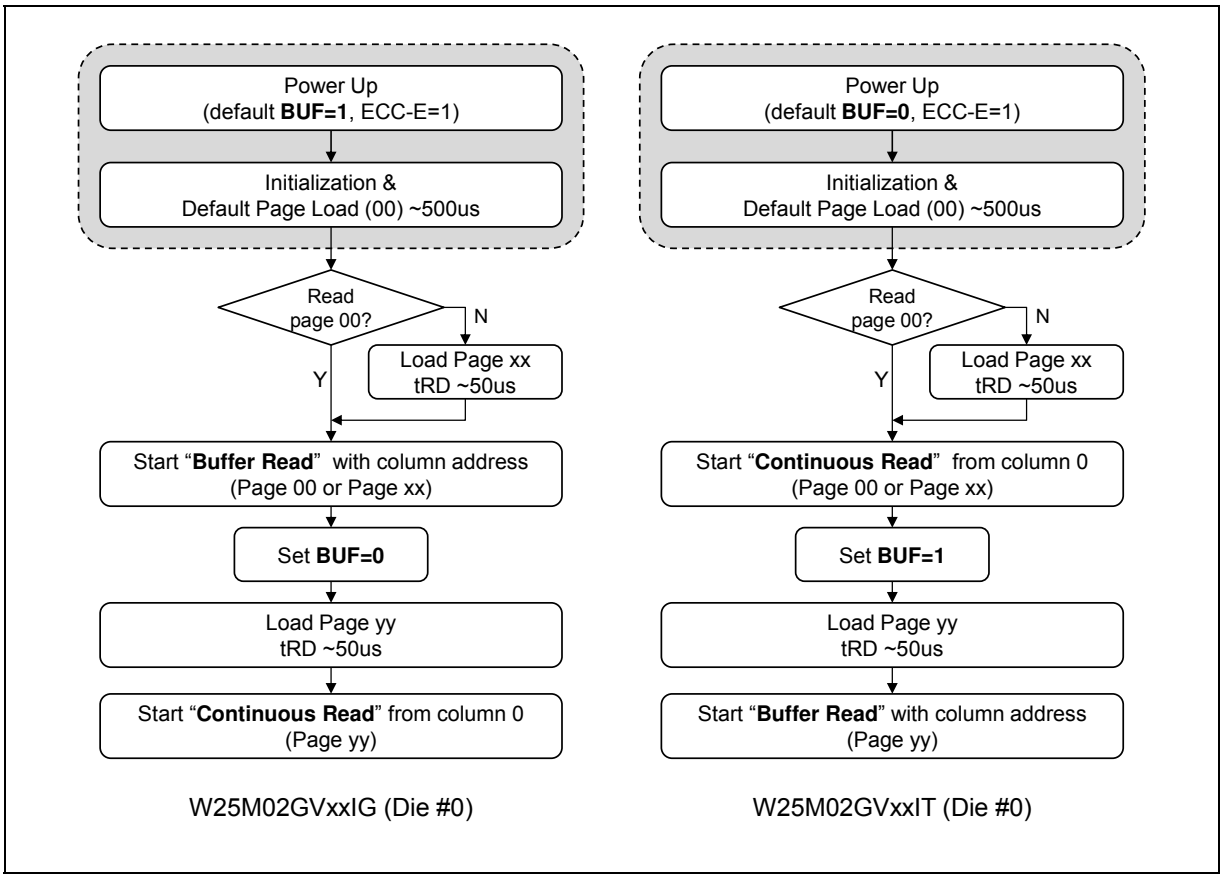


Figure 2c. W25M02GV Flash Memory Operation Diagram

6.1.1 Stacked Die Operations

Once the device is power on, Die #0 will be active and have control of the SPI bus. "Software Die Select (C2h)" instruction followed by the 8-bit Die ID can be used to select the active die. The active die is available to accept any instruction issued by the controller and perform specific operations. The inactive/idle die does not accept any other instructions except the "Software Die Select (C2h)" and "Device Reset (FFh)". However, the inactive/idle die can still perform internal Program/Erase operation which was initiated when the die was active. Therefore, "Read (on Active die) while Program/Erase (on Idle die)" and "Multi-die Program/Erase (both Active & Idle dies)" concurrent operations are feasible in the ***SpiStack®*** series. "Software Die Select (C2h)" instruction will only change the active/idle status of the stacked dies, and it will not interrupt any on-going Program/Erase operations.

6.1.2 Standard SPI Instructions

The W25M02GV is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions

use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

6.1.3 Dual SPI Instructions

The W25M02GV supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

6.1.4 Quad SPI Instructions

The W25M02GV supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)”, “Fast Read Quad I/O (EBh)” and “Quad Program Data Load (32h/34h)”. These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively.

6.1.5 Hold Function

For Standard SPI and Dual SPI operations, the /HOLD signal allows the W25M02GV operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The /HOLD function is only available for standard SPI and Dual SPI operation, not during Quad SPI. When a Quad SPI command is issued, /HOLD pin will act as a dedicated IO pin (IO3).

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will terminate after the next falling edge of CLK. During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active (low) for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

6.2 Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the W25M02GV provides several means to protect the data from inadvertent writes.

- Device resets when VCC is below threshold
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (/WP pin) write protection using Protection Register (SR-1)
- Lock Down write protection for Protection Register (SR-1) until the next power-up
- One Time Program (OTP) write protection for memory array using Protection Register (SR-1)
- Hardware write protection using /WP pin when WP-E is set to 1

Upon power-up or at power-down, the W25M02GV will maintain a reset condition while VCC is below the threshold value of V_{WI}, (See Power-up Timing and Voltage Levels and Figure 30a). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds V_{WI}, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Program Execute, Block Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached, and it must also track the VCC supply level at power-down to prevent adverse command sequence. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Program Execute, Block Erase or Bad Block Management instruction will be accepted. After completing a program or erase instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP0, SRP1) and Block Protect (TB, BP[3:0]) bits. These settings allow a portion or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Protection Register section for further information.

The WP-E bit in Protection Register (SR-1) is used to enable the hardware protection. When WP-E is set to 1, bringing /WP low in the system will block any Write/Program/Erase command to the W25M02GV, the device will become read-only. The Quad SPI operations are also disabled when WP-E is set to 1.

7. PROTECTION, CONFIGURATION AND STATUS REGISTERS

Three Status Registers are provided for each stacked W25N01GV die: Protection Register (SR-1), Configuration Register (SR-2) & Status Register (SR-3). Each register is accessed by Read Status Register and Write Status Register commands combined with 1-Byte Register Address respectively.

The Read Status Register instruction (05h / 0Fh) can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Read modes, Protection Register/OTP area lock status, Erase/Program results, ECC usage/status. The Write Status Register instruction can be used to configure the device write protection features, Software/Hardware write protection, Read modes, enable/disable ECC, Protection Register/OTP area lock. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP0, SRP1), the Write Enable instruction, and when WP-E is set to 1, the /WP pin.

7.1 Protection Register / Status Register-1 (Volatile Writable, OTP lockable)

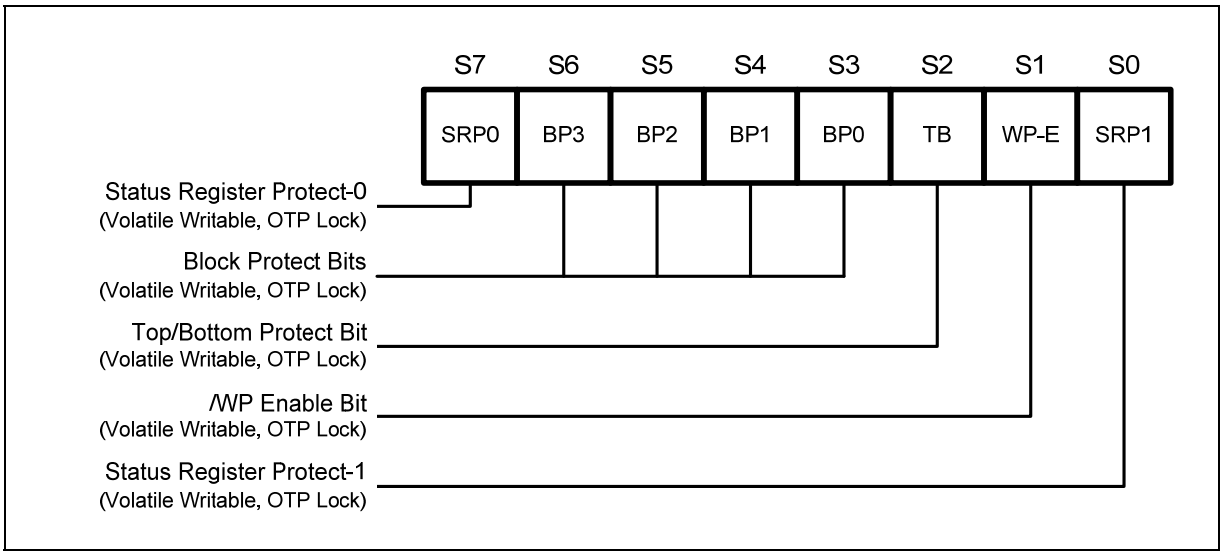


Figure 3a. Protection Register / Status Register-1 (Address Axh)

7.1.1 Block Protect Bits (BP3, BP2, BP1, BP0, TB) – *Volatile Writable, OTP lockable*

The Block Protect bits (BP3, BP2, BP1, BP0 & TB) are volatile read/write bits in the status register-1 (S6, S5, S4, S3 & S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction. All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The default values for the Block Protection bits are 1 after power up to protect the entire array. If the SR1-L bit in the Configuration Register (SR-2) is set to 1, the default values will the values that are OTP locked.

7.1.2 Write Protection Enable Bit (WP-E) – *Volatile Writable, OTP lockable*

The Write Protection Enable bit (WP-E) is a volatile read/write bits in the status register-1 (S1). The WP-E bit, in conjunction with SRP1 & SRP0, controls the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection, /WP pin functionality, and Quad SPI operation enable/disable. When WP-E = 0 (default value), the device is in Software Protection mode, /WP & /HOLD pins are multiplexed as IO pins, and Quad program/read functions are enabled all the time. When WP-E is set to 1, the device is in Hardware Protection mode, all Quad functions are disabled and /WP & /HOLD pins become dedicated control input pins.

7.1.3 Status Register Protect Bits (SRP1, SRP0) – *Volatile Writable, OTP lockable*

The Status Register Protect bits (SRP1 and SRP0) are volatile read/write bits in the status register (S0 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

Software Protection (Driven by Controller, Quad Program/Read is enabled)				
SRP1	**SRP0**	**WP-E**	**/WP / IO2**	**Descriptions**
0	0	0	X	No /WP functionality */WP pin will always function as IO2*
0	1	0	0	SR-1 cannot be changed (/WP = 0 during Write Status) */WP pin will function as IO2 for Quad operations*
0	1	0	1	SR-1 can be changed (/WP = 1 during Write Status) */WP pin will function as IO2 for Quad operations*
1	0	0	X	Power Lock Down(1) SR-1 */WP pin will always function as IO2*
1	1	0	X	Enter OTP mode to protect SR-1 (allow SR1-L=1) */WP pin will always function as IO2*

Hardware Protection (System Circuit / PCB layout, Quad Program/Read is disabled)				
SRP1	**SRP0**	**WP-E**	**/WP only**	**Descriptions**
0	X	1	VCC	SR-1 can be changed
1	0	1	VCC	Power Lock-Down(1) SR-1
1	1	1	VCC	Enter OTP mode to protect SR-1 (allow SR1-L=1)
X	X	1	GND	All "Write/Program/Erase" commands are blocked Entire device (SRs, Array, OTP area) is read-only

Notes:

1. When SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change SRP1, SRP0 to (0, 0) state.

7.2 Configuration Register / Status Register-2 (Volatile Writable)

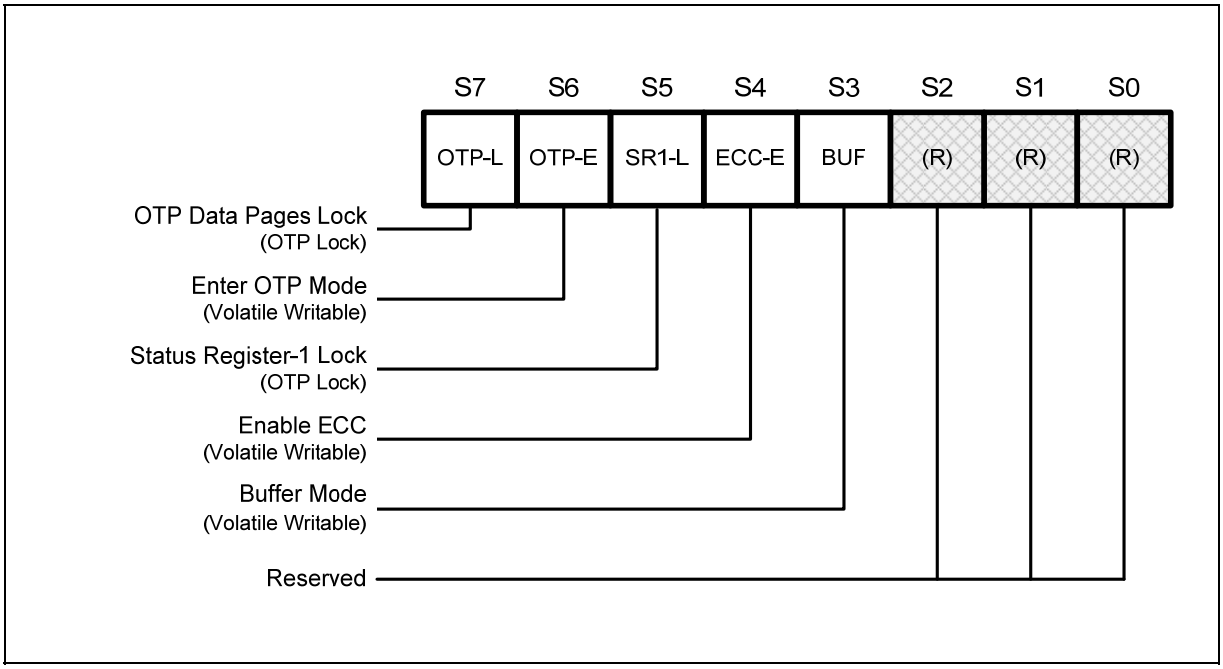


Figure 3b. Configuration Register / Status Register-2 (Address Bxh)

7.2.1 One Time Program Lock Bit (OTP-L) – *OTP lockable*

In addition to the main memory array, W25M02GV also provides an OTP area for the system to store critical data that cannot be changed once it's locked. The OTP area consists of 10 pages of 2,112-Byte each. The default data in the OTP area are FFh. Only Program command can be issued to the OTP area to change the data from "1" to "0", and data is not reversible ("0" to "1") by the Erase command. Once the correct data is programmed in and verified, the system developer can set OTP-L bit to 1, so that the entire OTP area will be locked to prevent further alteration to the data.

7.2.2 Enter OTP Access Mode Bit (OTP-E) – *Volatile Writable*

The OTP-E bit must be set to 1 in order to use the standard Program/Read commands to access the OTP area as well as to read the Unique ID / Parameter Page information. The default value after power up or a RESET command is 0.

7.2.3 Status Register-1 Lock Bit (SR1-L) – *OTP lockable*

The SR1-L lock bit is used to OTP lock the values in the Protection Register (SR-1). Depending on the settings in the SR-1, the device can be configured to have a portion of or up to the entire array to be write-protected, and the setting can be OTP locked by setting SR1-L bit to 1. SR1-L bit can only be set to 1 permanently when SRP1 & SRP0 are set to (1,1), and OTP Access Mode must be entered (OTP-E=1) to execute the programming. Please refer to 8.2.26 for detailed information.

7.2.4 ECC Enable Bit (ECC-E) – *Volatile Writable*

W25M02GV has a built-in ECC algorithm that can be used to preserve the data integrity. Internal ECC calculation is done during page programming, and the result is stored in the extra 64-Byte area for each page. During the data read operation, ECC engine will verify the data values according to the previously stored ECC information and to make necessary corrections if needed. The verification and correction status is indicated by the ECC Status Bits. ECC function is enabled by default when power on (ECC-E=1), and it will not be reset to 0 by the Device Reset command.

7.2.5 Buffer Read / Continuous Read Mode Bit (BUF) – *Volatile Writable*

Each stacked W25N01GV die provides two different modes for read operations, Buffer Read Mode (BUF=1) and Continuous Read Mode (BUF=0). Prior to any Read operation, a Page Data Read command is needed to initiate the data transfer from a specified page in the memory array to the Data Buffer. By default, after power up, the data in page 0 will be automatically loaded into the Data Buffer and the device is ready to accept any read commands.

The Buffer Read Mode (BUF=1) requires a Column Address to start outputting the existing data inside the Data Buffer, and once it reaches the end of the data buffer (Byte 2,111), DO (IO1) pin will become high-Z state.

The Continuous Read Mode (BUF=0) doesn't require the starting Column Address. The device will always start output the data from the first column (Byte 0) of the Data buffer, and once the end of the data buffer (Byte 2,048) is reached, the data output will continue through the next memory page. With Continuous Read Mode, it is possible to read out the entire memory array using a single read command. Please refer to respective command descriptions for the dummy cycle requirements for each read commands under different read modes.

For W25M02GVxxIG part number, the default value of BUF bit after power up is 1 for both stacked dies. BUF bit can be written to 0 individually in the Status Register-2 to perform the Continuous Read operation.

For W25M02GVxxIT part number, the default value of BUF bit after power up is 0 for both stacked dies. BUF bit can be written to 1 individually in the Status Register-2 to perform the Buffer Read operation.

BUF	ECC-E	Read Mode (Starting from Buffer)	ECC Status	Data Output Structure
1	0	Buffer Read	N/A	2,048 + 64
1	1	Buffer Read	Page based	2,048 + 64
0	0	Continuous Read	N/A	2,048
0	1	Continuous Read	Operation based	2,048

7.3 Status Register-3 (Status Only)

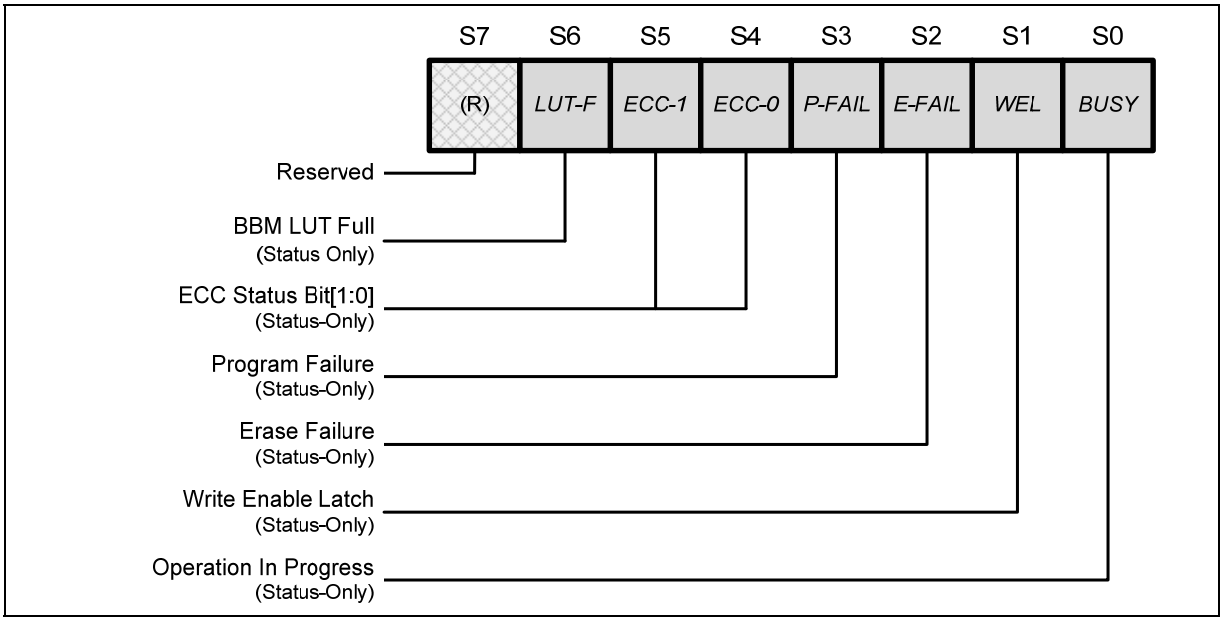


Figure 3c. Status Register-3 (Address Cxh)

7.3.1 Look-Up Table Full (LUT-F) – *Status Only*

To facilitate the NAND flash memory bad block management, each stacked W25N01GV die is equipped with an internal Bad Block Management Look-Up-Table (BBM LUT). Up to 20 bad memory blocks may be replaced by a good memory block respectively. The addresses of the blocks are stored in the internal Look-Up Table as Logical Block Address (LBA, the bad block) & Physical Block Address (PBA, the good block). The LUT-F bit indicates whether the 20 memory block links have been fully utilized or not. The default value of LUT-F is 0, once all 20 links are used, LUT-F will become 1, and no more memory block links may be established.

7.3.2 Cumulative ECC Status (ECC-1, ECC-0) – *Status Only*

ECC function is used in NAND flash memory to correct limited memory errors during read operations. The ECC Status Bits (ECC-1, ECC-0) should be checked after the completion of a Read operation to verify the data integrity. The ECC Status bits values are don't care if ECC-E=0. These bits will be cleared to 0 after a power cycle or a RESET command.

ECC Status		Descriptions
ECC-1	ECC-0	
0	0	Entire data output is **successful**, without any ECC correction.
0	1	Entire data output is **successful**, with 1~4 bit/page ECC corrections in either a single page or multiple pages.
1	0	Entire data output contains **more than 4 bits errors only in a single page which cannot be repaired by ECC**. In the Continuous Read Mode, an additional command can be used to read out the Page Address (PA) which had the errors.
1	1	Entire data output contains **more than 4 bits errors/page in multiple pages**. In the Continuous Read Mode, the additional command can only provide the last Page Address (PA) that had failures, the user cannot obtain the PAs for other failure pages. **Data is not suitable to use.**

Notes:

1. **ECC-1,ECC-0 = (1,1) is only applicable during Continuous Read operation (BUF=0).**

7.3.3 Program/Erase Failure (P-FAIL, E-FAIL) – *Status Only*

The Program/Erase Failure Bits are used to indicate whether the internally-controlled Program/Erase operation was executed successfully or not. These bits will also be set respectively when the Program or Erase command is issued to a locked or protected memory array or OTP area. Both bits will be cleared at the beginning of the Program Execute or Block Erase instructions as well as the device RESET instruction.

7.3.4 Write Enable Latch (WEL) – *Status Only*

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Program Execute, Block Erase, Page Data Read, Program Execute and Bad Block Management for OTP pages.

7.3.5 Erase/Program In Progress (BUSY) – *Status Only*

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is powering up or executing a Page Data Read, Bad Block Management, Program Execute, Block Erase, Program Execute for OTP area, OTP Locking or after a Continuous Read instruction. During this time the device will ignore further instructions except for the Read Status Register and Read JEDEC ID instructions. When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

7.3.6 Reserved Bits – *Non Functional*

There are a few reserved Status Register bits that may be read out as a “0” or “1”. It is recommended to ignore the values of those bits. During a “Write Status Register” instruction, the Reserved Bits can be written as “0”, but there will not be any effects.

7.4 Single Die W25N01GV Status Register Memory Protection

STATUS REGISTER[1]					W25N01GV (1G-BIT / 128M-BYTE) MEMORY PROTECTION[2]			
TB	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED PAGE ADDRESS PA[15:0]	PROTECTED DENSITY	PROTECTED PORTION
X	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	1022 & 1023	FF80h - FFFFh	256KB	Upper 1/512
0	0	0	1	0	1020 thru 1023	FF00h - FFFFh	512KB	Upper 1/256
0	0	0	1	1	1016 thru 1023	FE00h - FFFFh	1MB	Upper 1/128
0	0	1	0	0	1008 thru 1023	FC00h - FFFFh	2MB	Upper 1/64
0	0	1	0	1	992 thru 1023	F800h - FFFFh	4MB	Upper 1/32
0	0	1	1	0	960 thru 1023	F000h - FFFFh	8MB	Upper 1/16
0	0	1	1	1	896 thru 1023	E000h - FFFFh	16MB	Upper 1/8
0	1	0	0	0	768 thru 1023	C000h - FFFFh	32MB	Upper 1/4
0	1	0	0	1	512 thru 1023	8000h - FFFFh	64MB	Upper 1/2
1	0	0	0	1	0 & 1	0000h – 007Fh	256KB	Lower 1/512
1	0	0	1	0	0 thru 3	0000h - 00FFh	512KB	Lower 1/256
1	0	0	1	1	0 thru 7	0000h - 01FFh	1MB	Lower 1/128
1	0	1	0	0	0 thru 15	0000h - 03FFh	2MB	Lower 1/64
1	0	1	0	1	0 thru 31	0000h - 07FFh	4MB	Lower 1/32
1	0	1	1	0	0 thru 63	0000h - 0FFFh	8MB	Lower 1/16
1	0	1	1	1	0 thru 127	0000h - 1FFFh	16MB	Lower 1/8
1	1	0	0	0	0 thru 255	0000h - 3FFFh	32MB	Lower 1/4
1	1	0	0	1	0 thru 511	0000h - 7FFFh	64MB	Lower 1/2
X	1	0	1	X	0 thru 1023	0000h - FFFFh	128MB	ALL
X	1	1	X	X	0 thru 1023	0000h - FFFFh	128MB	ALL

Notes:

1. X = don't care
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

8. INSTRUCTIONS

The Standard/Dual/Quad SPI instruction set for each stacked W25N01GV die consists of 28 basic instructions that are fully controlled through the SPI bus (see Instruction Set Table1, 2). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in Figures 4 through 29. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the device is performing Program or Erase operation, BBM management, Page Data Read or OTP locking operations, BUSY bit will be high, and all instructions except for Read Status Register or Read JEDEC ID will be ignored until the current operation cycle has completed.

8.1 Device ID and Instruction Set Tables

8.1.1 Manufacturer and Device Identification

MANUFACTURER ID	**(MF7 - MF0)**
Winbond Serial Flash	EFh
Device ID	**(ID15 - ID0)**
Single Die W25N01GV 2x stacked	AB21h

8.1.2 Instruction Set Table 1 (Continuous Read, BUF = 0, xxIT Default Power Up Mode)(11)

Commands	OpCode	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7	Byte8	Byte9
Device RESET	**FFh**								
Software Die Select	**C2h**	Die ID7-0							
JEDEC ID	**9Fh**	Dummy	***EFh***	***ABh***	***21h***				
Read Status Register	**0Fh** / **05h**	SR Addr	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***
Write Status Register	**1Fh** / **01h**	SR Addr	S7-0						
Write Enable	**06h**								
Write Disable	**04h**								
BB Management (Swap Blocks)	**A1h**	LBA	LBA	PBA	PBA				
Read BBM LUT	**A5h**	Dummy	***LBA0***	***LBA0***	***PBA0***	***PBA0***	***LBA1***	***LBA1***	***PBA1***
Last ECC failure Page Address	**A9h**	Dummy	***PA15-8***	***PA7-0***					
Block Erase	**D8h**	Dummy	**PA15-8**	**PA7-0**					
Program Data Load (Reset Buffer)	**02h**	**CA15-8**	**CA7-0**	Data-0	Data-1	Data-2	Data-3	Data-4	Data-5
Random Program Data Load	**84h**	**CA15-8**	**CA7-0**	Data-0	Data-1	Data-2	Data-3	Data-4	Data-5
Quad Program Data Load (Reset Buffer)	**32h**	**CA15-8**	**CA7-0**	Data-0 / 4	Data-1 / 4	Data-2 / 4	Data-3 / 4	Data-4 / 4	Data-5 / 4
Random Quad Program Data Load	**34h**	**CA15-8**	**CA7-0**	Data-0 / 4	Data-1 / 4	Data-2 / 4	Data-3 / 4	Data-4 / 4	Data-5 / 4
Program Execute	**10h**	Dummy	**PA15-8**	**PA7-0**					
Page Data Read	**13h**	Dummy	**PA15-8**	**PA7-0**					
Read	**03h**	Dummy	Dummy	Dummy	***D7-0***	***D7-0***	***D7-0***	***D7-0***	***D7-0***
Fast Read	**0Bh**	Dummy	Dummy	Dummy	Dummy	***D7-0***	***D7-0***	***D7-0***	***D7-0***
Fast Read with 4-Byte Address	**0Ch**	Dummy	Dummy	Dummy	Dummy	Dummy	***D7-0***	***D7-0***	***D7-0***
Fast Read Dual Output	**3Bh**	Dummy	Dummy	Dummy	Dummy	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***
Fast Read Dual Output with 4-Byte Address	**3Ch**	Dummy	Dummy	Dummy	Dummy	Dummy	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***
Fast Read Quad Output	**6Bh**	Dummy	Dummy	Dummy	Dummy	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***
Fast Read Quad Output with 4-Byte Address	**6Ch**	Dummy	Dummy	Dummy	Dummy	Dummy	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***
Fast Read Dual I/O	**BBh**	Dummy / 2	Dummy / 2	Dummy / 2	Dummy / 2	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***
Fast Read Dual I/O with 4-Byte Address	**BCh**	Dummy / 2	Dummy / 2	Dummy / 2	Dummy / 2	Dummy / 2	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***
Fast Read Quad I/O	**EBh**	Dummy / 4	Dummy / 4	Dummy / 4	Dummy / 4	Dummy / 4	Dummy / 4	***D7-0 / 4***	***D7-0 / 4***
Fast Read Quad I/O with 4-Byte Address	**ECh**	Dummy / 4	Dummy / 4	Dummy / 4	Dummy / 4	Dummy / 4	Dummy / 4	Dummy / 4	***D7-0 / 4***