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16M-BIT
SERIAL FLASH MEMORY WITH
DUAL AND QUAD SPI

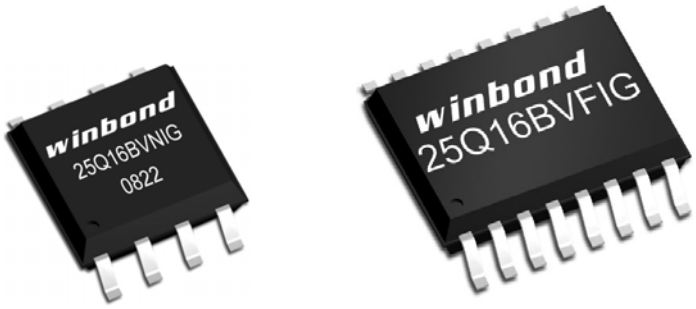

Table of Contents

1. GENERAL DESCRIPTION

The W25Q16BV (16M-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25Q series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The devices operate on a single 2.7V to 3.6V power supply with current consumption as low as 4mA active and 1µA for power-down. All devices are offered in space-saving packages.

The W25Q16BV array is organized into 8,192 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The W25Q16BV has 512 erasable sectors and 32 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See figure 2.)

The W25Q16BV supports the standard Serial Peripheral Interface (SPI), and a high performance Dual/Quad output as well as Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz for Dual Output and 416MHz for Quad Output when using the Fast Read Dual/Quad Output instructions. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories. The Continuous Read Mode allows for efficient memory access with as few as 8-clocks of instruction-overhead to read a 24-bit address, allowing true XIP (execute in place) operation.

A Hold pin, Write Protect pin and programmable write protection, with top or bottom array control, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device identification with a 64-bit Unique Serial Number.

2. FEATURES

- **Family of SpiFlash Memories**
  - W25Q16BV: 16M-bit / 2M-byte (2,097,152)
  - 256-bytes per programmable page
- **Standard, Dual or Quad SPI**
  - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  - Dual SPI: CLK, /CS, IO0, IO1, /WP, /Hold
  - Quad SPI: CLK, /CS, IO0, IO1, IO2, IO3
- **Highest Performance Serial Flash**
  - Up to 8X that of ordinary Serial Flash
  - 104MHz clock operation
  - 208MHz equivalent Dual SPI
  - 416MHz equivalent Quad SPI
  - 50MB/S continuous data transfer rate
- **Efficient "Continuous Read Mode"**
  - Low Instruction overhead
  - As few as 8 clocks to address memory
  - Allows true XIP (execute in place) operation
  - Outperforms X16 Parallel Flash
- **Low Power, Wide Temperature Range**
  - Single 2.7 to 3.6V supply
  - 4mA active current, <1µA Power-down (typ.)
  - -40°C to +85°C operating range
- **Flexible Architecture with 4KB sectors**
  - Uniform Sector Erase (4K-bytes)
  - Block Erase (32K and 64K-bytes)
  - Program one to 256 bytes
  - More than 100,000 erase/write cycles
  - More than 20-year data retention
- **Advanced Security Features**
  - Software and Hardware Write-Protect
  - Top or Bottom, Sector or Block selection
  - Lock-Down and OTP protection(1)
  - 64-Bit Unique ID for each device
- **Space Efficient Packaging**
  - 8-pin SOIC 150(2)/208-mil
  - 8-pad WSON 6x5-mm
  - 8-pin PDIP 300-mil(2)
  - 16-pin SOIC 300-mil(2)
  - Contact Winbond for KGD and other options

Notes 1. Refer to Ordering Information.
2. These package types are Special Order Only, please contact Winbond for more information.

3. PIN CONFIGURATION SOIC 150 / 208-MIL

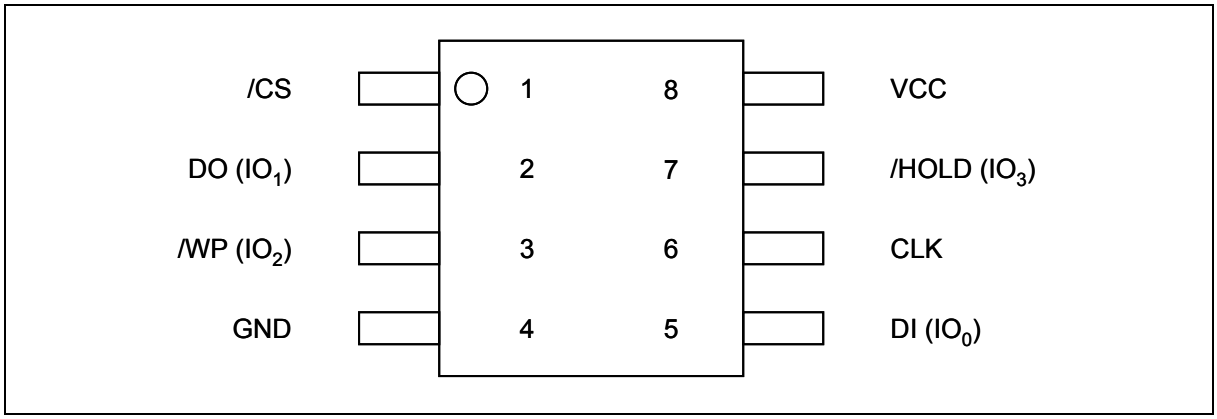

Figure 1a. W25Q16BV Pin Assignments, 8-pin SOIC 150 / 208-mil (Package Code SN & SS)

4. PAD CONFIGURATION WSON 6X5-MM

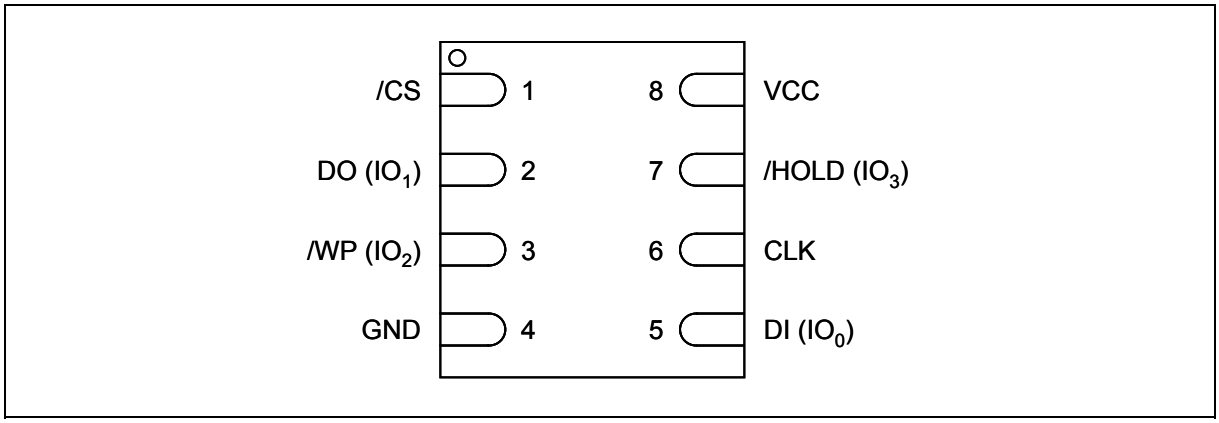

Figure 1b. W25Q16BV Pad Assignments, 8-pad WSON 6x5-mm(Package Code ZP)

5. PAD CONFIGURATION PDIP 300-MIL

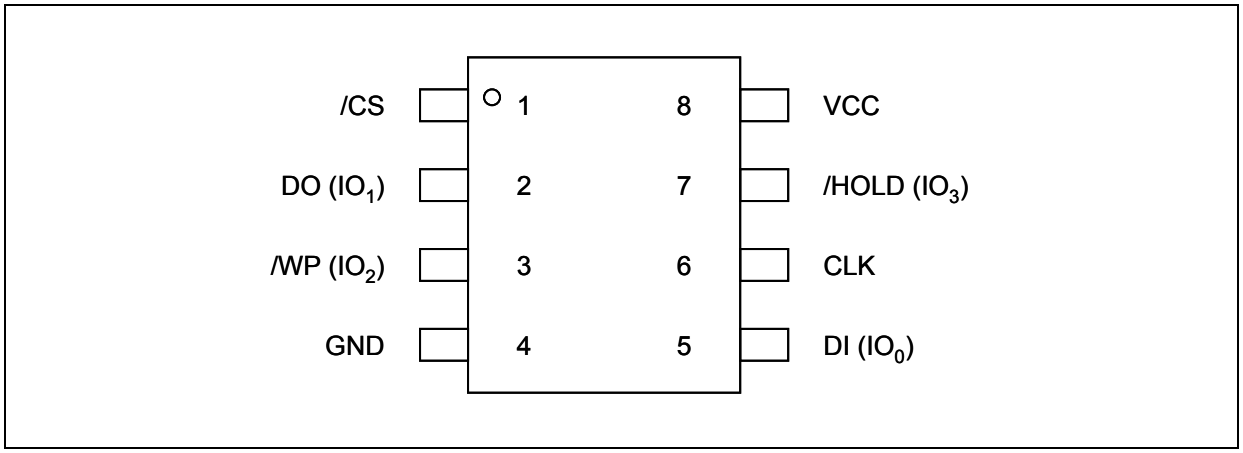

Figure 1c. W25Q16BV Pin Assignments, 8-pin PDIP (Package Code DA)

6. PIN DESCRIPTION SOIC 150/208-MIL, PDIP 300-MIL AND WSON 6X5-MM

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)*1
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)*2
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)*1
6	CLK	I	Serial Clock Input
7	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)*2
8	VCC		Power Supply

*1 IO0 and IO1 are used for Standard and Dual SPI instructions

*2 IO0 – IO3 are used for Quad SPI instructions

7. PIN CONFIGURATION SOIC 300-MIL

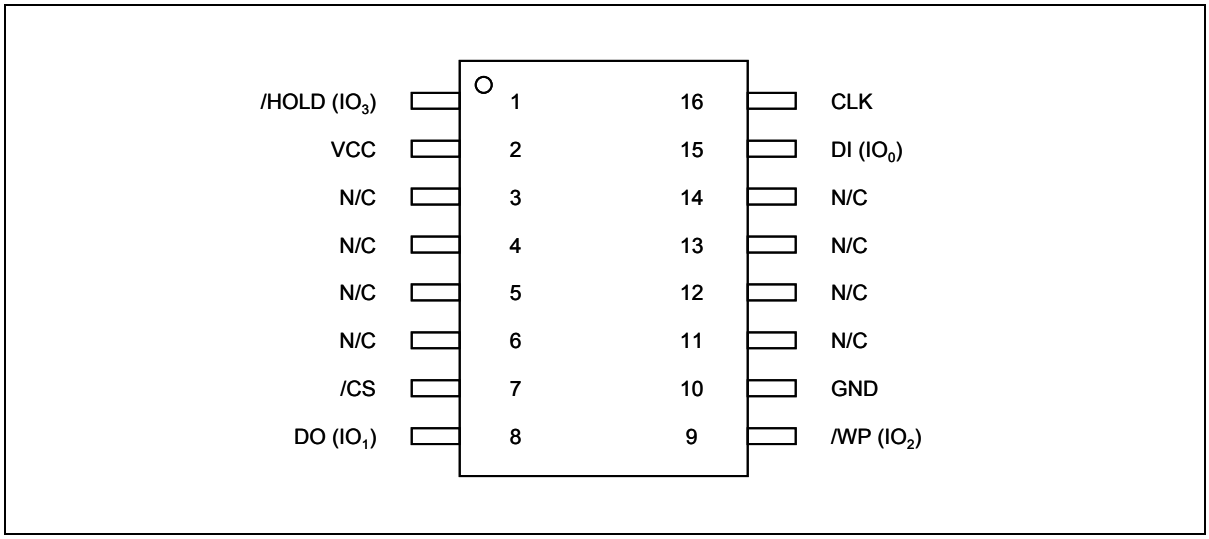

Figure 1d. W25Q16BV Pin Assignments, 16-pin SOIC 300-mil (Package Code SF)

8. PIN DESCRIPTION SOIC 300-MIL

PAD NO.	PAD NAME	I/O	FUNCTION
1	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)*2
2	VCC		Power Supply
3	N/C		No Connect
4	N/C		No Connect
5	N/C		No Connect
6	N/C		No Connect
7	/CS	I	Chip Select Input
8	DO (IO1)	I/O	Data Output (Data Input Output 1)*1
9	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)*2
10	GND		Ground
11	N/C		No Connect
12	N/C		No Connect
13	N/C		No Connect
14	N/C		No Connect
15	DI (IO0)	I/O	Data Input (Data Input Output 0)*1
16	CLK	I	Serial Clock Input

*1 IO0 and IO1 are used for Standard and Dual SPI instructions

*2 IO0 – IO3 are used for Quad SPI instructions

8.1 Package Types

W25Q16BV is offered in an 8-pin plastic 150-mil or 208-mil width SOIC (package code SN & SS) and 6x5-mm WSON (package code ZP) as shown in figure 1a, and 1b, respectively. The 300-mil 8-pin PDIP is another option of package selections (Figure 1c). The W25Q16BV is also offered in a 16-pin plastic 300-mil width SOIC (package code SF) as shown in figure 1d. Package diagrams and dimensions are illustrated at the end of this datasheet.

8.2 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up (see “Write Protection” and figure 32). If needed a pull-up resister on /CS can be used to accomplish this.

8.3 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The W25Q16BV supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge CLK.

Dual and Quad SPI instruction use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1 the /WP pin becomes IO2 and /HOLD pin becomes IO3.

8.4 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect (SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion or the entire memory array can be hardware protected. The /WP pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /WP pin (Hardware Write Protect) function is not available since this pin is used for IO2. See figure 1a, 1b, 1c, and 1d for the pin configuration of Quad I/O operation.

8.5 HOLD (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /HOLD pin function is not available since this pin is used for IO3. See figure 1a-d for the pin configuration of Quad I/O operation.

8.6 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

9. BLOCK DIAGRAM

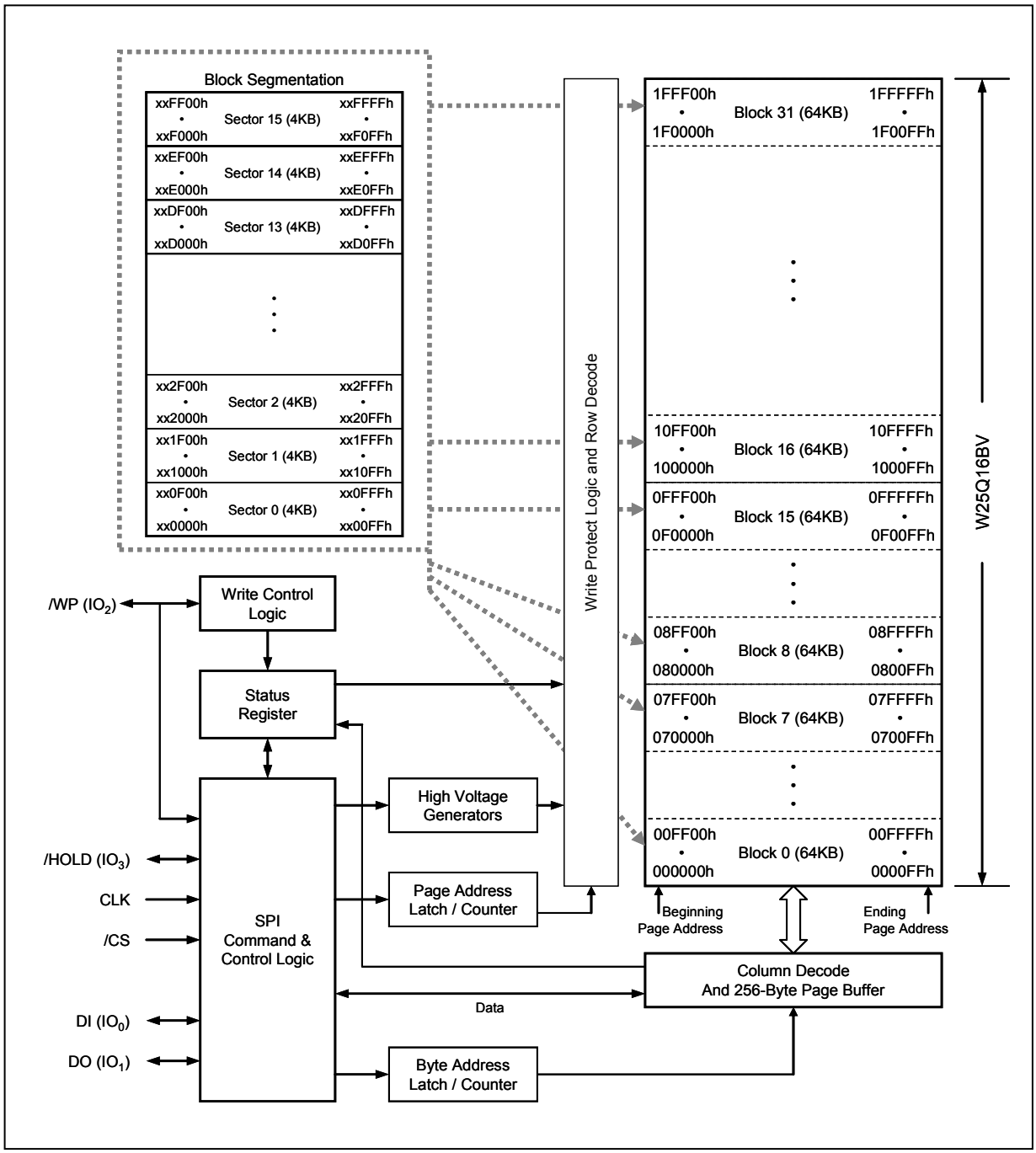

Figure 2. W25Q16BV Serial Flash Memory Block Diagram

10. FUNCTIONAL DESCRIPTION

10.1 SPI OPERATIONS

10.1.1 Standard SPI Instructions

The W25Q16BV is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge CLK.

SPI bus operation Modes 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3 the CLK signal is normally high on the falling and rising edges of /CS.

10.1.2 Dual SPI Instructions

The W25Q16BV supports Dual SPI operation when using the “Fast Read Dual Output and Dual I/O” (3B and BB hex) instructions. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

10.1.3 Quad SPI Instructions

The W25Q16BV supports Quad SPI operation when using the “Fast Read Quad Output”, “Fast Read Quad I/O”, “Word Read Quad I/O” and “Octal Word Quad I/O” (6B, EB, E7 and E3 hex respectively). These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

10.1.4 Hold Function

The /HOLD signal allows the W25Q16BV operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The /HOLD function is only available for standard SPI and Dual SPI operation, not during Quad SPI.

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will terminate after the next falling edge of CLK. During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active (low) for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

10.2 WRITE PROTECTION

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern the W25Q16BV provides several means to protect data from inadvertent writes.

10.2.1 Write Protect Features

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after program and erase
- Software and Hardware (/WP pin) write protection using Status Register
- Write Protection using Power-down instruction
- Lock Down write protection until next power-up(1)
- One Time Program (OTP) write protection(1)

Note 1: These features are available upon special order. Please refer to Ordering Information.

Upon power-up or at power-down, the W25Q16BV will maintain a reset condition while VCC is below the threshold value of V_{WI}, (See Power-up Timing and Voltage Levels and Figure 32). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds V_{WI}, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP0, SRP1) and Block Protect (SEC,TB, BP2, BP1 and BP0) bits. These settings allow a portion or all of the memory to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

11. CONTROL AND STATUS REGISTERS

The Read Status Register-1 and Status Register-2 instructions can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled, the state of write protection, the Quad SPI setting and Erase Suspend status. The Write Status Register instruction can be used to configure the devices write protection features and Quad SPI setting. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP0, SRP1), the Write Enable instruction, and in some cases the /WP pin.

11.1 STATUS REGISTER

11.1.1 BUSY

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction. During this time the device will ignore further instructions except for the Read Status Register and Erase Suspend instruction (see t_W, t_{PP}, t_{SE}, t_{BE}, and t_{CE} in AC Characteristics). When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

11.1.2 Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to a 1 after executing a Write Enable Instruction. The WEL status bit is cleared to a 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register.

11.1.3 Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see t_W in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

11.1.4 Top/Bottom Block Protect (TB)

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP0, SRP1 and WEL bits.

11.1.5 Sector/Block Protect (SEC)

The non-volatile Sector protect bit (SEC) controls if the Block Protect Bits (BP2, BP1, BP0) protect 4KB Sectors (SEC=1) or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The default setting is SEC=0.

11.1.6 Status Register Protect (SRP1, SRP0)

The Status Register Protect bits (SRP1 and SRP0) are non-volatile read/write bits in the status register (S8 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

SRP1	SRP0	/WP	Status Register	Description
0	0	X	Software Protection	/WP pin has no control. The Status register can be written to after a Write Enable instruction, WEL=1. [Factory Default]
0	1	0	Hardware Protected	When /WP pin is low the Status Register locked and can not be written to.
0	1	1	Hardware Unprotected	When /WP pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	0	X	Power Supply Lock-Down(1)	Status Register is protected and can not be written to again until the next power-down, power-up cycle.(2)
1	1	X	One Time Program(1)	Status Register is permanently protected and can not be written to.

Note:
1. These features are available upon special order. Please refer to Ordering Information.
2. When SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change SRP1, SRP0 to (0, 0) state.

11.1.7 Erase Suspend Status (SUS)

The Suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing an Erase Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase Resume (7Ah) instruction as well as a power-down, power-up cycle.

11.1.8 Quad Enable (QE)

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI operation. When the QE bit is set to a 0 state (factory default), the /WP pin and /HOLD are enabled. When the QE bit is set to a 1, the Quad IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled.

WARNING: If the /WP or /HOLD pins are tied directly to the power supply or ground during standard SPI or Dual SPI operation, the QE bit should never be set to a 1.

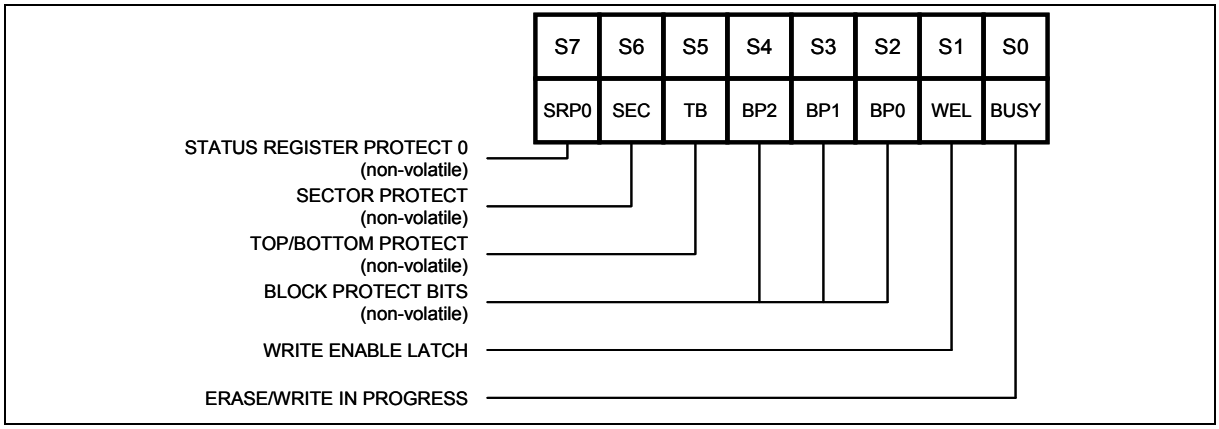

Figure 3a. Status Register-1

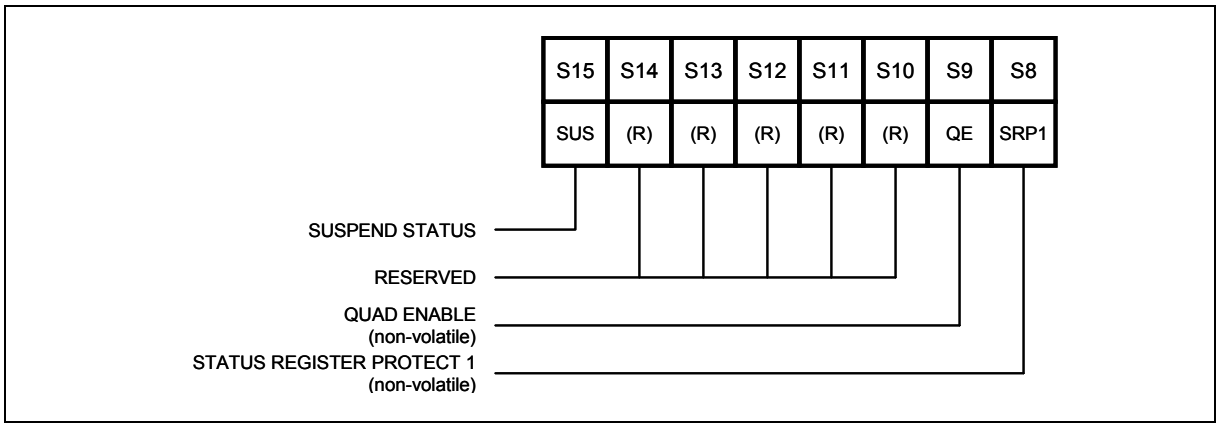

Figure 3b. Status Register-2

11.1.9 Status Register Memory Protection

STATUS REGISTER(1)					W25Q16BV (16M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	31	1F0000h – 1FFFFFh	64KB	Upper 1/32
0	0	0	1	0	30 and 31	1E0000h – 1FFFFFh	128KB	Upper 1/16
0	0	0	1	1	28 thru 31	1C0000h – 1FFFFFh	256KB	Upper 1/8
0	0	1	0	0	24 thru 31	180000h – 1FFFFFh	512KB	Upper 1/4
0	0	1	0	1	16 thru 31	100000h – 1FFFFFh	1MB	Upper 1/2
0	1	0	0	1	0	000000h – 00FFFFh	64KB	Lower 1/32
0	1	0	1	0	0 and 1	000000h – 01FFFFh	128KB	Lower 1/16
0	1	0	1	1	0 thru 3	000000h – 03FFFFh	256KB	Lower 1/8
0	1	1	0	0	0 thru 7	000000h – 07FFFFh	512KB	Lower 1/4
0	1	1	0	1	0 thru 15	000000h – 0FFFFFh	1MB	Lower 1/2
X	X	1	1	X	0 thru 31	000000h – 1FFFFFh	2MB	ALL
1	0	0	0	1	31	1FF000h – 1FFFFFh	4KB	Top Block
1	0	0	1	0	31	1FE000h – 1FFFFFh	8KB	Top Block
1	0	0	1	1	31	1FC000h – 1FFFFFh	16KB	Top Block
1	0	1	0	X	31	1F8000h – 1FFFFFh	32KB	Top Block
1	1	0	0	1	0	000000h – 000FFFh	4KB	Bottom Block
1	1	0	1	0	0	000000h – 001FFFh	8KB	Bottom Block
1	1	0	1	1	0	000000h – 003FFFh	16KB	Bottom Block
1	1	1	0	X	0	000000h – 007FFFh	32KB	Bottom Block

Note:
1. x = don't care

11.2 INSTRUCTIONS

The instruction set of the W25Q16BV consists of thirty basic instructions that are fully controlled through the SPI bus (see Instruction Set table1-3). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in figures 4 through 32. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be terminated. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

11.2.1 Manufacturer and Device Identification

MANUFACTURER ID	**(M7-M0)**	
Winbond Serial Flash	EFh	
Device ID	**(ID7-ID0)**	**(ID15-ID0)**
Instruction	**ABh, 90h**	**9Fh**
W25Q16BV	14h	4015h

11.2.2 Instruction Set Table 1 (Erase, Program Instructions)(1)

INSTRUCTION NAME	BYTE 1 (CODE)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Write Enable	**06h**					
Write Disable	**04h**					
Read Status Register-1	**05h**	(S7–S0) (2)				
Read Status Register-2	**35h**	(S15-S8) (2)				
Write Status Register	**01h**	(S7–S0)	(S15-S8)			
Page Program	**02h**	A23–A16	A15–A8	A7–A0	(D7–D0)	
Quad Page Program	**32h**	A23–A16	A15–A8	A7–A0	(D7–D0, …)(3)	
Sector Erase (4KB)	**20h**	A23–A16	A15–A8	A7–A0		
Block Erase (32KB)	**52h**	A23–A16	A15–A8	A7–A0		
Block Erase (64KB)	**D8h**	A23–A16	A15–A8	A7–A0		
Chip Erase	**C7h/60h**					
Erase Suspend	**75h**					
Erase Resume	**7Ah**					
Power-down	**B9h**					
Continuous Read Mode Reset (4)	**FFh**	FFh				

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "()" indicate data being read from the device on the DO pin.

2. The Status Register contents will repeat continuously until /CS terminates the instruction.

3. Quad Page Program Input Data:
   IO0 = (D4, D0, ……)
   IO1 = (D5, D1, ……)
   IO2 = (D6, D2, ……)
   IO3 = (D7, D3, ……)

4. This instruction is recommended when using the Dual or Quad "Continuous Read Mode" feature. See section 11.2.32 for more information.

11.2.3 Instruction Set Table 2 (Read Instructions)

INSTRUCTION NAME	BYTE 1 (CODE)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Read Data	**03h**	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Fast Read Dual Output	**3Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0, …)(1)
Fast Read Dual I/O	**BBh**	A23-A8(2)	A7-A0, M7-M0(2)	(D7-D0, …)(1)		
Fast Read Quad Output	**6Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0, …)(3)
Fast Read Quad I/O	**EBh**	A23-A0, M7-M0(4)	(x,x,x,x, D7-D0, …)(5)	(D7-D0, …)(3)		
Word Read Quad I/O(7)	**E7h**	A23-A0, M7-M0(4)	(x,x, D7-D0, …)(6)	(D7-D0, …)(3)		
Octal Word Read Quad I/O(8)	**E3h**	A23-A0, M7-M0(4)	(D7-D0, …)(3)			

Notes:

1. Dual Output data
   IO0 = (D6, D4, D2, D0)
   IO1 = (D7, D5, D3, D1)

2. Dual Input Address
   IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
   IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1

3. Quad Output Data
   IO0 = (D4, D0, …..)
   IO1 = (D5, D1, …..)
   IO2 = (D6, D2, …..)
   IO3 = (D7, D3, …..)

4. Quad Input Address
   IO0 = A20, A16, A12, A8, A4, A0, M4, M0
   IO1 = A21, A17, A13, A9, A5, A1, M5, M1
   IO2 = A22, A18, A14, A10, A6, A2, M6, M2
   IO3 = A23, A19, A15, A11, A7, A3, M7, M3

5. Fast Read Quad I/O Data
   IO0 = (x, x, x, x, D4, D0, …..)
   IO1 = (x, x, x, x, D5, D1, …..)
   IO2 = (x, x, x, x, D6, D2, …..)
   IO3 = (x, x, x, x, D7, D3, …..)

6. Word Read Quad I/O Data
   IO0 = (x, x, D4, D0, …..)
   IO1 = (x, x, D5, D1, …..)
   IO2 = (x, x, D6, D2, …..)
   IO3 = (x, x, D7, D3, …..)

7. The lowest address bit must be 0. (A0 = 0)

8. The lowest 4 address bits must be 0. (A0, A1, A2, A3 = 0)

11.2.4 Instruction Set Table 3 (ID, Security Instructions)

INSTRUCTION NAME	BYTE 1 (CODE)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Release Power down / Device ID	**ABh**	dummy	dummy	dummy	(ID7-ID0)(1)	
Manufacturer/ Device ID(2)	**90h**	dummy	dummy	00h	(MF7-MF0)	(ID7-ID0)
Manufacturer/Device ID by Dual I/O	**92h**	A23-A8	A7-A0, M[7:0]	(MF[7:0], ID[7:0])		
Manufacture/Device ID by Quad I/O	**94h**	A23-A0, M[7:0]	xxxx, (MF[7:0], ID[7:0])	(MF[7:0], ID[7:0], …)		
JEDEC ID	**9Fh**	(MF7-MF0) Manufacturer	(ID15-ID8) Memory Type	(ID7-ID0) Capacity		
Read Unique ID	**4Bh**	dummy	dummy	dummy	dummy	(ID63-ID0)

Notes:

1. The Device ID will repeat continuously until /CS terminates the instruction.
2. See Manufacturer and Device Identification table for Device ID information.

11.2.5 Write Enable (06h)

The Write Enable instruction (Figure 4) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

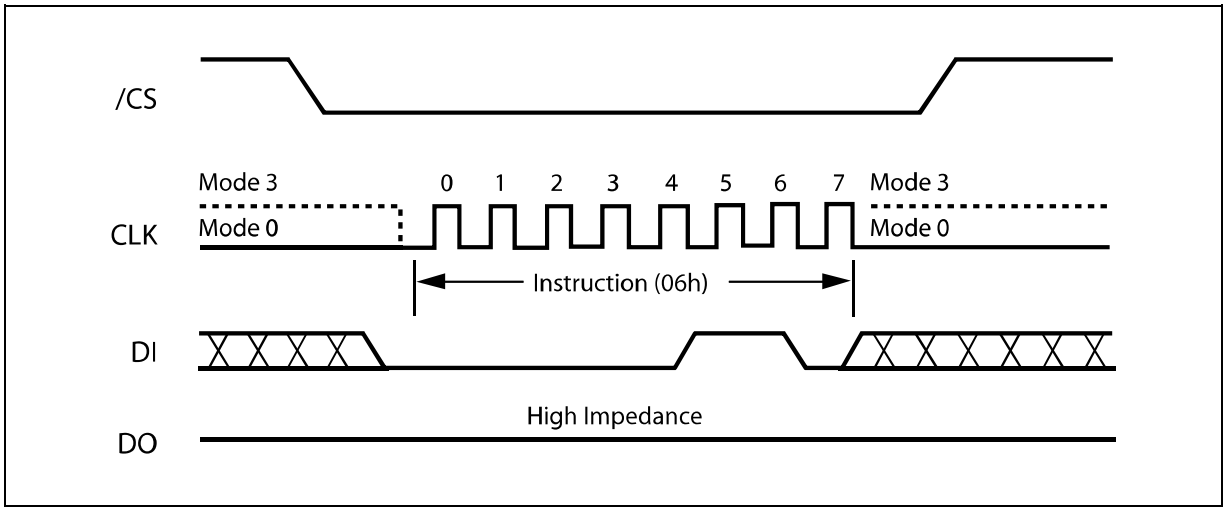

Figure 4. Write Enable Instruction Sequence Diagram

11.2.6 Write Disable (04h)

The Write Disable instruction (Figure 5) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase instructions.

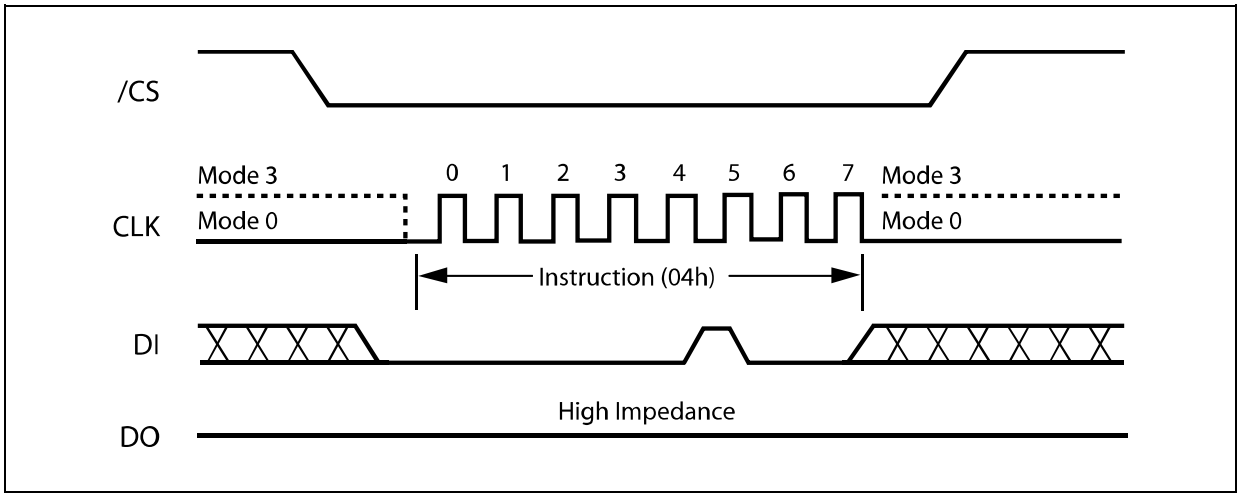

Figure 5. Write Disable Instruction Sequence Diagram

11.2.7 Read Status Register-1 (05h) and Read Status Register-2 (35h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving /CS low and shifting the instruction code “05h” for Status Register-1 and “35h” for Status Register-2 into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in figure 6. The Status Register bits are shown in figure 3a and 3b and include the BUSY, WEL, BP2-BP0, TB, SEC, SRP0, SRP1, QE and SUS bits (see description of the Status Register earlier in this datasheet).

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 6. The instruction is completed by driving /CS high.

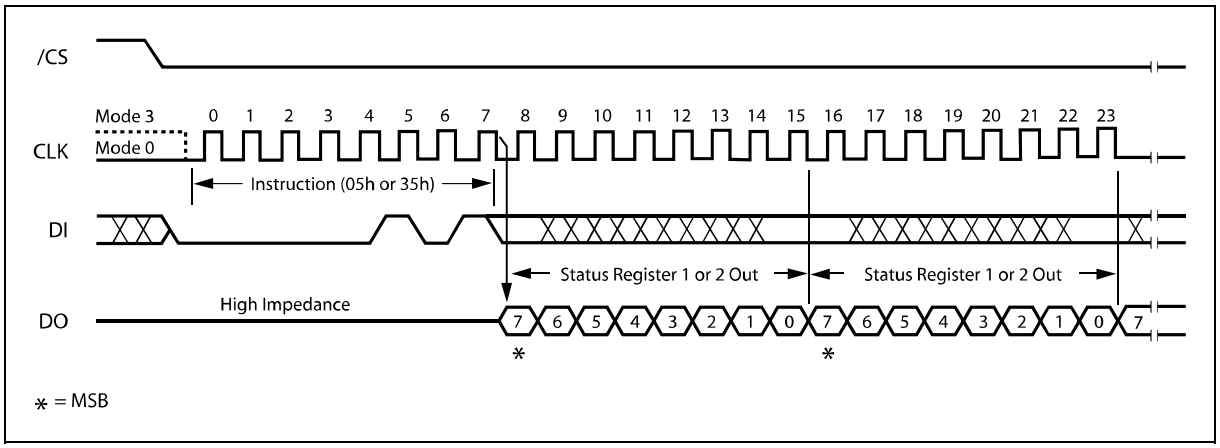

Figure 6. Read Status Register Instruction Sequence Diagram

11.2.8 Write Status Register (01h)

The Write Status Register instruction allows the Status Register to be written. A Write Enable instruction must previously have been executed for the device to accept the Write Status Register Instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code “01h”, and then writing the status register data byte as illustrated in figure 7. The Status Register bits are shown in figure 3 and described earlier in this datasheet.

Only non-volatile Status Register bits SRP0, SEC, TB, BP2, BP1, BP0 (bits 7, 5, 4, 3, 2 of Status Register-1) and QE, SRP1(bits 9 and 8 of Status Register-2) can be written to. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction.

The /CS pin must be driven high after the eighth or sixteenth bit of data that is clocked in. If this is not done the Write Status Register instruction will not be executed. If /CS is driven high after the eighth clock (compatible with the 25X series) the QE and SRP1 bits will be cleared to 0. After /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of tW (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

The Write Status Register instruction allows the Block Protect bits (SEC, TB, BP2, BP1 and BP0) to be set for protecting all, a portion, or none of the memory from erase and program instructions. Protected areas become read-only (see Status Register Memory Protection table and description). The Write Status Register instruction also allows the Status Register Protect bits (SRP0, SRP1) to be set. Those bits are used in conjunction with the Write Protect (/WP) pin, Lock out or OTP features to disable writes to the status register. Please refer to 11.1.6 for detailed descriptions regarding Status Register protection methods. Factory default for all status Register bits are 0.

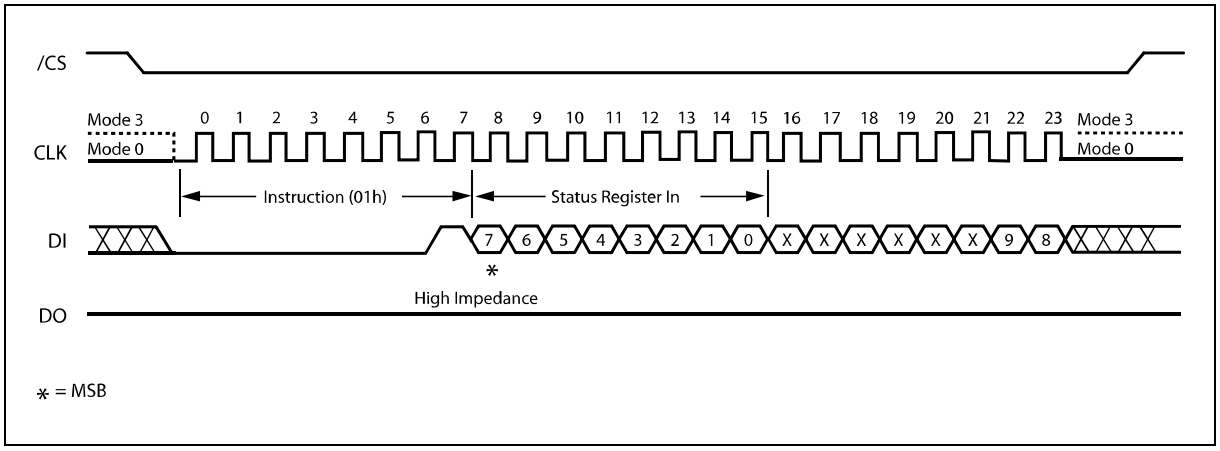

Figure 7. Write Status Register Instruction Sequence Diagram

11.2.9 Read Data (03h)

The Read Data instruction allows one more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high.

The Read Data instruction sequence is shown in figure 8. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (see AC Electrical Characteristics).

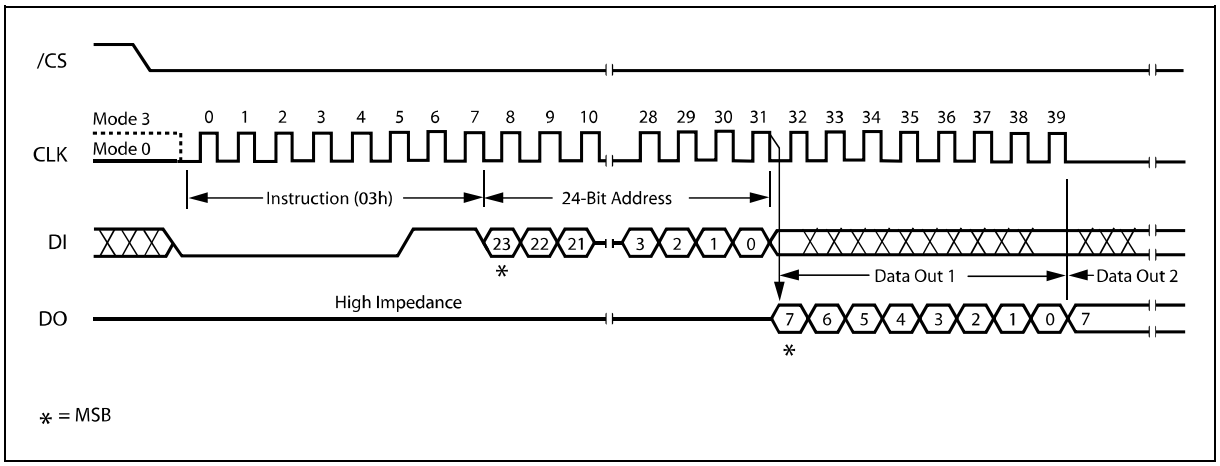

Figure 8. Read Data Instruction Sequence Diagram

11.2.10 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in figure 9. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DO pin is a "don't care".

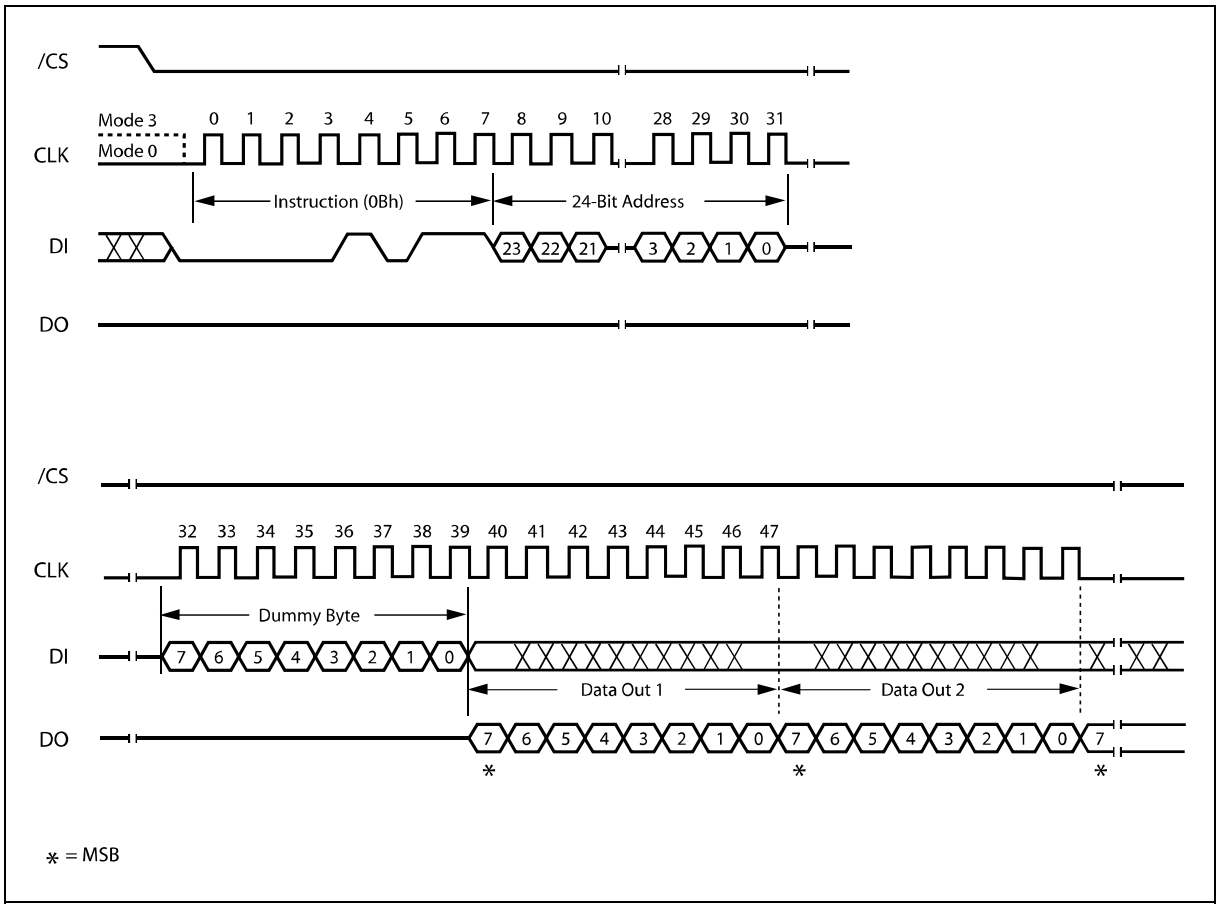

Figure 9. Fast Read Instruction Sequence Diagram