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W25Q256JV

3V 256M-BIT
SERIAL FLASH MEMORY WITH
DUAL/QUAD SPI

Publication Release Date: August 03, 2017
Revision G

winbond

Table of Contents

1. GENERAL DESCRIPTIONS

The W25Q256JV (256M-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25Q series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 2.7V to 3.6V power supply with current consumption as low as 1µA for power-down. All devices are offered in space-saving packages.

The W25Q256JV array is organized into 131,072 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The W25Q256JV has 8,192 erasable sectors and 512 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage.

The W25Q256JV supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2, and I/O3. SPI clock frequencies of W25Q256JV of up to 133MHz are supported allowing equivalent clock rates of 266MHz (133MHz x 2) for Dual I/O and 532MHz (133MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories.

Additionally, the device supports JEDEC standard manufacturer and device ID and SFDP Register, a 64-bit Unique Serial Number and three 256-bytes Security Registers.

2. FEATURES

- **New Family of SpiFlash Memories**
  - W25Q256JV: 256M-bit / 32M-byte
  - Standard SPI: CLK, /CS, DI, DO
  - Dual SPI: CLK, /CS, IO_0, IO_1,
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - 3 or 4-Byte Addressing Mode
  - Software & Hardware Reset(1)
- **Highest Performance Serial Flash**
  - 133MHz Standard/Dual/Quad SPI clocks
  - 266/532MHz equivalent Dual/Quad SPI
  - 66MB/S continuous data transfer rate
  - Min. 100K Program-Erase cycles per sector
  - More than 20-year data retention
- **Efficient "Continuous Read"**
  - Quad Peripheral Interface
  - Allows true XIP (execute in place) operation
  - Outperforms X16 Parallel Flash
- **Low Power, Wide Temperature Range**
  - Single 2.7 to 3.6V supply
  - <1µA Power-down (typ.)
  - -40°C to +85°C operating range
- **Flexible Architecture with 4KB sectors**
  - Uniform Sector/Block Erase (4K/32K/64K-Byte)
  - Program 1 to 256 byte per programmable page
  - Erase/Program Suspend & Resume
- **Advanced Security Features**
  - Software and Hardware Write-Protect
  - Power Supply Lock-Down
  - Special OTP protection
  - Top/Bottom, Complement array protection
  - Individual Block/Sector array protection
  - 64-Bit Unique ID for each device
  - Discoverable Parameters (SFDP) Register
  - 3X256-Bytes Security Registers with OTP locks
  - Volatile & Non-volatile Status Register Bits
- **Space Efficient Packaging(2)**
  - 8-pad WSON 8x6-mm
  - 16-pin SOIC 300-mil (additional /Reset pin)
  - 24-ball TFBGA 8x6-mm(additional /Reset pin)
  - Contact Winbond for KGD and other options

Note: 1. Hardware /RESET pin is only available on TFBGA or SOIC16 packages
2. Please contact Winbond for other packages.

3. PACKAGE TYPES AND PIN CONFIGURATIONS

W25Q256JV is offered in an 8-pad WSON 8x6-mm (package code E), a 16-pin SOIC 300-mil (package code F) and two 24-ball 8x6-mm TFBGA (package code B & C) packages as shown in Figure 1a-c respectively. Package diagrams and dimensions are illustrated at the end of this datasheet.

3.1 Pad Configuration WSON 8x6-mm

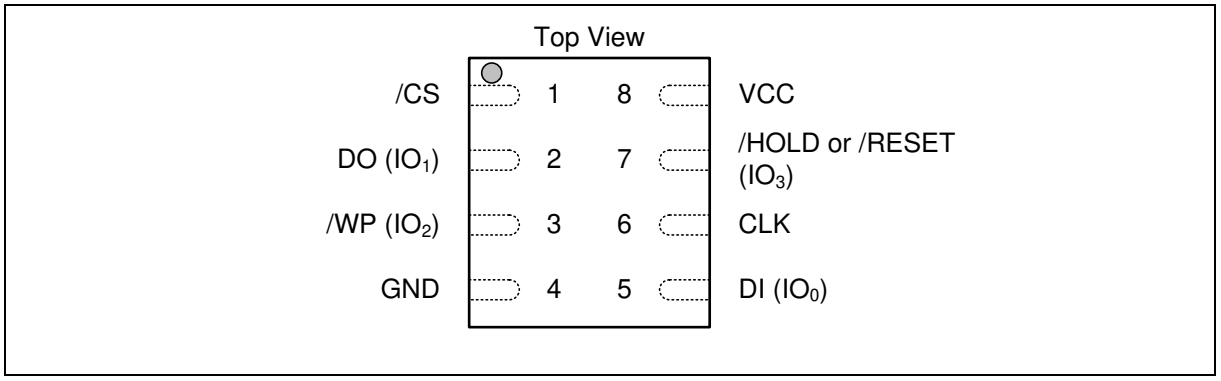

Figure 1a. W25Q256JV Pad Assignments, 8-pad WSON 8x6-mm (Package Code E)

3.2 Pad Description WSON 8x6-mm

PAD NO.	PAD NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	/HOLD or /RESET (IO3)	I/O	Hold or Reset Input (Data Input Output 3)(2)
8	VCC		Power Supply

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /HOLD (or /RESET) function is only available for Standard/Dual SPI.

3.3 Pin Configuration SOIC 300-mil

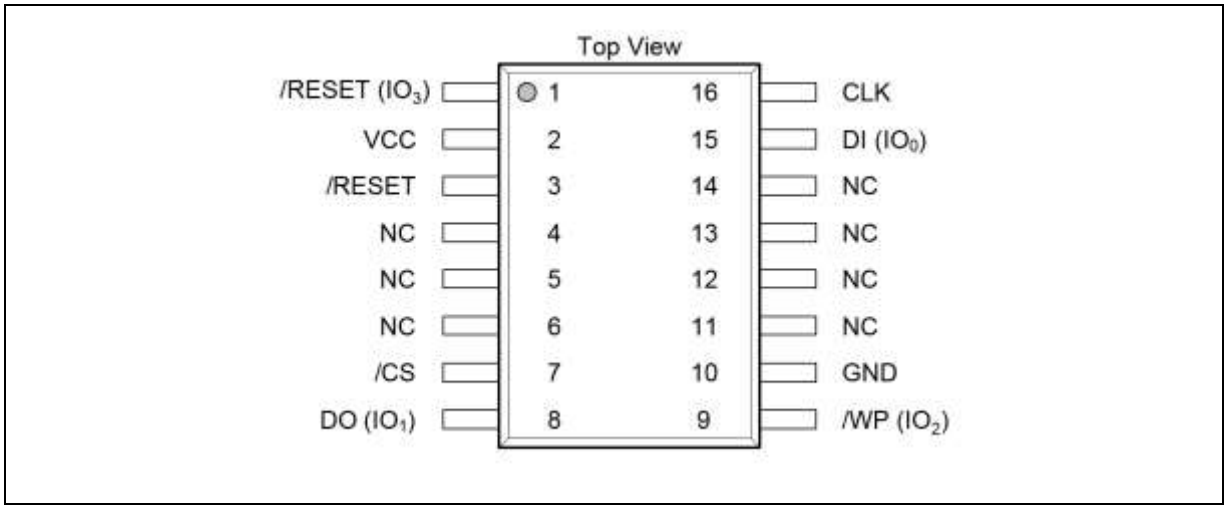

Figure 1b. W25Q256JV Pin Assignments, 16-pin SOIC 300-mil (Package Code F)

3.4 Pin Description SOIC 300-mil

PIN NO.	PIN NAME	I/O	FUNCTION
1	/HOLD or /RESET (IO3)	I/O	Hold or Reset Input (Data Input Output 3)(2)
2	VCC		Power Supply
3	/RESET	I	Reset Input(3)
4	N/C		No Connect
5	N/C		No Connect
6	N/C		No Connect
7	/CS	I	Chip Select Input
8	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
9	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
10	GND		Ground
11	N/C		No Connect
12	N/C		No Connect
13	N/C		No Connect
14	N/C		No Connect
15	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
16	CLK	I	Serial Clock Input

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions.
2. IO0 – IO3 are used for Quad SPI instructions, /HOLD (or /RESET) function is only available for Standard/Dual SPI.
3. The /RESET pin is a dedicated hardware reset pin regardless of device settings or operation states. If the hardware reset function is not used, this pin can be left floating or connected to VCC in the system.

3.5 Ball Configuration TFBGA 8x6-mm (5x5 or 6x4 Ball Array)

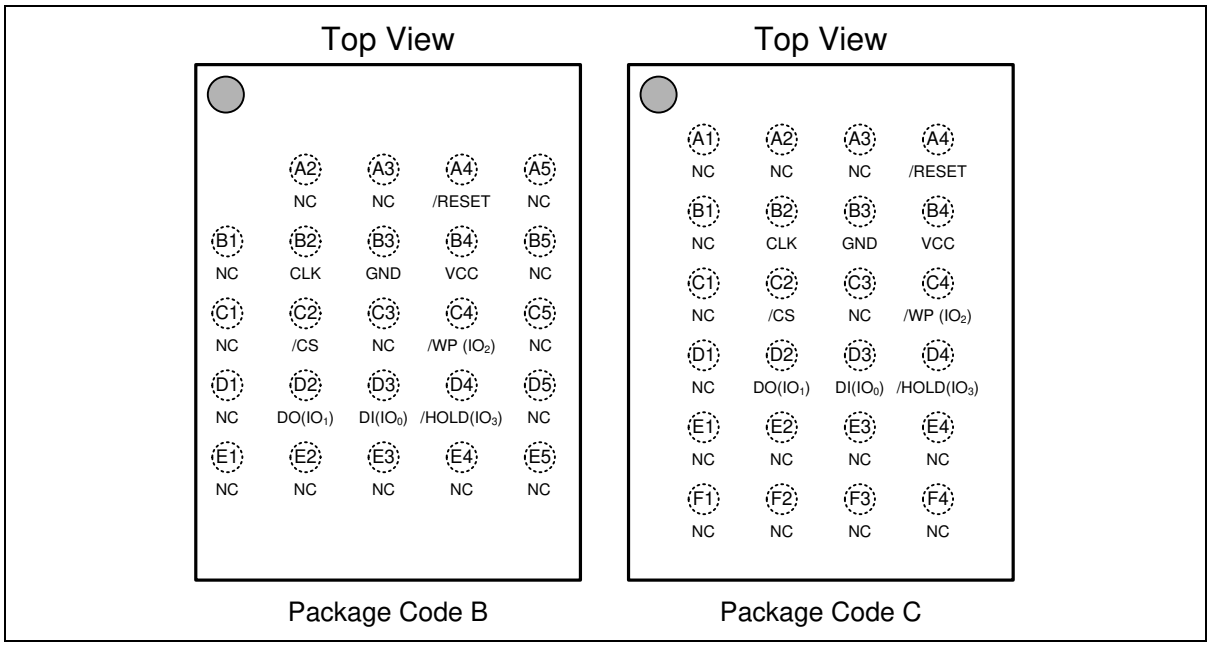

Figure 1c. W25Q256JV Ball Assignments, 24-ball TFBGA 6x8-mm (Package Code B & C)

3.6 Ball Description TFBGA 8x6-mm

BALL NO.	PIN NAME	I/O	FUNCTION
A4	/RESET	I	Reset Input(3)
B2	CLK	I	Serial Clock Input
B3	GND		Ground
B4	VCC		Power Supply
C2	/CS	I	Chip Select Input
C4	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
D2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
D3	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
D4	/HOLD (IO3)	I/O	Hold or Reset Input (Data Input Output 3)(2)
Multiple	NC		No Connect

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /HOLD (or /RESET) function is only available for Standard/Dual SPI.
3. The /RESET pin is a dedicated hardware reset pin regardless of device settings or operation states. If the hardware reset function is not used, this pin can be left floating or connected to VCC in the system

4. PIN DESCRIPTIONS

4.1 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down (see “Write Protection” and Figure 58). If needed a pull-up resistor on the /CS pin can be used to accomplish this.

4.2 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The W25Q256JV supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and the /HOLD pin becomes IO3.

4.3 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The /WP pin is active low.

4.4 HOLD (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /HOLD pin function is not available since this pin is used for IO3. See Figure 1a-c for the pin configuration of Quad I/O operation.

4.5 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

4.6 Reset (/RESET)(1)

A dedicated hardware /RESET pin is available on SOIC-16 and TFBGA packages. When it’s driven low for a minimum period of ~1µS, this device will terminate any external or internal operations and return to its power-on state.

Note: Hardware /RESET pin is available on SOIC-16 or TFBGA; please contact Winbond for this package.

5. BLOCK DIAGRAM

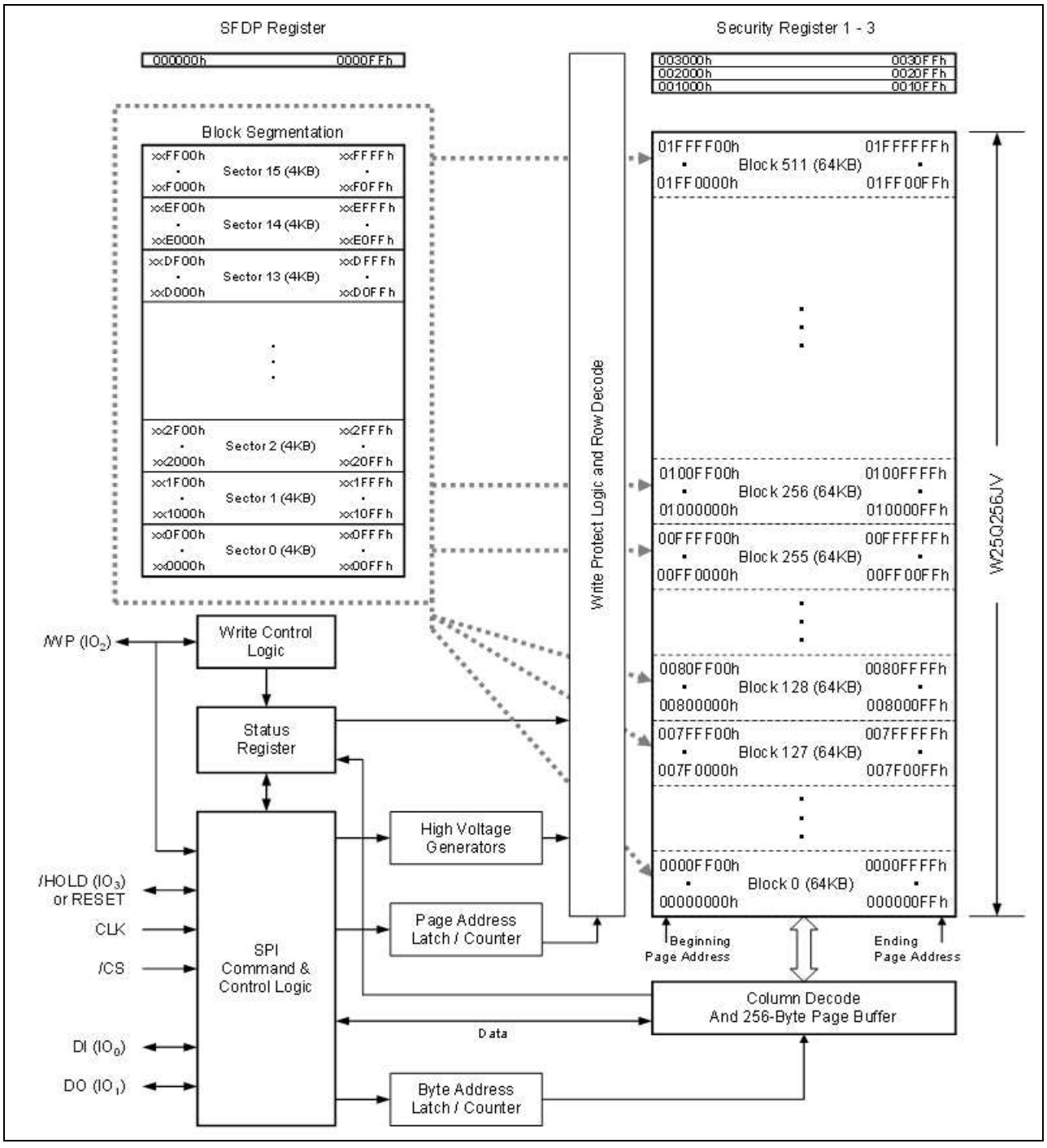

Figure 2. W25Q256JV Serial Flash Memory Block Diagram

6. FUNCTIONAL DESCRIPTIONS

6.1 SPI Operations

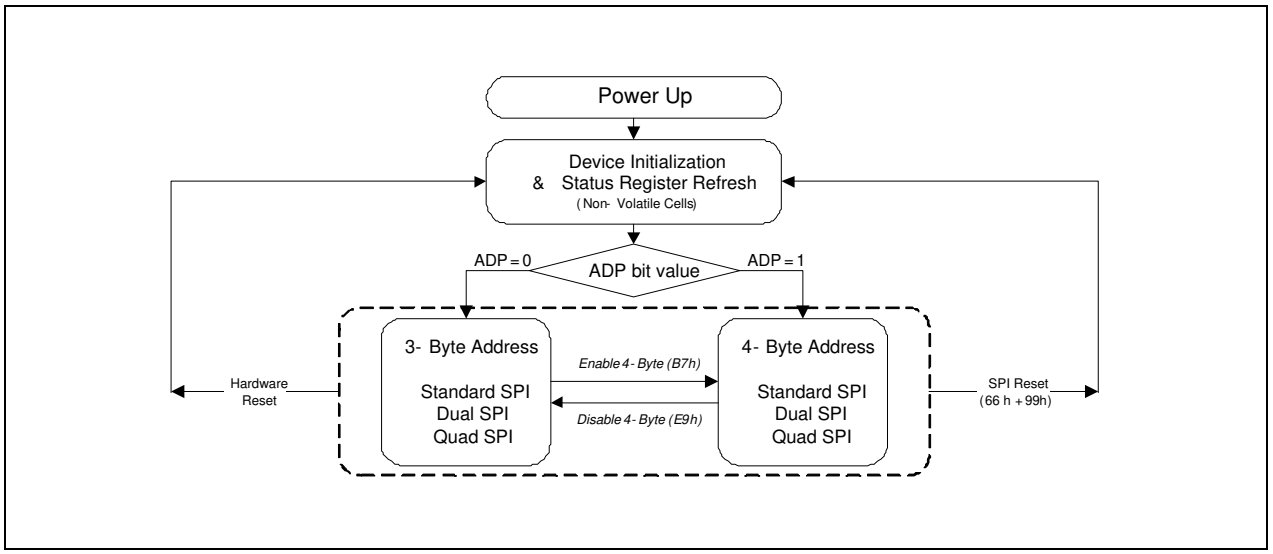

Figure 3. W25Q256JV Serial Flash Memory Operation Diagram

6.1.1 Standard SPI Instructions

The W25Q256JV is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

6.1.2 Dual SPI Instructions

The W25Q256JV supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

6.1.3 Quad SPI Instructions

The W25Q256JV supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)”, and “Fast Read Quad I/O (EBh)”. These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

6.1.4 3-Byte / 4-Byte Address Modes

The W25Q256JV provides two Address Modes that can be used to specify any byte of data in the memory array. The 3-Byte Address Mode is backward compatible to older generations of serial flash memory that only support up to 128M-bit data. To address the 256M-bit or more data in 3-Byte Address Mode, Extended Address Register must be used in addition to the 3-Byte addresses.

4-Byte Address Mode is designed to support Serial Flash Memory devices from 256M-bit to 32G-bit. The extended Address Register is not necessary when the 4-Byte Address Mode is enabled.

Upon power up, the W25Q256JV can operate in either 3-Byte Address Mode or 4-Byte Address Mode, depending on the Non-Volatile Status Register Bit ADP (S17) setting. If ADP=0, the device will operate in 3-Byte Address Mode; if ADP=1, the device will operate in 4-Byte Address Mode. The factory default value for ADP is 0.

To switch between the 3-Byte or 4-Byte Address Modes, “Enter 4-Byte Mode (B7h)” or “Exit 4-Byte Mode (E9h)” instructions must be used. The current address mode is indicated by the Status Register Bit ADS (S16).

W25Q256JV also supports a set of basic SPI instructions which requires dedicated 4-Byte address regardless the device Address Mode setting. Please refer to Instruction Set Table 2 for details.

6.1.5 Software Reset & Hardware /RESET pin

The W25Q256JV can be reset to the initial power-on state by a software Reset sequence in SPI mode. This sequence must include two consecutive commands: Enable Reset (66h) & Reset (99h). If the command sequence is successfully accepted, the device will take approximately 30uS (t_{RST}) to reset. No command will be accepted during the reset period.

For the SOIC-16 and TFBGA package, W25Q256JV provides a dedicated /RESET pin. Drive the /RESET pin low for a minimum period of ~1us (tRESET*) will reset the device to its initial power-on state.

Hardware /RESET pin has the highest priority among all the input signals. Drive /RESET low for a minimum period of ~1us (tRESET*) will interrupt any on-going external/internal operations, regardless the status of other SPI signals (/CS, CLK, IOs).

Note:

1. While a faster /RESET pulse (as short as a few hundred nanoseconds) will often reset the device, a 1us minimum pulse is recommended to ensure reliable operation.
2. There is an internal pull-up resistor for the dedicated /RESET pin on the SOIC-16 package. If the reset function is not used, this pin can be left floating in the system.

6.2 Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the W25Q256JV provides several means to protect the data from inadvertent writes.

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (/WP pin) write protection using Status Registers
- Additional Individual Block/Sector Locks for array protection
- Write Protection using Power-down instruction
- Lock Down write protection for Status Register until the next power-up
- One Time Program (OTP) write protection for array and Security Registers using Status Register*

  * Note: This feature is available upon special order. Please contact Winbond for details.

Upon power-up or at power-down, the W25Q256JV will maintain a reset condition while VCC is below the threshold value of V_{WI}, (See Power-up Timing and Voltage Levels and Figure 43). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds V_{WI}, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached, and it must also track the VCC supply level at power-down to prevent adverse command sequence. If needed, a pull-up resistor on /CS pin can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP, SRL) and Block Protect (CMP, TB, BP[3:0]) bits. These settings allow a portion or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

The W25Q256JV also provides another Write Protect method using the Individual Block Locks. Each 64KB block (except the top and bottom blocks, total of 510 blocks) and each 4KB sector within the top/bottom blocks (total of 32 sectors) are equipped with an Individual Block Lock bit. When the lock bit is 0, the corresponding sector or block can be erased or programmed; when the lock bit is set to 1, Erase or Program commands issued to the corresponding sector or block will be ignored. When the device is powered on, all Individual Block Lock bits will be 1, so the entire memory array is protected from Erase/Program. An “Individual Block Unlock (39h)” instruction must be issued to unlock any specific sector or block.

The WPS bit in Status Register-3 is used to decide which Write Protect scheme should be used. When WPS=0 (factory default), the device will only utilize CMP, TB, BP[3:0] bits to protect specific areas of the array; when WPS=1, the device will utilize the Individual Block Locks for write protection.

7. STATUS AND CONFIGURATION REGISTERS

Three Status and Configuration Registers are provided for W25Q256JV. The Read Status Register-1/2/3 instructions can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status, Erase/Program Suspend status, output driver strength, power-up and current Address Mode. The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting, Security Register OTP locks functions, output driver strength and power-up Address Mode. Write access to the Status Register is controlled by the state of the non-volatile Status Register Lock bits (SRL), and the Write Enable instruction.

7.1 Status Registers

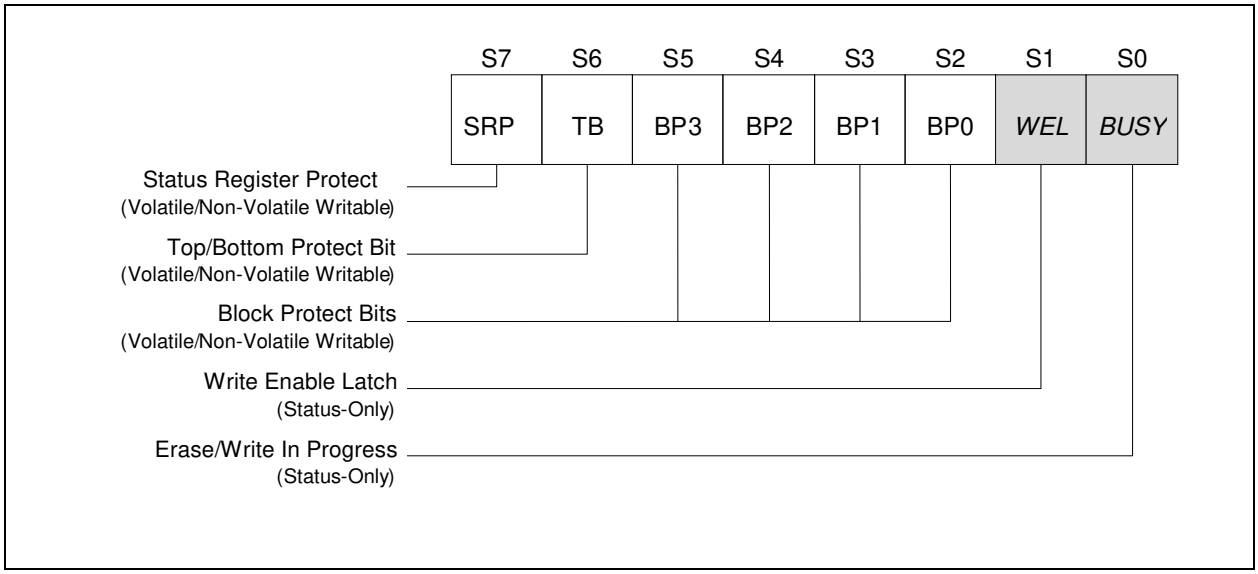

Figure 4a. Status Register-1

7.1.1 Erase/Write In Progress (BUSY) – *Status Only*

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Register instruction. During this time the device will ignore further instructions except for the Read Status Register and Erase/Program Suspend instruction (see tW, tPP, tSE, tBE, and tCE in AC Characteristics). When the program, erase or write status/security register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

7.1.2 Write Enable Latch (WEL) – *Status Only*

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Register and Program Security Register.

7.1.3 Block Protect Bits (BP3, BP2, BP1, BP0) – *Volatile/Non-Volatile Writable*

The Block Protect Bits (BP3, BP2, BP1, BP0) are non-volatile read/write bits in the status register (S5, S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see tw in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

7.1.4 Top/Bottom Block Protect (TB) – *Volatile/Non-Volatile Writable*

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP3, BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the WEL bits.

7.1.5 Complement Protect (CMP) – *Volatile/Non-Volatile Writable*

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with TB, BP3, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by TB, BP3, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 64KB block can be protected while the rest of the array is not; when CMP=1, the top 64KB block will become unprotected while the rest of the array become read-only. Please refer to the Status Register Memory Protection table for details. The default setting is CMP=0.

7.1.1 Status Register Protect (SRP, SRL) – *Volatile/Non-Volatile Writable*

Three Status and Configuration Registers are provided for W25Q256JV. The Read Status Register-1/2/3 instructions can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status, Erase/Program Suspend status, and output driver strength, The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting, Security Register OTP locks, output driver. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP, SRL), the Write Enable instruction, and during Standard/Dual SPI operations, the /WP pin.

SRL	SRP	/WP	Status Register	Description
0	0	X	Software Protection	/WP pin has no control. The Status register can be written to after a Write Enable instruction, WEL=1. [Factory Default]
0	1	0	Hardware Protected	When /WP pin is low the Status Register locked and cannot be written to.
0	1	1	Hardware Unprotected	When /WP pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	X	X	Power Supply Lock-Down	Status Register is protected and cannot be written to again until the next power-down, power-up cycle.(1)
1	X	X	One Time Program(2)	Status Register is permanently protected and cannot be written to. (**enabled by adding prefix command AAh, 55h)**

1. When SRL =1, a power-down, power-up cycle will change SRL =0 state.
2. Please contact Winbond for details regarding the special instruction sequence.

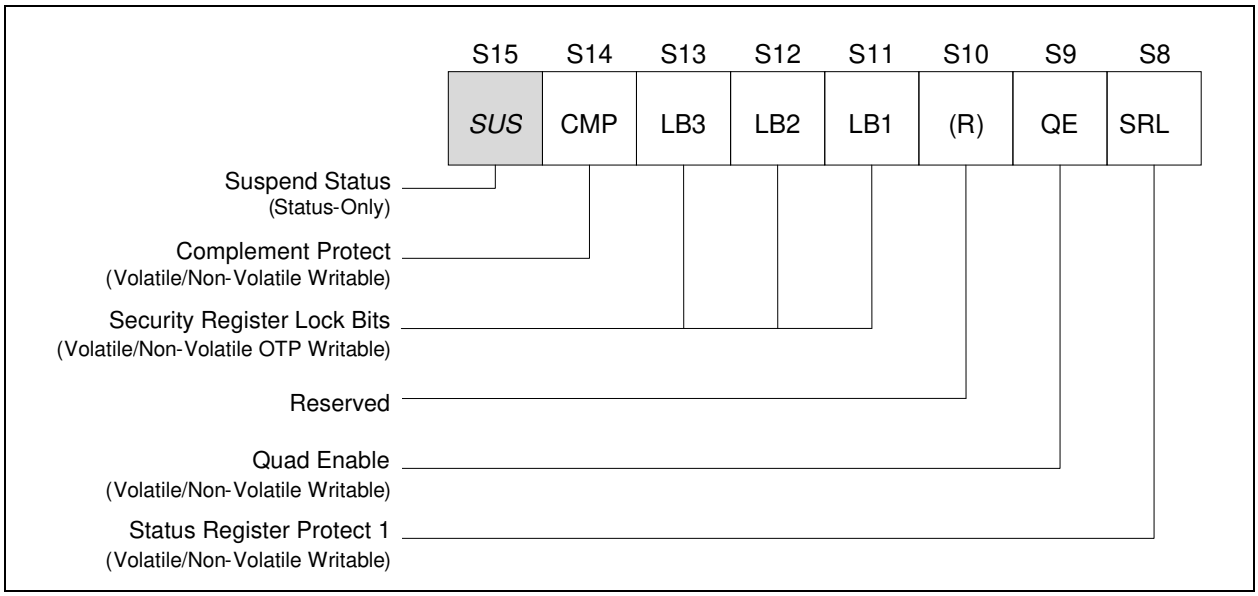

Figure 4b. Status Register-2

7.1.2 Erase/Program Suspend Status (SUS) – *Status Only*

The Suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing a Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power-down, power-up cycle.

7.1.3 Security Register Lock Bits (LB3, LB2, LB1) – *Volatile/Non-Volatile OTP Writable*

The Security Register Lock Bits (LB3, LB2, LB1) are non-volatile One Time Program (OTP) bits in Status Register (S13, S12, S11) that provide the write protect control and status to the Security Registers. The default state of LB3-1 is 0, Security Registers are unlocked. LB3-1 can be set to 1 individually using the Write Status Register instruction. LB3-1 are One Time Programmable (OTP), once it's set to 1, the corresponding 256-Byte Security Register will become read-only permanently.

7.1.4 Quad Enable (QE) – *Volatile/Non-Volatile Writable*

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that enables Quad SPI operation. When the QE bit is set to a 0 state (factory default for part numbers with ordering options "IM"), the /HOLD are enabled, the device operates in Standard/Dual SPI modes. When the QE bit is set to a 1 (factory fixed default for part numbers with ordering options "IQ"), the Quad IO2 and IO3 pins are enabled, and /HOLD function is disabled, the device operates in Standard/Dual/Quad SPI modes.

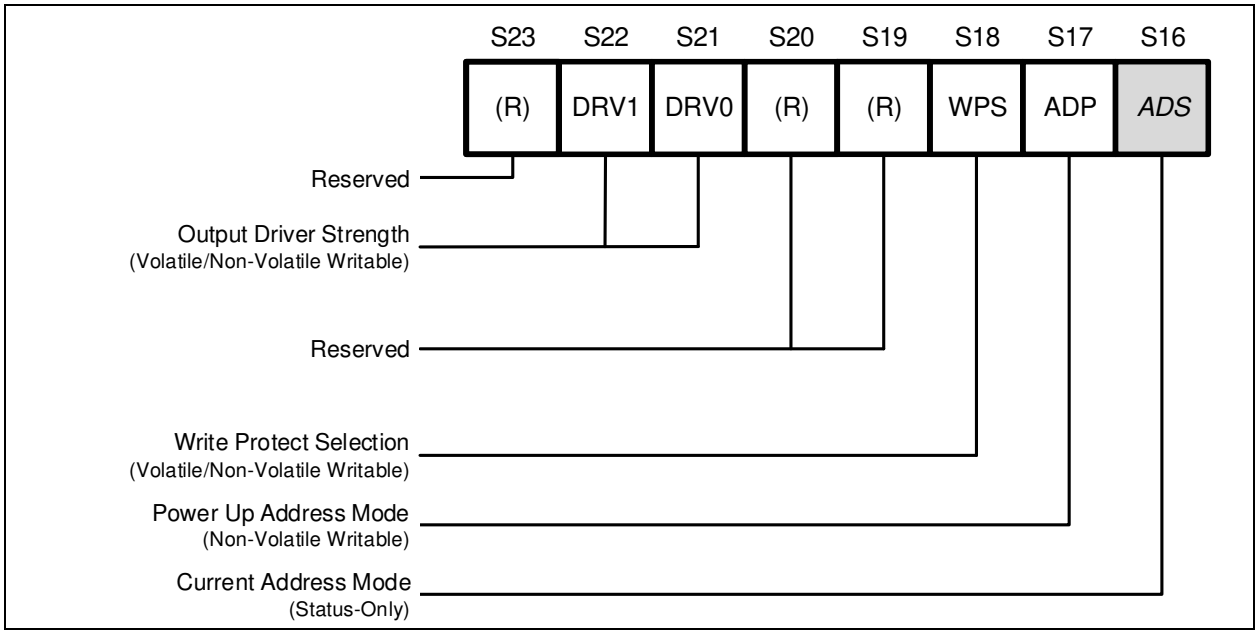

Figure 4c. Status Register-3

7.1.5 Current Address Mode (ADS) – *Status Only*

The Current Address Mode bit is a read only bit in the Status Register-3 that indicates which address mode the device is currently operating in. When ADS=0, the device is in the 3-Byte Address Mode, when ADS=1, the device is in the 4-Byte Address Mode.

7.1.6 Power-Up Address Mode (ADP) – *Non-Volatile Writable*

The ADP bit is a non-volatile bit that determines the initial address mode when the device is powered on or reset. This bit is only used during the power on or device reset initialization period, and it is only writable by the non-volatile Write Status sequence (06h + 11h). When ADP=0 (factory default), the device will power up into 3-Byte Address Mode, the Extended Address Register must be used to access memory regions beyond 128Mb. When ADP=1, the device will power up into 4-Byte Address Mode directly.

7.1.7 Write Protect Selection (WPS) – *Volatile/Non-Volatile Writable*

The WPS bit is used to select which Write Protect scheme should be used. When WPS=0, the device will use the combination of CMP, TB, BP[3:0] bits to protect a specific area of the memory array. When WPS=1, the device will utilize the Individual Block Locks to protect any individual sector or blocks. The default value for all Individual Block Lock bits is 1 upon device power on or after reset.

7.1.8 Output Driver Strength (DRV1, DRV0) – *Volatile/Non-Volatile Writable*

The DRV1 & DRV0 bits are used to determine the output driver strength for the Read operations.

DRV1, DRV0	Driver Strength
0, 0	100%
0, 1	75%
1, 0	50%
1, 1	25% (default setting)

7.1.9 Reserved Bits – *Non Functional*

There are a few reserved Status Register bits that may be read out as a "0" or "1". It is recommended to ignore the values of those bits. During a "Write Status Register" instruction, the Reserved Bits can be written as "0", but there will not be any effects.

7.1.10 W25Q256JV Status Register Memory Protection (WPS = 0, CMP = 0)

STATUS REGISTER(1)					W25Q256JV (256M-BIT / 32M-BYTE) MEMORY PROTECTION(2)			
TB	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
X	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	511	01FF0000h - 01FFFFFFh	64KB	Upper 1/512
0	0	0	1	0	510 thru 511	01FE0000h - 01FFFFFFh	128KB	Upper 1/256
0	0	0	1	1	508 thru 511	01FC0000h - 01FFFFFFh	256KB	Upper 1/128
0	0	1	0	0	504 thru 511	01F80000h - 01FFFFFFh	512KB	Upper 1/64
0	0	1	0	1	496 thru 511	01F00000h - 01FFFFFFh	1MB	Upper 1/32
0	0	1	1	0	480 thru 511	01E00000h - 01FFFFFFh	2MB	Upper 1/16
0	0	1	1	1	448 thru 511	01C00000h - 01FFFFFFh	4MB	Upper 1/8
0	1	0	0	0	384 thru 511	01800000h - 01FFFFFFh	8MB	Upper 1/4
0	1	0	0	1	256 thru 511	01000000h - 01FFFFFFh	16MB	Upper 1/2
1	0	0	0	1	0	00000000h - 0000FFFFh	64KB	Lower 1/512
1	0	0	1	0	0 thru 1	00000000h - 0001FFFFh	128KB	Lower 1/256
1	0	0	1	1	0 thru 3	00000000h - 0003FFFFh	256KB	Lower 1/128
1	0	1	0	0	0 thru 7	00000000h - 0007FFFFh	512KB	Lower 1/64
1	0	1	0	1	0 thru 15	00000000h - 000FFFFFh	1MB	Lower 1/32
1	0	1	1	0	0 thru 31	00000000h - 001FFFFFh	2MB	Lower 1/16
1	0	1	1	1	0 thru 63	00000000h - 003FFFFFh	4MB	Lower 1/8
1	1	0	0	0	0 thru 127	00000000h - 007FFFFFh	8MB	Lower 1/4
1	1	0	0	1	0 thru 255	00000000h - 00FFFFFFh	16MB	Lower 1/2
X	1	1	0	X	0 thru 511	00000000h - 01FFFFFFh	32MB	ALL
X	1	X	1	X	0 thru 511	00000000h - 01FFFFFFh	32MB	ALL

Notes:
1. X = don't care
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

7.1.11 W25Q256JV Status Register Memory Protection (WPS = 0, CMP = 1)

STATUS REGISTER(1)					W25Q256JV (256M-BIT / 32M-BYTE) MEMORY PROTECTION(2)			
TB	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
X	0	0	0	0	ALL	00000000h - 01FFFFFFh	ALL	ALL
0	0	0	0	1	0 thru 510	00000000h - 01FEFFFFh	32,704KB	Lower 511/512
0	0	0	1	0	0 thru 509	00000000h - 01FDFFFFh	32,640KB	Lower 255/256
0	0	0	1	1	0 thru 507	00000000h - 01FBFFFFh	32,512KB	Lower 127/128
0	0	1	0	0	0 thru 503	00000000h - 01F7FFFFh	32,256KB	Lower 63/64
0	0	1	0	1	0 thru 495	00000000h - 01EFFFFFh	31MB	Lower 31/32
0	0	1	1	0	0 thru 479	00000000h - 01DFFFFFh	30MB	Lower 15/16
0	0	1	1	1	0 thru 447	00000000h - 01BFFFFFh	28MB	Lower 7/8
0	1	0	0	0	0 thru 383	00000000h - 017FFFFFh	24MB	Lower 3/4
0	1	0	0	1	0 thru 255	00000000h - 00FFFFFFh	16MB	Lower 1/2
1	0	0	0	1	1 thru 511	00010000h - 01FFFFFFh	32,704KB	Upper 511/512
1	0	0	1	0	2 thru 511	00020000h - 01FFFFFFh	32,640KB	Upper 255/256
1	0	0	1	1	4 thru 511	00040000h - 01FFFFFFh	32,512KB	Upper 127/128
1	0	1	0	0	8 thru 511	00080000h - 01FFFFFFh	32,256KB	Upper 63/64
1	0	1	0	1	16 thru 511	00100000h - 01FFFFFFh	31MB	Upper 31/32
1	0	1	1	0	32 thru 511	00200000h - 01FFFFFFh	30MB	Upper 15/16
1	0	1	1	1	64 thru 511	00400000h - 01FFFFFFh	28MB	Upper 7/8
1	1	0	0	0	128 thru 511	00800000h - 01FFFFFFh	24MB	Upper 3/4
1	1	0	0	1	256 thru 511	01000000h - 01FFFFFFh	16MB	Upper 1/2
X	1	1	0	X	NONE	NONE	NONE	NONE
X	1	X	1	X	NONE	NONE	NONE	NONE

Notes:

1. X = don't care
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

7.1.12 W25Q256JV Individual Block Memory Protection (WPS=1)

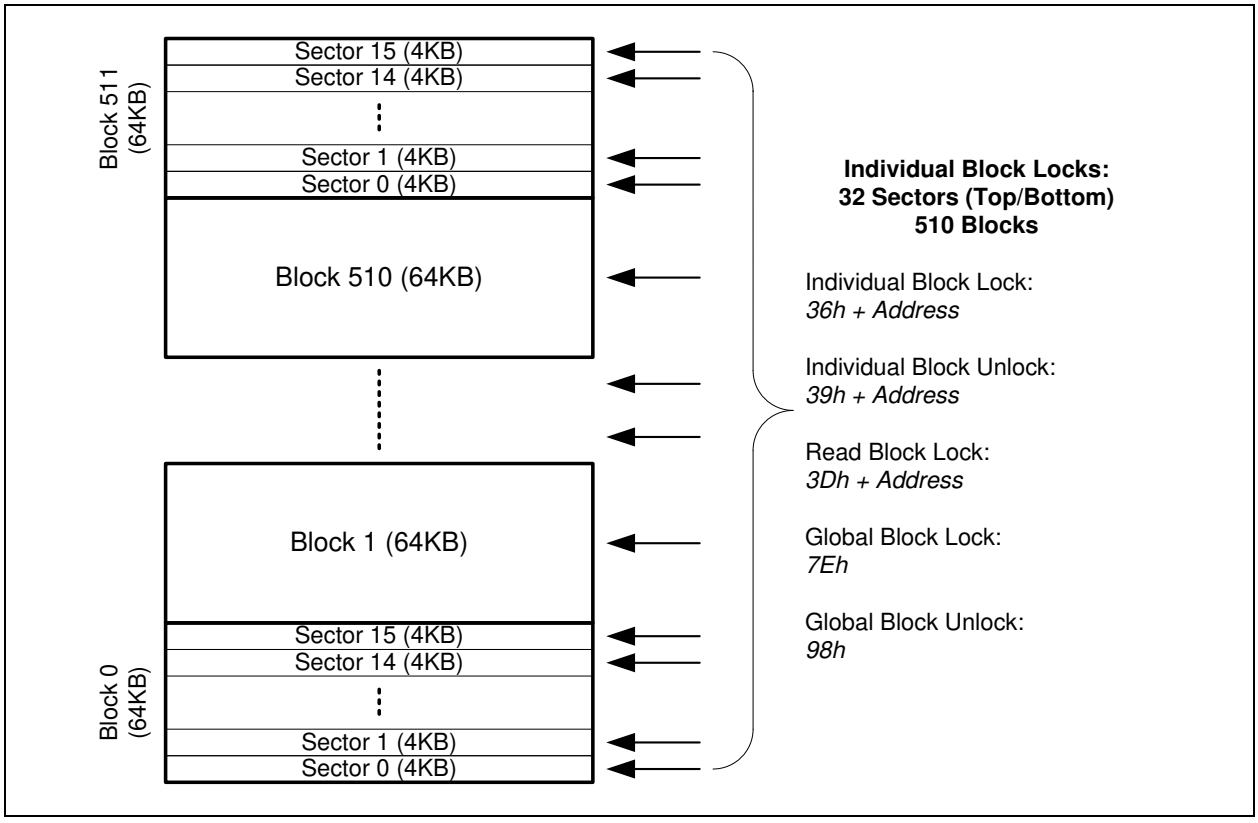

Figure 4d. Individual Block/Sector Locks

Notes:

1. Individual Block/Sector protection is only valid when WPS=1.
2. All individual block/sector lock bits are set to 1 by default after power up, all memory array is protected.

7.2 Extended Address Register – *Volatile Writable Only*

In addition to the Status Registers, W25Q256JV provides a volatile Extended Address Register which consists of the 4th byte of memory address. The Extended Address Register is used only when the device is operating in the 3-Byte Address Mode (ADS=0). The lower 128Mb memory array (00000000h – 00FFFFFFh) is selected when A24=0, all instructions with 3-Byte addresses will be executed within that region. When A24=1, the upper 128Mb memory array (01000000h – 01FFFFFFh) will be selected.

If the device powers up with ADP bit set to 1, or an "Enter 4-Byte Address Mode (B7h)" instruction is issued, the device will require 4-Byte address input for all address related instructions, and the Extended Address Register setting will be ignored. However, any command with 4-byte address input will replace the Extended Address Register Bits (A31-A24) with new settings.

Upon power up or after the execution of a Software/Hardware Reset, the Extended Address Register values will be cleared to 0.

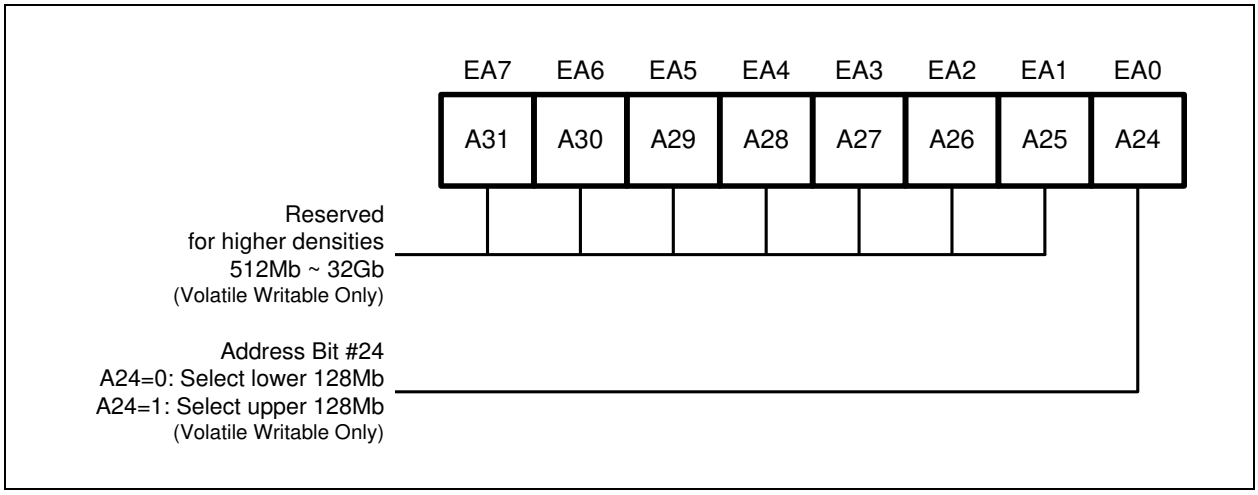

Figure 4e. Extended Address Register

8. INSTRUCTIONS

The Standard/Dual/Quad SPI instruction set of the W25Q256JV consists of 48 basic instructions that are fully controlled through the SPI bus (see Instruction Set Table1-4). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in Figures 5 through 57. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

8.1 Device ID and Instruction Set Tables

8.1.1 Manufacturer and Device Identification

MANUFACTURER ID	**(MF7 - MF0)**	
Winbond Serial Flash	EFh	
Device ID	**(ID7 - ID0)**	**(ID15 - ID0)**
Instruction	**ABh, 90h, 92h, 94h**	**9Fh**
W25Q256JV-IQ	18h	4019h
W25Q256JV-IM*	18h	7019h

Note: For DTR, QPI supporting, please refer to W25Q256JV DTR datasheet.