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W25Q32FV

3V 32M-BIT
SERIAL FLASH MEMORY WITH
DUAL/QUAD SPI & QPI

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Revision J

winbond

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1. GENERAL DESCRIPTIONS

The W25Q32FV (32M-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25Q series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 2.7V to 3.6V power supply with current consumption as low as 4mA active and 1µA for power-down. All devices are offered in space-saving packages.

The W25Q32FV array is organized into 16,384 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The W25Q32FV has 1,024 erasable sectors and 64 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See Figure 2.)

The W25Q32FV support the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI as well as 2-clocks instruction cycle Quad Peripheral Interface (QPI): Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz (104MHz x 2) for Dual I/O and 416MHz (104MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O and QPI instructions. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories. The Continuous Read Mode allows for efficient memory access with as few as 8-clocks of instruction-overhead to read a 24-bit address, allowing true XIP (execute in place) operation.

A Hold pin, Write Protect pin and programmable write protection, with top or bottom array control, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device ID and SFDP Register, a 64-bit Unique Serial Number and three 256-bytes Security Registers.

2. FEATURES

- **New Family of SpiFlash Memories**
  - W25Q32FV: 32M-bit / 4M-byte
  - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  - Dual SPI: CLK, /CS, IO_0, IO_1, /WP, /Hold
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - QPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - Software & Hardware Reset
- **Highest Performance Serial Flash**
  - 104MHz Single, Dual/Quad SPI clocks
  - 208/416MHz equivalent Dual/Quad SPI
  - 50MB/S continuous data transfer rate
  - More than 100,000 erase/program cycles
  - More than 20-year data retention
- **Efficient "Continuous Read" and QPI Mode**
  - Continuous Read with 8/16/32/64-Byte Wrap
  - As few as 8 clocks to address memory
  - Quad Peripheral Interface (QPI) reduces instruction overhead
  - Allows true XIP (execute in place) operation
  - Outperforms X16 Parallel Flash
- **Low Power, Wide Temperature Range**
  - Single 2.7 to 3.6V supply
  - 4mA active current, <1µA Power-down (typ.)
  - -40°C to +85°C operating range
- **Flexible Architecture with 4KB sectors**
  - Uniform Sector/Block Erase (4K/32K/64K-Byte)
  - Program 1 to 256 byte per programmable page
  - Erase/Program Suspend & Resume
- **Advanced Security Features**
  - Software and Hardware Write-Protect
  - Power Supply Lock-Down and OTP protection
  - Top/Bottom, Complement array protection
  - Individual Block/Sector array protection
  - 64-Bit Unique ID for each device
  - Discoverable Parameters (SFDP) Register
  - 3X256-Bytes Security Registers with OTP locks
  - Volatile & Non-volatile Status Register Bits
- **Space Efficient Packaging**
  - 8-pin SOIC 208-mil / VSOP 208-mil
  - 8-pad WSON 6x5-mm / 8x6-mm
  - 16-pin SOIC 300-mil (additional /RESET pin)
  - 8-pin PDIP 300-mil
  - 24-ball TFBGA 8x6-mm (6x4/5x5 ball array)
  - Contact Winbond for KGD and other options

3. PACKAGE TYPES AND PIN CONFIGURATIONS

3.1 Pin Configuration SOIC 208-mil / VSOP 208-mil

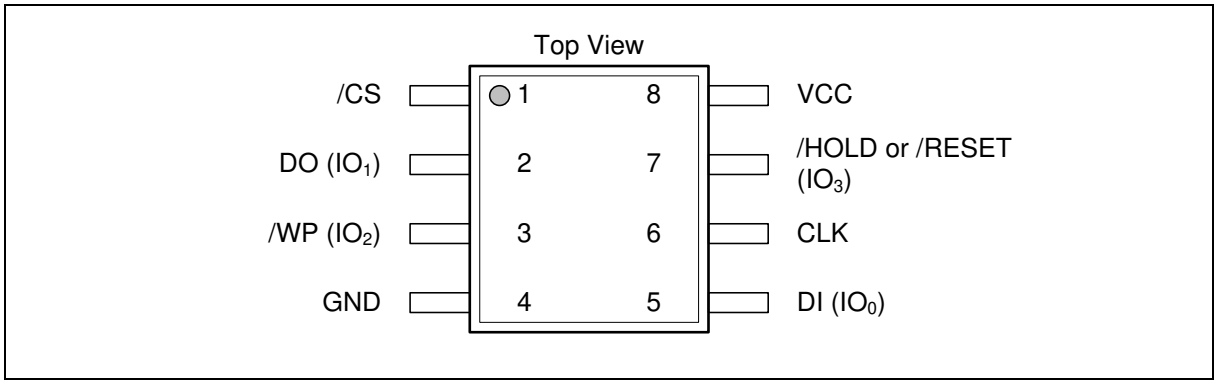

Figure 1a. W25Q32FV Pin Assignments, 8-pin SOIC / VSOP 208-mil (Package Code SS / ST)

3.2 Pad Configuration WSON 6x5-mm / 8x6-mm

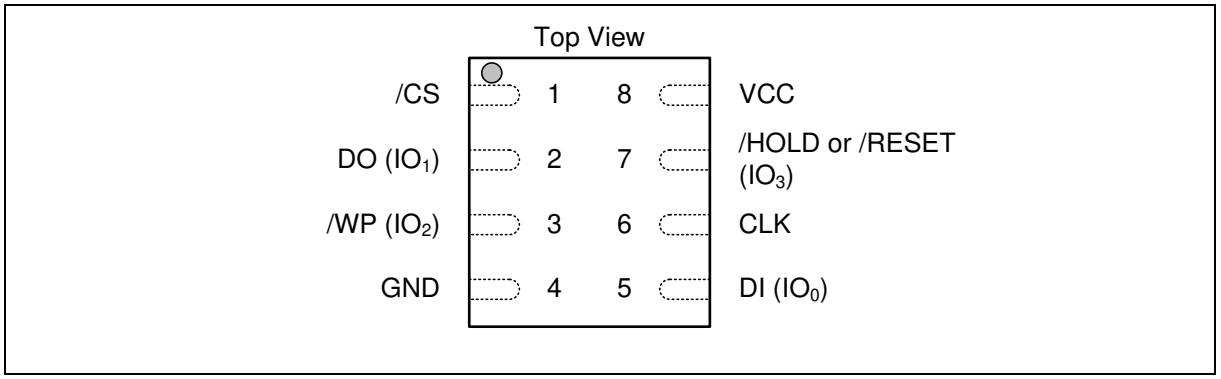

Figure 1b. W25Q32FV Pad Assignments, 8-pad WSON 6x5-mm / 8x6-mm (Package Code ZP / ZE)

3.3 Pin Description SOIC / VSOP 208-mil, WSON 6x5-mm / 8x6-mm

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	/HOLD or /RESET (IO3)	I/O	Hold or Reset Input (Data Input Output 3)(2)
8	VCC		Power Supply

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD (or /RESET) functions are only available for Standard/Dual SPI.

3.4 Pin Configuration SOIC 300-mil

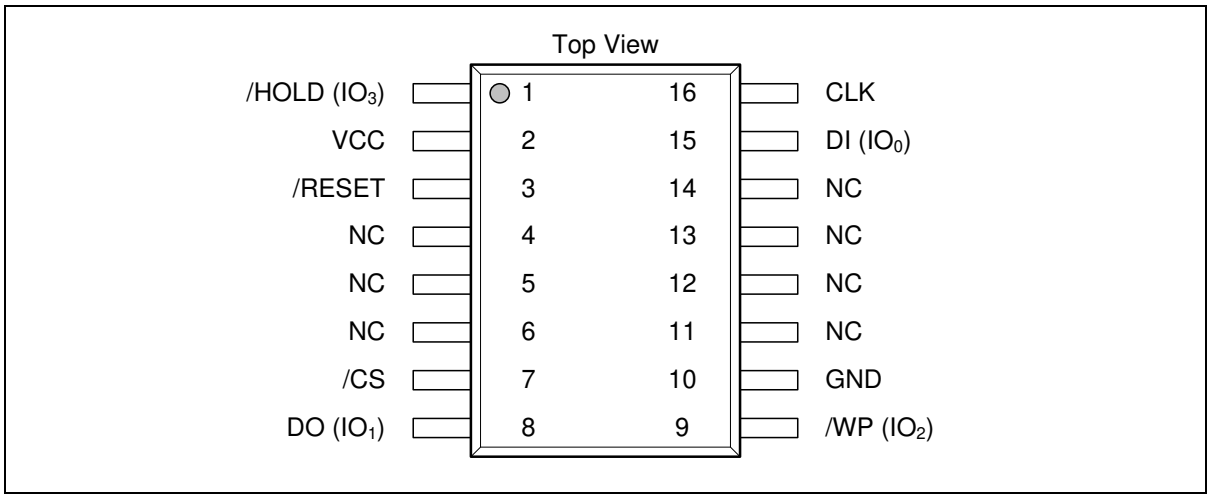

Figure 1c. W25Q32FV Pin Assignments, 16-pin SOIC 300-mil (Package Code SF)

3.5 Pin Description SOIC 300-mil

PIN NO.	PIN NAME	I/O	FUNCTION
1	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)(2)
2	VCC		Power Supply
3	/RESET	I	Reset Input(3)
4	N/C		No Connect
5	N/C		No Connect
6	N/C		No Connect
7	/CS	I	Chip Select Input
8	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
9	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
10	GND		Ground
11	N/C		No Connect
12	N/C		No Connect
13	N/C		No Connect
14	N/C		No Connect
15	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
16	CLK	I	Serial Clock Input

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD (or /RESET) functions are only available for Standard/Dual SPI.
3. The /RESET pin on SOIC-16 package is independent of the HOLD/RST bit and QE bit settings in the Status Register. This pin can be left floating, if Rest function is not needed.

3.6 Ball Configuration TFBGA 8x6-mm (5x5 or 6x4 Ball Array)

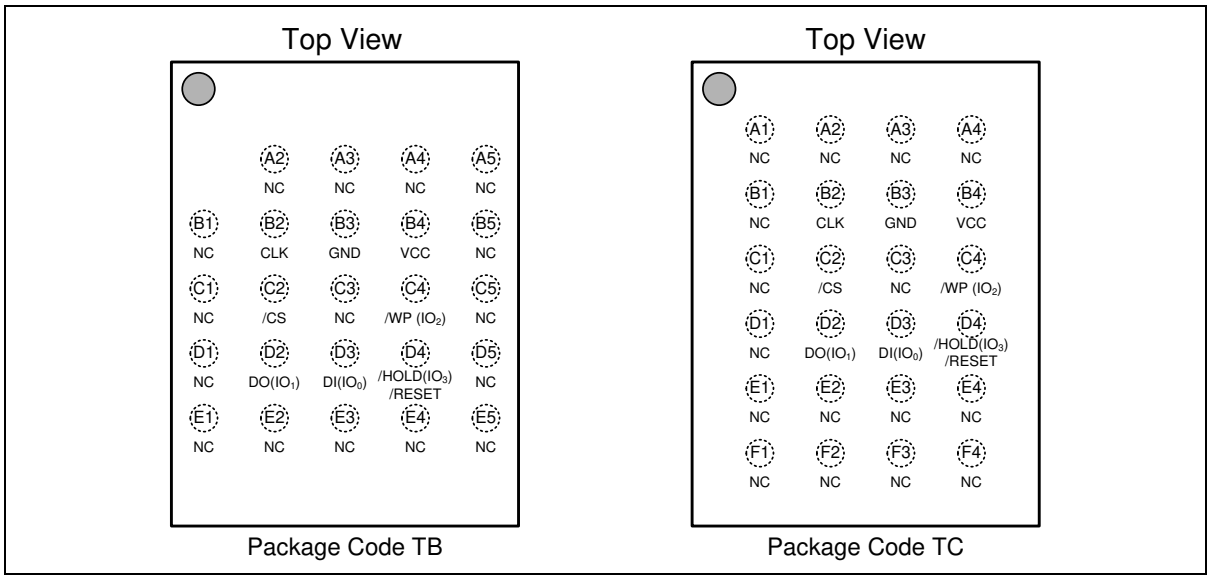

Figure 1d. W25Q32FV Ball Assignments, 24-ball TFBGA 8x6-mm (Package Code TB & TC)

3.7 Ball Description TFBGA 8x6-mm

BALL NO.	PIN NAME	I/O	FUNCTION
B2	CLK	I	Serial Clock Input
B3	GND		Ground
B4	VCC		Power Supply
C2	/CS	I	Chip Select Input
C4	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
D2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
D3	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
D4	/HOLD or /RESET (IO3)	I/O	Hold or Reset Input (Data Input Output 3)(2)
Multiple	NC		No Connect

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD (or /RESET) functions are only available for Standard/Dual SPI.

3.8 Pin Configuration PDIP 300-mil

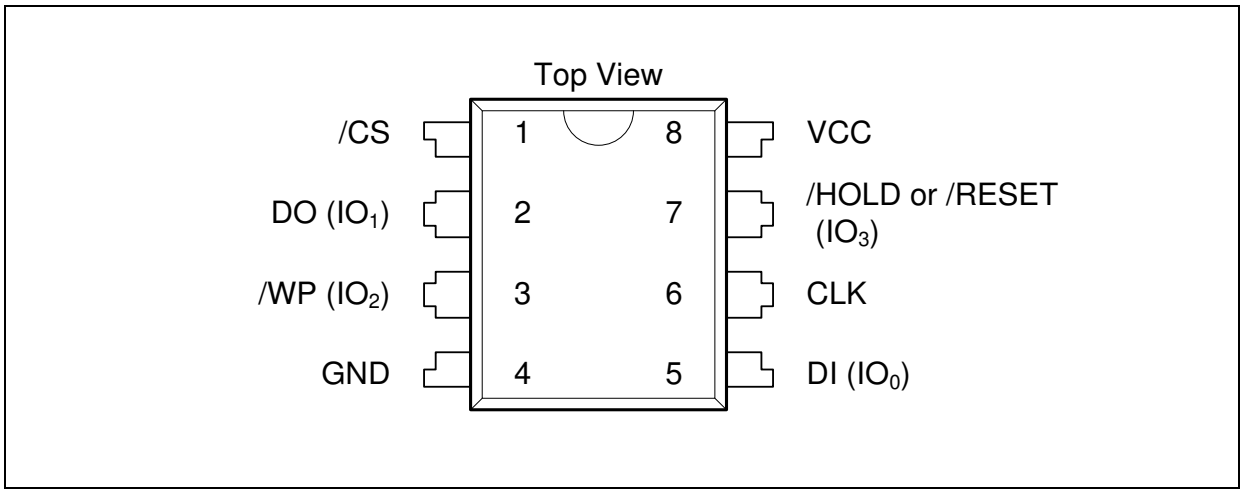

Figure 1e. W25Q32FV Pin Assignments, 8-pin PDIP (Package Code DA)

3.9 Pin Description PDIP 300-mil

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	/HOLD or /RESET (IO3)	I/O	Hold or Reset Input (Data Input Output 3)(2)
8	VCC		Power Supply

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD (or /RESET) functions are only available for Standard/Dual SPI.

4. PIN DESCRIPTIONS

4.1 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down (see “Write Protection” and Figure 58). If needed a pull-up resister on the /CS pin can be used to accomplish this.

4.2 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The W25Q32FV supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

4.3 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The /WP pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /WP pin function is not available since this pin is used for IO2. See Figure 1a-c for the pin configuration of Quad I/O operation.

4.4 HOLD (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /HOLD pin function is not available since this pin is used for IO3. See Figure 1a-e for the pin configuration of Quad I/O operation.

4.5 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

4.6 Reset (/RESET)

The /RESET pin allows the device to be reset by the controller. For 8-pin packages, when QE=0, the IO3 pin can be configured either as a /HOLD pin or as a /RESET pin depending on Status Register setting. When QE=1, the /HOLD or /RESET function is not available for 8-pin configuration. On the 16-pin SOIC package, a dedicated /RESET pin is provided and it is independent of QE bit setting.

5. BLOCK DIAGRAM

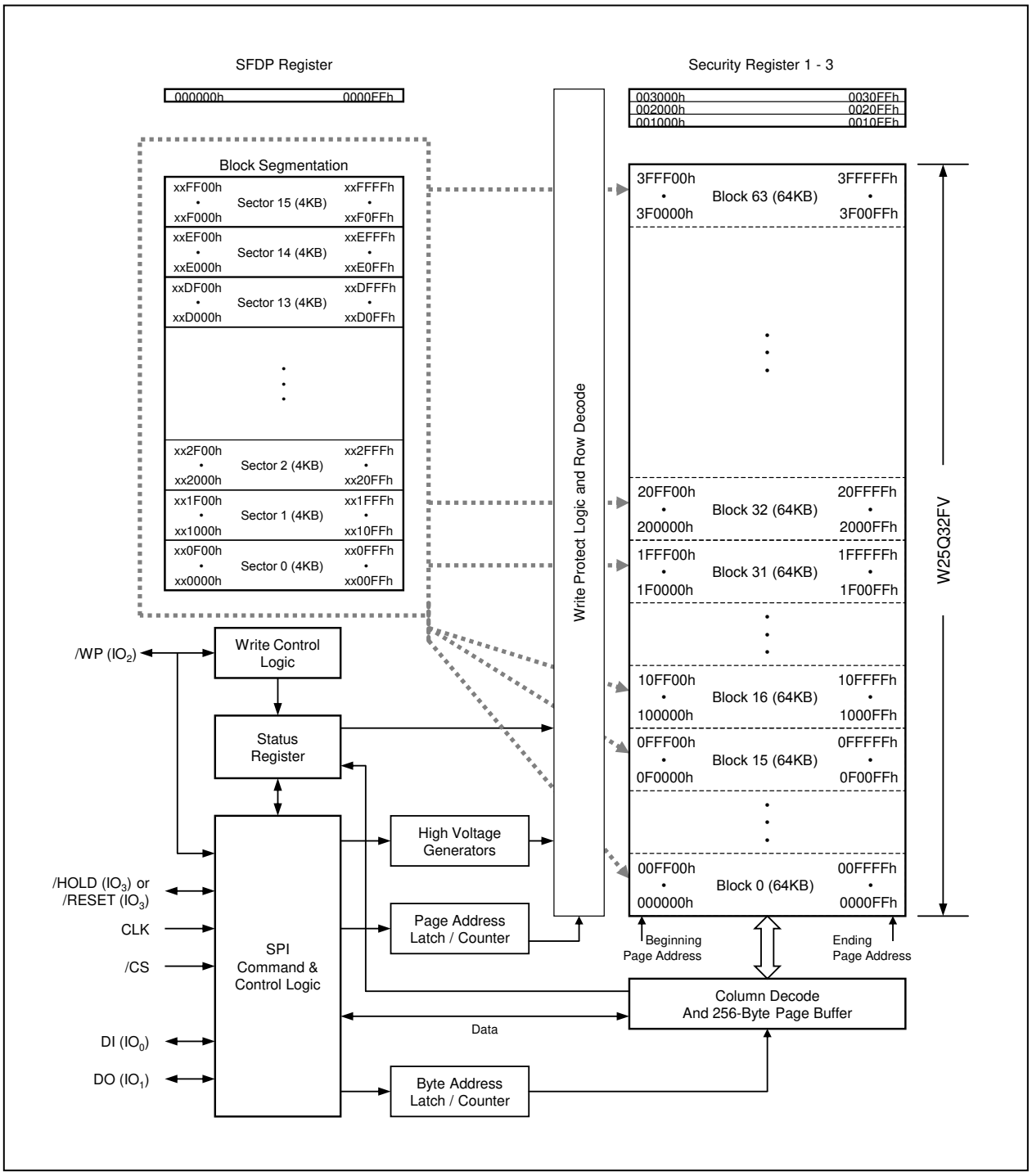

Figure 2. W25Q32FV Serial Flash Memory Block Diagram

6. FUNCTIONAL DESCRIPTIONS

6.1 SPI / QPI Operations

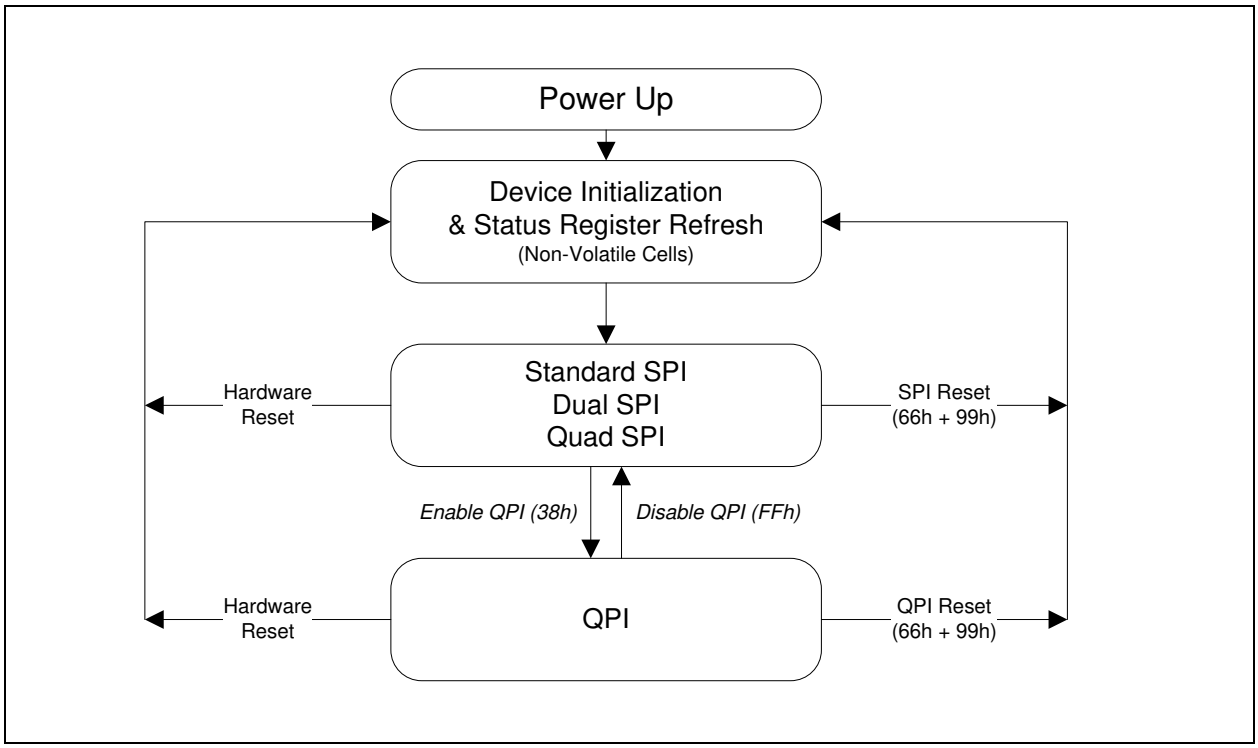

Figure 3. W25Q32FV Serial Flash Memory Operation Diagram

6.1.1 Standard SPI Instructions

The W25Q32FV is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

6.1.2 Dual SPI Instructions

The W25Q32FV supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

6.1.3 Quad SPI Instructions

The W25Q32FV supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)”, “Fast Read Quad I/O (EBh)”, “Word Read Quad I/O (E7h)” and “Octal Word Read Quad I/O (E3h)”. These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

6.1.4 QPI Instructions

The W25Q32FV supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the “Enter QPI (38h)” instruction. The typical SPI protocol requires that the byte-long instruction code being shifted into the device only via DI pin in eight serial clocks. The QPI mode utilizes all four IO pins to input the instruction code, thus only two serial clocks are required. This can significantly reduce the SPI instruction overhead and improve system performance in an XIP environment. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time. “Enter QPI (38h)” and “Exit QPI (FFh)” instructions are used to switch between these two modes. Upon power-up or after a software reset using “Reset (99h)” instruction, the default state of the device is Standard/Dual/Quad SPI mode. To enable QPI mode, the non-volatile Quad Enable bit (QE) in Status Register-2 is required to be set. When using QPI instructions, the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. See Figure 3 for the device operation modes.

6.1.5 Hold Function

For Standard SPI and Dual SPI operations, the /HOLD signal allows the W25Q32FV operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The /HOLD function is only available for standard SPI and Dual SPI operation, not during Quad SPI or QPI. The Quad Enable Bit QE in Status Register-2 is used to determine if the pin is used as /HOLD pin or data I/O pin. When QE=0 (factory default), the pin is /HOLD, when QE=1, the pin will become an I/O pin, /HOLD function is no longer available.

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will terminate after the next falling edge of CLK. During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active (low) for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

6.1.6 Software Reset & Hardware /RESET pin

The W25Q32FV can be reset to the initial power-on state by a software Reset sequence, either in SPI mode or QPI mode. This sequence must include two consecutive commands: Enable Reset (66h) & Reset (99h). If the command sequence is successfully accepted, the device will take approximately 30uS (t_{RST}) to reset. No command will be accepted during the reset period.

For the WSON-8 and TFBGA package types, W25Q32FV can also be configured to utilize a hardware /RESET pin. The HOLD/RST bit in the Status Register-3 is the configuration bit for /HOLD pin function or RESET pin function. When HOLD/RST=0 (factory default), the pin acts as a /HOLD pin as described above; when HOLD/RST=1, the pin acts as a /RESET pin. Drive the /RESET pin low for a minimum period of ~1us (tRESET*) will reset the device to its initial power-on state. Any on-going Program/Erase operation will be interrupted and data corruption may happen. While /RESET is low, the device will not accept any command input.

If QE bit is set to 1, the /HOLD or /RESET function will be disabled, the pin will become one of the four data I/O pins.

For the SOIC-16 package, W25Q32FV provides a dedicated /RESET pin in addition to the /HOLD (IO_3) pin as illustrated in Figure 1b. Drive the /RESET pin low for a minimum period of ~1us (tRESET*) will reset the device to its initial power-on state. The HOLD/RST bit or QE bit in the Status Register will not affect the function of this dedicated /RESET pin.

Hardware /RESET pin has the highest priority among all the input signals. Drive /RESET low for a minimum period of ~1us (tRESET*) will interrupt any on-going external/internal operations, regardless the status of other SPI signals (/CS, CLK, IOs, /WP and/or /HOLD).

Note:

1. While a faster /RESET pulse (as short as a few hundred nanoseconds) will often reset the device, a 1us minimum is recommended to ensure reliable operation.
2. There is an internal pull-up resistor for the dedicated /RESET pin on the SOIC-16 package. If the reset function is not needed, this pin can be left floating in the system.

6.2 Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the W25Q32FV provides several means to protect the data from inadvertent writes.

6.2.1 Write Protect Features

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (/WP pin) write protection using Status Registers
- Additional Individual Block/Sector Locks for array protection
- Write Protection using Power-down instruction
- Lock Down write protection for Status Register until the next power-up
- One Time Program (OTP) write protection for array and Security Registers using Status Register*

  * Note: This feature is available upon special order. Please contact Winbond for details.

Upon power-up or at power-down, the W25Q32FV will maintain a reset condition while VCC is below the threshold value of V_{WI}, (See Power-up Timing and Voltage Levels and Figure 43). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds V_{WI}, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached, and it must also track the VCC supply level at power-down to prevent adverse command sequence. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP0, SRP1) and Block Protect (CMP, SEC, TB, BP[2:0]) bits. These settings allow a portion or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

The W25Q32FV also provides another Write Protect method using the Individual Block Locks. Each 64KB block (except the top and bottom blocks, total of 510 blocks) and each 4KB sector within the top/bottom blocks (total of 32 sectors) are equipped with an Individual Block Lock bit. When the lock bit is 0, the corresponding sector or block can be erased or programmed; when the lock bit is set to 1, Erase or Program commands issued to the corresponding sector or block will be ignored. When the device is powered on, all Individual Block Lock bits will be 1, so the entire memory array is protected from Erase/Program. An “Individual Block Unlock (39h)” instruction must be issued to unlock any specific sector or block.

The WPS bit in Status Register-3 is used to decide which Write Protect scheme should be used. When WPS=0 (factory default), the device will only utilize CMP, SEC, TB, BP[2:0] bits to protect specific areas of the array; when WPS=1, the device will utilize the Individual Block Locks for write protection.

7. STATUS AND CONFIGURATION REGISTERS

Three Status and Configuration Registers are provided for W25Q32FV. The Read Status Register-1/2/3 instructions can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status, Erase/Program Suspend status, output driver strength, power-up and current Address Mode. The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting, Security Register OTP locks, Hold/Reset functions, output driver strength and power-up Address Mode. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP0, SRP1), the Write Enable instruction, and during Standard/Dual SPI operations, the /WP pin.

7.1 Status Registers

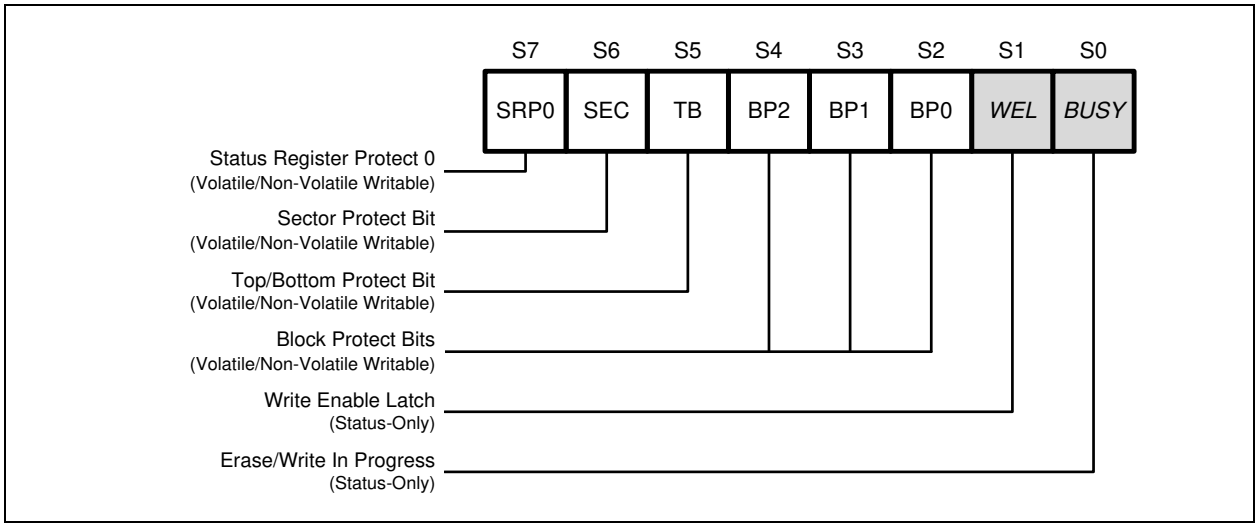

Figure 4a. Status Register-1

7.1.1 Erase/Write In Progress (BUSY) – *Status Only*

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Register instruction. During this time the device will ignore further instructions except for the Read Status Register and Erase/Program Suspend instruction (see tW, tPP, tSE, tBE, and tCE in AC Characteristics). When the program, erase or write status/security register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

7.1.2 Write Enable Latch (WEL) – *Status Only*

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Register and Program Security Register.

7.1.3 Block Protect Bits (BP2, BP1, BP0) – *Volatile/Non-Volatile Writable*

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see tW in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

7.1.4 Top/Bottom Block Protect (TB) – *Volatile/Non-Volatile Writable*

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP0, SRP1 and WEL bits.

7.1.5 Sector/Block Protect Bit (SEC) – *Volatile/Non-Volatile Writable*

The non-volatile Sector/Block Protect bit (SEC) controls if the Block Protect Bits (BP2, BP1, BP0) protect either 4KB Sectors (SEC=1) or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The default setting is SEC=0.

7.1.6 Complement Protect (CMP) – *Volatile/Non-Volatile Writable*

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 64KB block can be protected while the rest of the array is not; when CMP=1, the top 64KB block will become unprotected while the rest of the array become read-only. Please refer to the Status Register Memory Protection table for details. The default setting is CMP=0.

7.1.7 Status Register Protect (SRP1, SRP0) – *Volatile/Non-Volatile Writable*

The Status Register Protect bits (SRP1 and SRP0) are non-volatile read/write bits in the status register (S8 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

SRP1	SRP0	/WP	Status Register	Description
0	0	X	Software Protection	/WP pin has no control. The Status register can be written to after a Write Enable instruction, WEL=1. [Factory Default]
0	1	0	Hardware Protected	When /WP pin is low the Status Register locked and cannot be written to.
0	1	1	Hardware Unprotected	When /WP pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	0	X	Power Supply Lock-Down	Status Register is protected and cannot be written to again until the next power-down, power-up cycle.(1)
1	1	X	One Time Program(2)	Status Register is permanently protected and cannot be written to.

Notes:
1. When SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change SRP1, SRP0 to (0, 0) state.
2. This feature is available upon special order. Please contact Winbond for details.

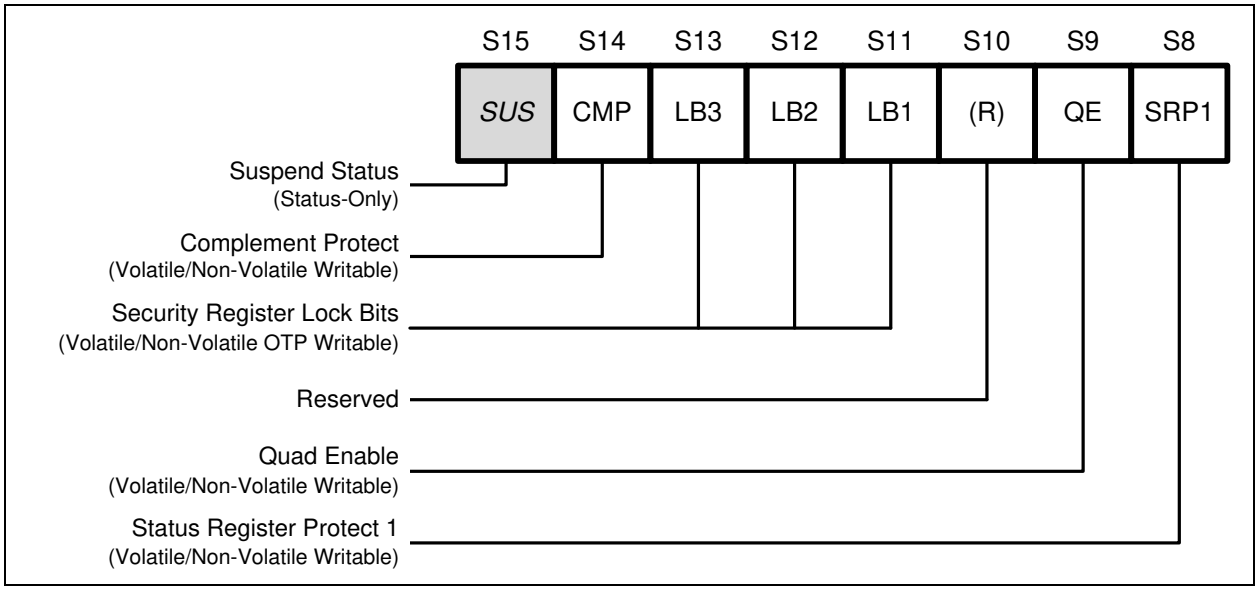

Figure 4b. Status Register-2

7.1.8 Erase/Program Suspend Status (SUS) – *Status Only*

The Suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing a Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power-down, power-up cycle.

7.1.9 Security Register Lock Bits (LB3, LB2, LB1) – *Volatile/Non-Volatile OTP Writable*

The Security Register Lock Bits (LB3, LB2, LB1) are non-volatile One Time Program (OTP) bits in Status Register (S13, S12, S11) that provide the write protect control and status to the Security Registers. The default state of LB3-1 is 0, Security Registers are unlocked. LB3-1 can be set to 1 individually using the Write Status Register instruction. LB3-1 are One Time Programmable (OTP), once it's set to 1, the corresponding 256-Byte Security Register will become read-only permanently.

7.1.10 Quad Enable (QE) – *Volatile/Non-Volatile Writable*

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI and QPI operation. When the QE bit is set to a 0 state (factory default for part numbers with ordering options "IG", and "IF"), the /WP pin and /HOLD are enabled. When the QE bit is set to a 1(factory default for Quad Enabled part numbers with ordering option "IQ"),, the Quad IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled.

QE bit is required to be set to a 1 before issuing an "Enter QPI (38h)" to switch the device from Standard/Dual/Quad SPI to QPI, otherwise the command will be ignored. When the device is in QPI mode, QE bit will remain to be 1. A "Write Status Register" command in QPI mode cannot change QE bit from a "1" to a "0".

WARNING: If the /WP or /HOLD pins are tied directly to the power supply or ground during standard SPI or Dual SPI operation, the QE bit should never be set to a 1.

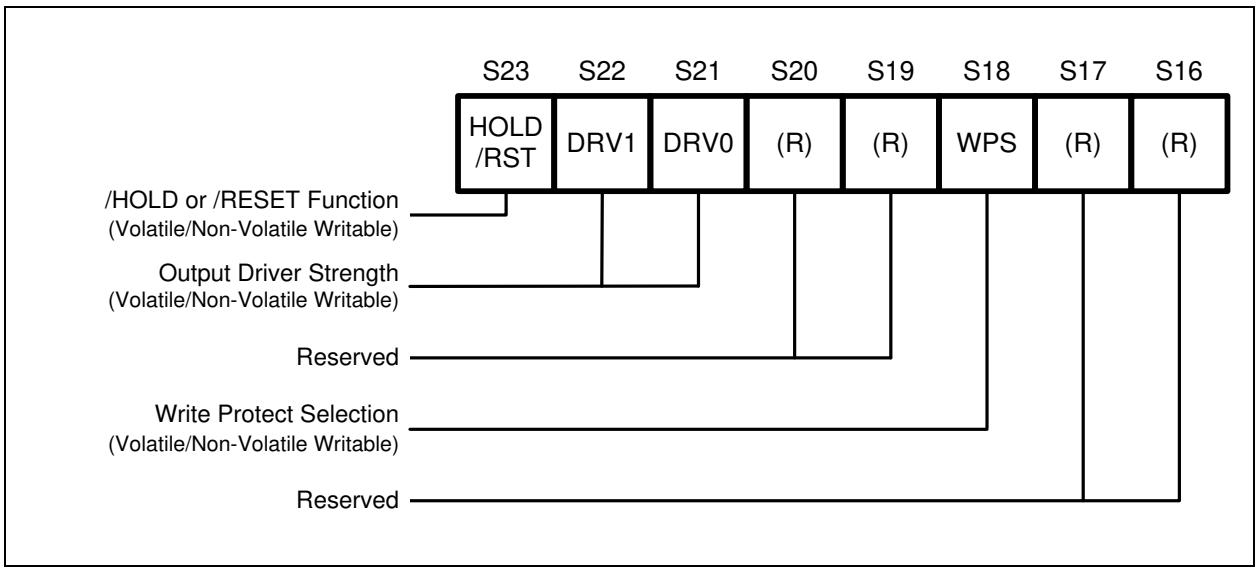

Figure 4c. Status Register-3

7.1.11 Write Protect Selection (WPS) – *Volatile/Non-Volatile Writable*

The WPS bit is used to select which Write Protect scheme should be used. When WPS=0, the device will use the combination of CMP, SEC, TB, BP[2:0] bits to protect a specific area of the memory array. When WPS=1, the device will utilize the Individual Block Locks to protect any individual sector or blocks. The default value for all Individual Block Lock bits is 1 upon device power on or after reset.

7.1.12 Output Driver Strength (DRV1, DRV0) – *Volatile/Non-Volatile Writable*

The DRV1 & DRV0 bits are used to determine the output driver strength for the Read operations.

DRV1, DRV0	Driver Strength
0, 0	100%
0, 1	75%
1, 0	50%
1, 1	25% (default)

7.1.13 /HOLD or /RESET Pin Function (HOLD/RST) – *Volatile/Non-Volatile Writable*

The HOLD/RST bit is used to determine whether /HOLD or /RESET function should be implemented on the hardware pin for 8-pin packages. When HOLD/RST=0 (factory default), the pin acts as /HOLD; when HOLD/RST=1, the pin acts as /RESET. However, /HOLD or /RESET functions are only available when QE=0. If QE is set to 1, the /HOLD and /RESET functions are disabled, the pin acts as a dedicated data I/O pin.

7.1.14 Reserved Bits – *Non Functional*

There are a few reserved Status Register bits that may be read out as a “0” or “1”. It is recommended to ignore the values of those bits. During a “Write Status Register” instruction, the Reserved Bits can be written as “0”, but there will not be any effects.

7.1.15 W25Q32FV Status Register Memory Protection (WPS = 0, CMP = 0)

STATUS REGISTER[1]					W25Q32FV (32M-BIT) MEMORY PROTECTION[3]			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION[2]
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	63	3F0000h – 3FFFFFh	64KB	Upper 1/64
0	0	0	1	0	62 and 63	3E0000h – 3FFFFFh	128KB	Upper 1/32
0	0	0	1	1	60 thru 63	3C0000h – 3FFFFFh	256KB	Upper 1/16
0	0	1	0	0	56 thru 63	380000h – 3FFFFFh	512KB	Upper 1/8
0	0	1	0	1	48 thru 63	300000h – 3FFFFFh	1MB	Upper 1/4
0	0	1	1	0	32 thru 63	200000h – 3FFFFFh	2MB	Upper 1/2
0	1	0	0	1	0	000000h – 00FFFFh	64KB	Lower 1/64
0	1	0	1	0	0 and 1	000000h – 01FFFFh	128KB	Lower 1/32
0	1	0	1	1	0 thru 3	000000h – 03FFFFh	256KB	Lower 1/16
0	1	1	0	0	0 thru 7	000000h – 07FFFFh	512KB	Lower 1/8
0	1	1	0	1	0 thru 15	000000h – 0FFFFFh	1MB	Lower 1/4
0	1	1	1	0	0 thru 31	000000h – 1FFFFFh	2MB	Lower 1/2
X	X	1	1	1	0 thru 63	000000h – 3FFFFFh	4MB	ALL
1	0	0	0	1	63	3FF000h – 3FFFFFh	4KB	U - 1/1024
1	0	0	1	0	63	3FE000h – 3FFFFFh	8KB	U - 1/512
1	0	0	1	1	63	3FC000h – 3FFFFFh	16KB	U - 1/256
1	0	1	0	X	63	3F8000h – 3FFFFFh	32KB	U - 1/128
1	1	0	0	1	0	000000h – 000FFFh	4KB	L - 1/1024
1	1	0	1	0	0	000000h – 001FFFh	8KB	L - 1/512
1	1	0	1	1	0	000000h – 003FFFh	16KB	L - 1/256
1	1	1	0	X	0	000000h – 007FFFh	32KB	L - 1/128

Notes:
1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored

7.1.16 W25Q32FV Status Register Memory Protection (WPS = 0, CMP = 1)

STATUS REGISTER[1]					W25Q32FV (32M-BIT) MEMORY PROTECTION[3]			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION[2]
X	X	0	0	0	0 thru 63	000000h – 3FFFFFh	4MB	ALL
0	0	0	0	1	0 thru 62	000000h – 3EFFFFh	4,032KB	Lower 63/64
0	0	0	1	0	0 and 61	000000h – 3DFFFFh	3,968KB	Lower 31/32
0	0	0	1	1	0 thru 59	000000h – 3BFFFFh	3,840KB	Lower 15/16
0	0	1	0	0	0 thru 55	000000h – 37FFFFh	3,584KB	Lower 7/8
0	0	1	0	1	0 thru 47	000000h – 2FFFFFh	3MB	Lower 3/4
0	0	1	1	0	0 thru 31	000000h – 1FFFFFh	2MB	Lower 1/2
0	1	0	0	1	1 thru 63	010000h – 3FFFFFh	4,032KB	Upper 63/64
0	1	0	1	0	2 and 63	020000h – 3FFFFFh	3,968KB	Upper 31/32
0	1	0	1	1	4 thru 63	040000h – 3FFFFFh	3,840KB	Upper 15/16
0	1	1	0	0	8 thru 63	080000h – 3FFFFFh	3,584KB	Upper 7/8
0	1	1	0	1	16 thru 63	100000h – 3FFFFFh	3MB	Upper 3/4
0	1	1	1	0	32 thru 63	200000h – 3FFFFFh	2MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 thru 63	000000h – 3FEFFFh	4,092KB	L - 1023/1024
1	0	0	1	0	0 thru 63	000000h – 3FDFFFh	4,088KB	L - 511/512
1	0	0	1	1	0 thru 63	000000h – 3FBFFFh	4,080KB	L - 255/256
1	0	1	0	X	0 thru 63	000000h – 3F7FFFh	4,064KB	L - 127/128
1	1	0	0	1	0 thru 63	001000h – 3FFFFFh	4,092KB	U - 1023/1024
1	1	0	1	0	0 thru 63	002000h – 3FFFFFh	4,088KB	U - 511/512
1	1	0	1	1	0 thru 63	004000h – 3FFFFFh	4,080KB	U - 255/256
1	1	1	0	X	0 thru 63	008000h – 3FFFFFh	4,064KB	U - 127/128

Notes:
4. X = don't care
5. L = Lower; U = Upper
6. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored

7.1.17 W25Q32FV Individual Block Memory Protection (WPS=1)

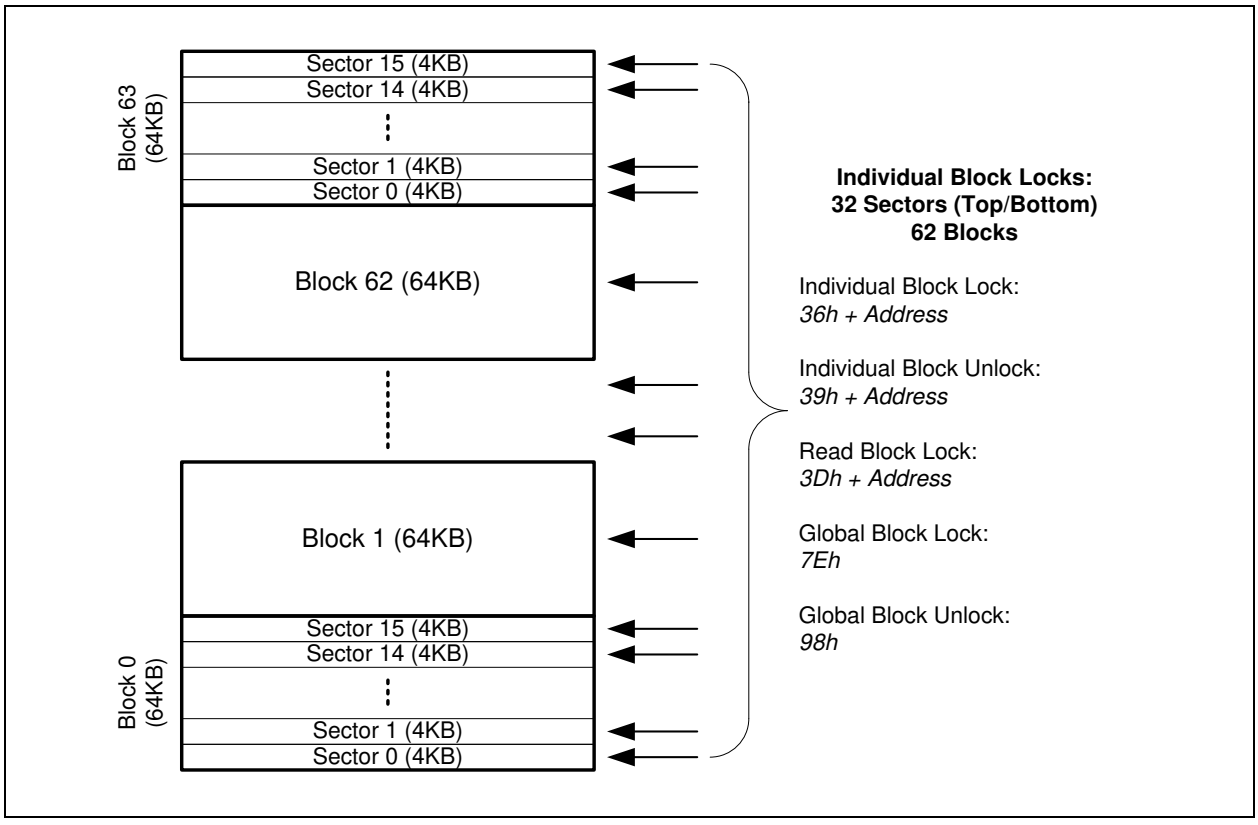

Figure 4d. Individual Block/Sector Locks

Notes:
1. Individual Block/Sector protection is only valid when WPS=1.
2. All individual block/sector lock bits are set to 1 by default after power up, all memory array is protected.

8. INSTRUCTIONS

The Standard/Dual/Quad SPI instruction set of the W25Q32FV consists of 45 basic instructions that are fully controlled through the SPI bus (see Instruction Set Table1-2). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

The QPI instruction set of the W25Q32FV consists of 32 basic instructions that are fully controlled through the SPI bus (see Instruction Set Table 3). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked through IO[3:0] pins provides the instruction code. Data on all four IO pins are sampled on the rising edge of clock with most significant bit (MSB) first. All QPI instructions, addresses, data and dummy bytes are using all four IO pins to transfer every byte of data with every two serial clocks (CLK).

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in Figures 5 through 57. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

8.1 Device ID and Instruction Set Tables

8.1.1 Manufacturer and Device Identification

MANUFACTURER ID	**(MF7 - MF0)**	
Winbond Serial Flash	EFh	
Device ID	**(ID7 - ID0)**	**(ID15 - ID0)**
Instruction	**ABh, 90h, 92h, 94h**	**9Fh**
W25Q32FV (SPI Mode)	15h	4016h
W25Q32FV (QPI Mode)	15h	6016h