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1.8V 8M-BIT
SERIAL FLASH MEMORY WITH
DUAL/QUAD SPI & QPI

Publication Release Date: August 22, 2017

Table of Contents

1. GENERAL DESCRIPTIONS

The W25Q80EW (8M-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25Q series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 1.65V to 1.95V power supply with current consumption as low as 1mA active and 1µA for power-down. All devices are offered in space-saving packages.

The W25Q80EW array is organized into 4,096 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The W25Q80EW has 256 erasable sectors and 16 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See figure 2.)

The W25Q80EW supports the standard Serial Peripheral Interface (SPI), and a high performance Dual/Quad output as well as Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz (104MHz x 2) for Dual I/O and 416MHz (104MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O instructions. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories.

A Hold pin, Write Protect pin and programmable write protection, with top, bottom or complement array control, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device identification with a 64-bit Unique Serial Number.

2. FEATURES

- **Family of SpiFlash Memories**
  - 8M-bit/1M-byte (1,048,576)
  - 256-byte per programmable page
  - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  - Dual SPI: CLK, /CS, IO_0, IO_1, /WP, /Hold
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - QPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
- **Highest Performance Serial Flash**
  - 104MHz Dual/Quad SPI clocks
  - 208/416MHz equivalent Dual/Quad SPI
  - 50MB/S continuous data transfer rate
  - Up to 6X that of ordinary Serial Flash
  - Min 100K Program-Erase cycles per sector
  - More than 20-year data retention
- **Low Power, Wide Temperature Range**
  - Single 1.65V to 1.95V supply
  - 1mA active current
  -- <1µA Power-down current
  - -40°C to +85°C operating range
- **Flexible Architecture with 4KB sectors**
  - Uniform Sector Erase (4K-bytes)
  - Uniform Block Erase (32K and 64K-bytes)
  - Program one to 256 bytes
  - Erase/Program Suspend & Resume
- **Advanced Security Features**
  - Software and Hardware Write-Protect
  - Top/Bottom, 4KB complement array protection
  - Lock-Down and Special OTP array protection
  - 64-Bit Unique Serial Number for each device
  - Discoverable Parameters (SFDP) Register
  - 3X256-Byte Security Registers with OTP locks
  - Volatile & Non-volatile Status Register Bits
- **Space Efficient Packaging**:
  - 8-pin SOIC 150/208-mil
  - 8-pin VSOP 150-mil
  - 8-pad WSON 6X5-mm
  - USON8 2X3mm
  - 8-ball WLCSP
  - Contact Winbond for KGD and other

3. PACKAGE TYPES:

W25Q80EW is offered in an 8-pin SOIC 208-mil (package code SS), an 8-pin 150-mil width SOIC (package code SN), an 8-pin VSOP 150-mil (package code SV), an an 8-pad USON 2x3-mm (package code UX), and an 8-pad WLCSP as shown in figure 1a-1c respectively. Package diagrams and dimensions are illustrated at the end of this datasheet.

3.1 Pin Configuration SOIC 150/208-mil AND VSOP 150-mil

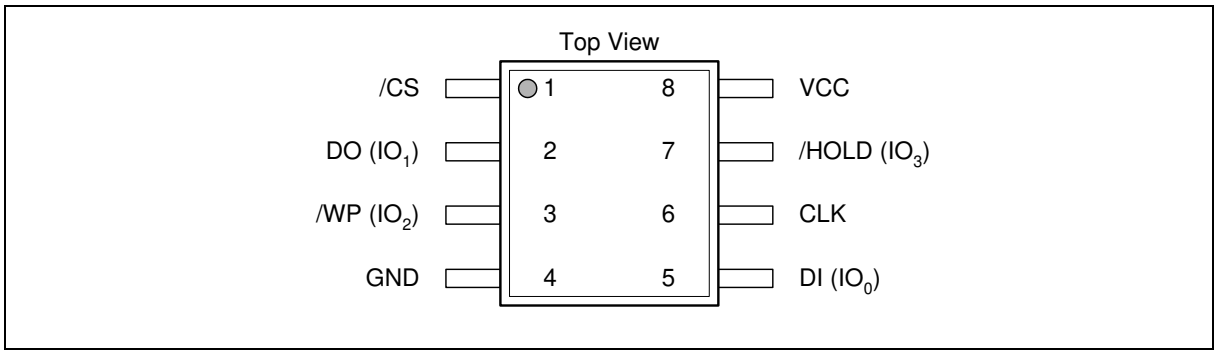

Figure 1a. W25Q80EW Pin Assignments, 8-pin SOIC 150-mil & VSOP 150-mil (Package Code SN,SS, SV)

3.2 PAD Configuration WSON 6x5-MM AND USON 2x3-mm

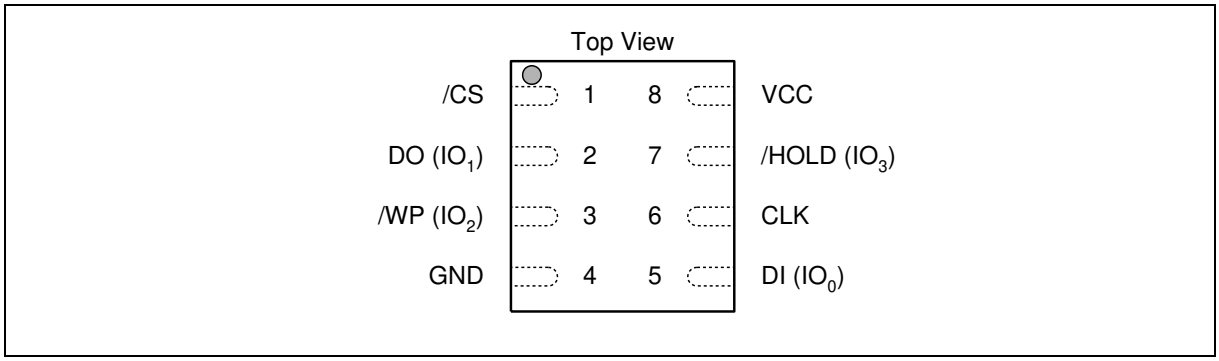

Figure 1b. W2580EW Pad Assignments WSON6X5 & USON 2x3-MM(Package Code ZP, UX)

3.3 Pin Description SOIC150/208-mil, VSOP 150-mil, WSON 6x5-MM,USON 2x3

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)*1
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)*2
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)*1
6	CLK	I	Serial Clock Input
7	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)*2
8	VCC		Power Supply

*1 IO0 and IO1 are used for Standard and Dual SPI instructions
*2 IO0 – IO3 are used for Quad SPI instructions

3.4 Ball Configuration WLCSP

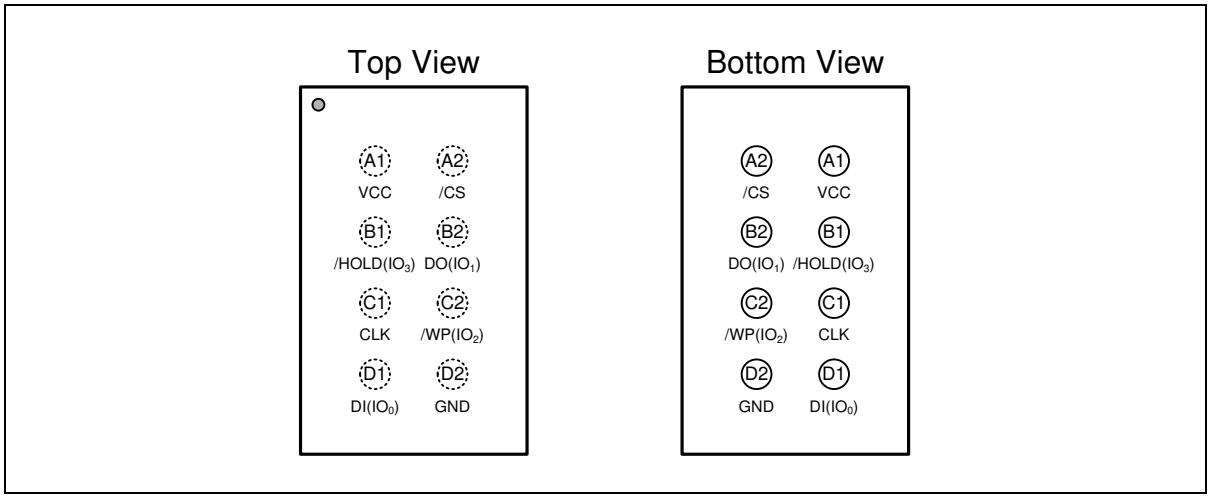

Figure 1c. W25Q80EW Ball Assignments, 8-ball WLCSP (Package Code BY)

3.5 Ball Description WLCSP

BALL NO.	PIN NAME	I/O	FUNCTION
A1	VCC		Power Supply
A2	/CS	I	Chip Select Input
B1	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)*2
B2	DO (IO1)	I/O	Data Output (Data Input Output 1)*1
C1	CLK	I	Serial Clock Input
C2	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)*2
D1	DI (IO0)	I/O	Data Input (Data Input Output 0)*1
D2	GND		Ground

*1 IO0 and IO1 are used for Standard and Dual SPI instructions
*2 IO0 – IO3 are used for Quad SPI instructions

4. PIN DESCRIPTIONS

4.1 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up (see “Write Protection” and figure 37). If needed a pull-up resister on /CS can be used to accomplish this.

4.2 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The W25Q80EW supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

4.3 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The /WP pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /WP pin function is not available since this pin is used for IO2. See figure 1a-b for the pin configuration of Quad I/O operation.

4.4 HOLD (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /HOLD pin function is not available since this pin is used for IO3. See figure 1a-c for the pin configuration of Quad I/O operation.

4.5 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

5. BLOCK DIAGRAM

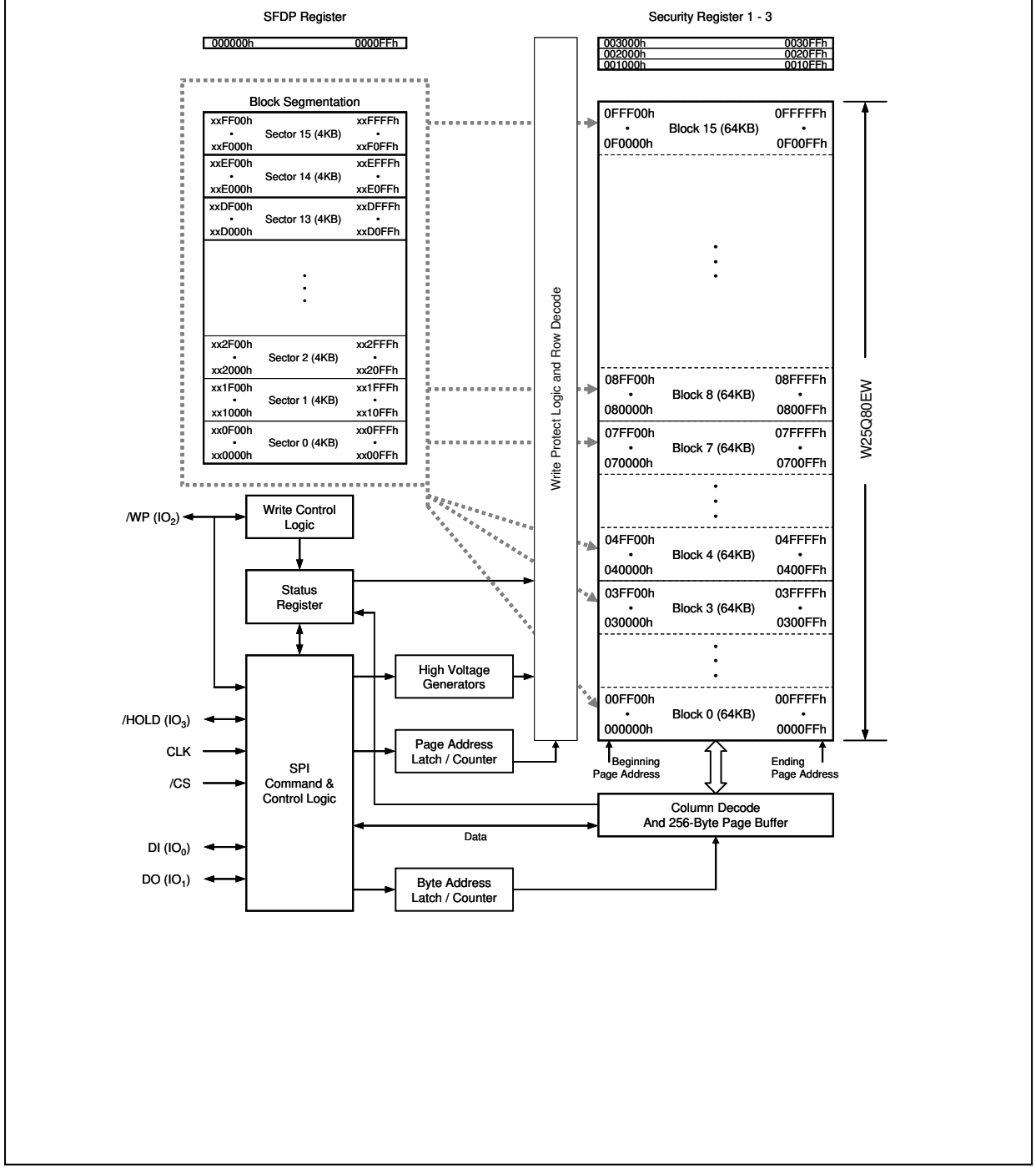

Figure 2. W25Q80EW Serial Flash Memory Block Diagram

6. FUNCTIONAL DESCRIPTION

6.1 SPI / QPI Operations

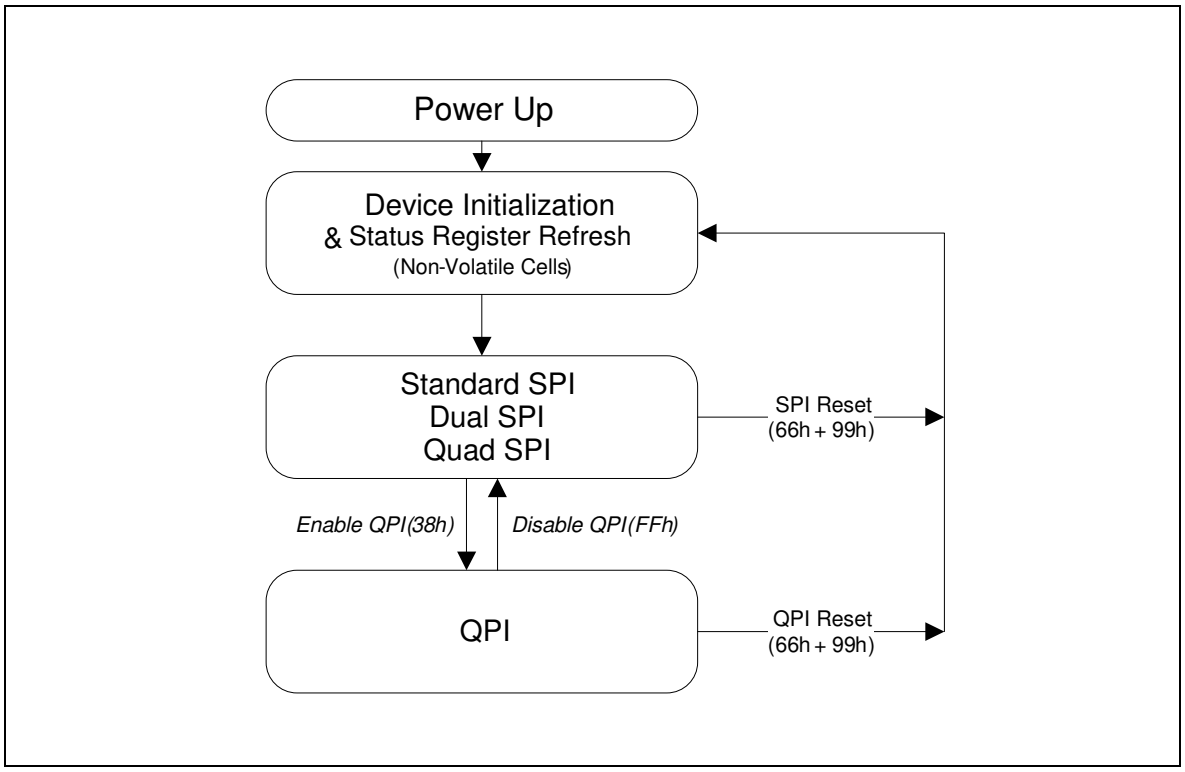

Figure 3. W25Q80EW Serial Flash Memory Operation Diagram

6.2 SPI OPERATIONS

6.2.1 Standard SPI Instructions

The W25Q80EW is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

6.2.2 Dual SPI Instructions

The W25Q80EW supports Dual SPI operation when using the “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)” instructions. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical

code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

6.2.3 Quad SPI Instructions

The W25Q80EW supports Quad SPI operation when using the "Fast Read Quad Output (6Bh)", and "Fast Read Quad I/O (EBh)" instructions. These instructions allow data to be transferred to or from the device six to eight times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

6.3 QPI Instructions

The W25Q80EW supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the "Enter QPI (38h)" instruction. The typical SPI protocol requires that the byte-long instruction code being shifted into the device only via DI pin in eight serial clocks. The QPI mode utilizes all four IO pins to input the instruction code, thus only two serial clocks are required. This can significantly reduce the SPI instruction overhead and improve system performance in an XIP environment. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time. "Enter QPI (38h)" and "Exit QPI (FFh)" instructions are used to switch between these two modes. Upon power-up or after a software reset using "Reset (99h)" instruction, the default state of the device is Standard/Dual/Quad SPI mode. To enable QPI mode, the non-volatile Quad Enable bit (QE) in Status Register-2 is required to be set. When using QPI instructions, the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. See Figure 3 for the device operation modes.

6.3.1 Hold Function

For Standard SPI and Dual SPI operations, the /HOLD signal allows the W25Q80EW operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The /HOLD function is only available for standard SPI and Dual SPI operation, not during Quad SPI or QPI. The Quad Enable Bit QE in Status Register-2 is used to determine if the pin is used as /HOLD pin or data I/O pin. When QE=0 (factory default), the pin is /HOLD, when QE=1, the pin will become an I/O pin, /HOLD function is no longer available.

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will terminate after the next falling edge of CLK. During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active low for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

6.4 WRITE PROTECTION

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the W25Q80EW provides several means to protect the data from inadvertent writes.

6.4.1 Write Protect Features

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (/WP pin) write protection using Status Register
- Write Protection using Power-down instruction
- Lock Down write protection until next power-up
- One Time Program (OTP) write protection*

* Note: This feature is available upon special order. Please contact Winbond for details.

Upon power-up or at power-down, the W25Q80EW will maintain a reset condition while VCC is below the threshold value of V_{WI}, (See Power-up Timing and Voltage Levels and Figure 37). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds V_{WI}, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP, SRL) and Block Protect (CMP, SEC,TB, BP2, BP1 and BP0) bits. These settings allow a portion as small as 4KB sector or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

7. STATUS REGISTERS AND INSTRUCTIONS

The Read Status Register-1 and Status Register-2 instructions can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status and Erase/Program Suspend status. The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting and Security Register OTP lock. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP, SRL), the Write Enable instruction, and during Standard/Dual SPI operations, the /WP pin.

7.1 STATUS REGISTERs

7.1.1 BUSY Status (BUSY)

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Register instruction. During this time the device will ignore further instructions except for the Read Status Register and Erase/Program Suspend instruction (see tW, tPP, tSE, tBE, and tCE in AC Characteristics). When the program, erase or write status/security register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

7.1.2 Write Enable Latch Status (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Register and Program Security Register.

7.1.3 Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see tW in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

7.1.4 Top/Bottom Block Protect (TB)

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP and WEL bits.

7.1.5 Sector/Block Protect (SEC)

The non-volatile Sector/Block Protect bit (SEC) controls if the Block Protect Bits (BP2, BP1, BP0) protect either 4KB Sectors (SEC=1) or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The default setting is SEC=0.

7.1.6 Complement Protect (CMP)

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 4KB sector can be protected while the rest of the array is not; when CMP=1, the top 4KB sector will become unprotected while the rest of the array become read-only. Please refer to the Status Register Memory Protection table for details. The default setting is CMP=0.

7.1.7 Status Register Protect (SRP, SRL)

The Status Register Protect bits (SRP) are non-volatile read/write bits in the status register (S7). The SRP bits control the method of write protection: software protection,

SRP	/WP	Status Protection	Description
0	X	Software Protection	/WP pin has no control. The Status register can be written to after a Write Enable instruction, WEL=1. [Factory Default]
1	0	Hardware Protected	When /WP pin is low the Status Register can not be written to.
	1	Hardware Unprotected	When /WP pin is high the Status register can be written to after a Write Enable instruction, WEL=1.

SRL	Status Register Lock	Description
0	Non-Lock	Status Register is **unlocked**
1	Lock-Down (1) (temporary/Volatile)	Status Register is **locked by standard status register write command** and can not be written to again until the next power-down, power-up cycle.
	One Time Program(2) (Permanently/Non-Volatile)	Status Register is permanently **locked by special command flow** and can not be written to

1. When SRP =1 , a power-down, power-up cycle will change SRP =0 state.
2. **Special One Time Protection feature is available upon special order; please contact Winbond for details**

7.1.8 Erase/Program Suspend Status (SUS)

The Suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing a Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power-down, power-up cycle.

7.1.9 Security Register Lock Bits (LB[3:0]) – *Volatile/Non-Volatile OTP Writable*

The Security Register Lock Bits (LB3, LB2, LB1, LB0) are non-volatile One Time Program (OTP) bits in Status Register (S13, S12, S11, S10) that provide the write protect control and status to the Security Registers. The default state of LB[3:0] is 0, Security Registers are unlocked. LB3-0 can be set to 1 individually using the Write Status Register instruction. LB3-0 are One Time Programmable (OTP), once it's set to 1, the corresponding 256-Byte Security Register will become read-only permanently.

7.1.10 Quad Enable (QE) – *Non-Volatile Writable*

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI and QPI operation. When the QE bit is set to a 0 state (factory default), the /WP pin and /HOLD are enabled. When the QE bit is set to a 1(factory default for Quad Enabled part numbers with ordering option "IQ"), the Quad IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled.

QE bit is required to be set to a 1 before issuing an "Enter QPI (38h)" to switch the device from Standard/Dual/Quad SPI to QPI, otherwise the command will be ignored. When the device is in QPI mode, QE bit will remain to be 1. A "Write Status Register" command in QPI mode cannot change QE bit from a "1" to a "0".

WARNING: If the /WP or /HOLD pins are tied directly to the power supply or ground during standard SPI or Dual SPI operation, the QE bit should never be set to a 1.

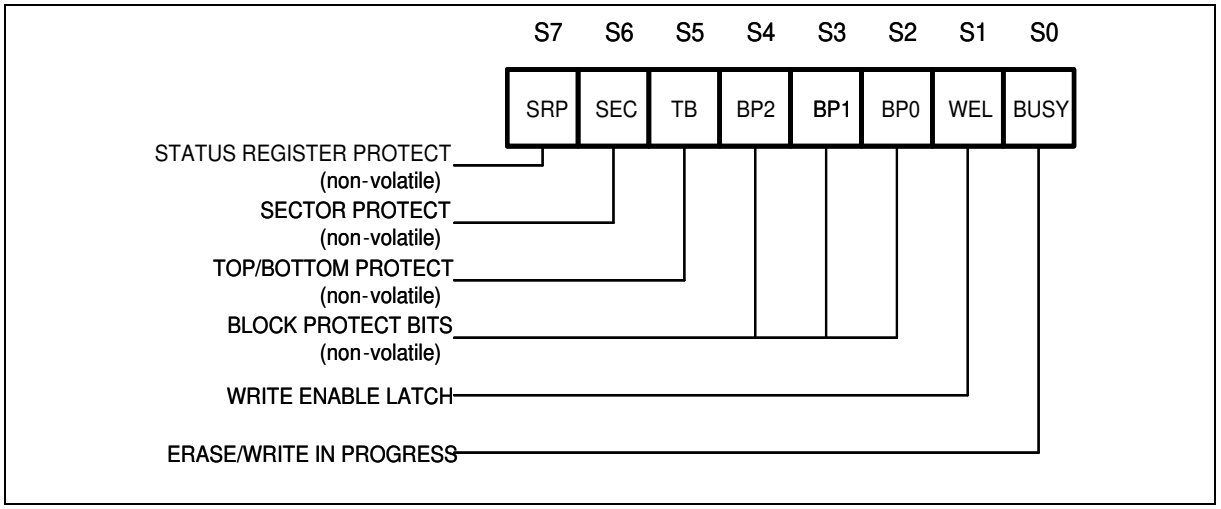

Figure 3a. Status Register-1

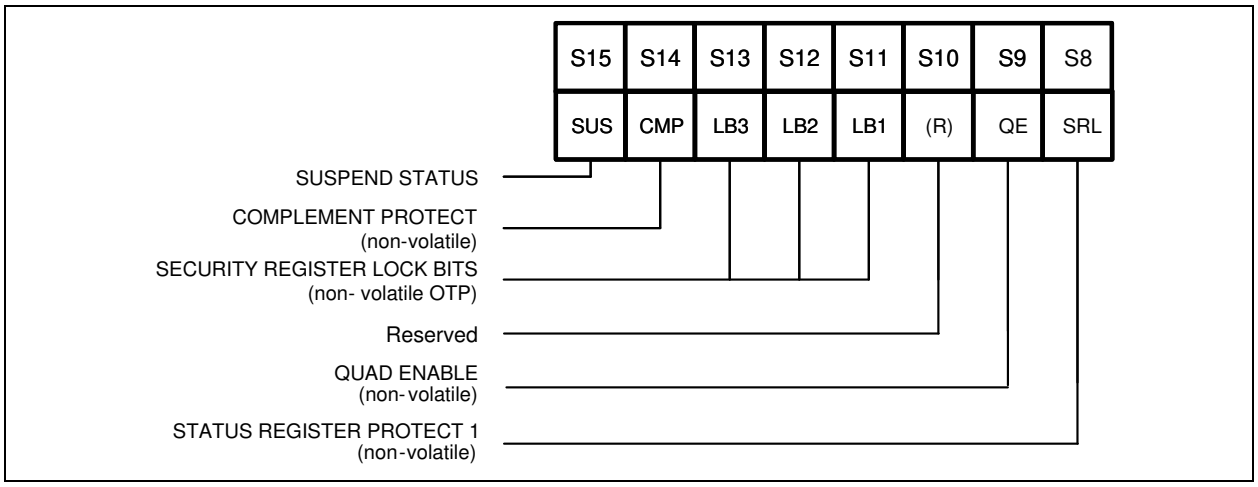

Figure 3b. Status Register-2

7.1.11 Reserved Bits – *Non Functional*

There are a few reserved Status Register bits that may be read out as a "0" or "1". It is recommended to ignore the values of those bits. During a "Write Status Register" instruction, the Reserved Bits can be written as "0", but there will not be any effects.

7.1.12 Status Register Memory Protection (CMP = 0)

STATUS REGISTER(1)					W25Q80EW (8M-BIT) MEMORY PROTECTION(2)			
SEC	TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	15	0F0000h – 0FFFFFh	64KB	Upper 1/16
0	0	0	1	0	14 and 15	0E0000h – 0FFFFFh	128KB	Upper 1/8
0	0	0	1	1	12 thru 15	0C0000h – 0FFFFFh	256KB	Upper 1/4
0	0	1	0	0	8 thru 15	080000h – 0FFFFFh	512KB	Upper 1/2
0	1	0	0	1	0	000000h – 00FFFFh	64KB	Lower 1/16
0	1	0	1	0	0 and 1	000000h – 01FFFFh	128KB	Lower 1/8
0	1	0	1	1	0 thru 3	000000h – 03FFFFh	256KB	Lower 1/4
0	1	1	0	0	0 thru 7	000000h – 07FFFFh	512KB	Lower 1/2
0	X	1	0	1	0 thru 15	000000h – 0FFFFFh	1MB	ALL
0	X	1	1	X	0 thru 15	000000h – 0FFFFFh	1MB	ALL
1	0	0	0	1	15	0FF000h – 0FFFFFh	4KB	Upper 1/256
1	0	0	1	0	15	0FE000h – 0FFFFFh	8KB	Upper 1/128
1	0	0	1	1	15	0FC000h – 0FFFFFh	16KB	Upper 1/64
1	0	1	0	X	15	0F8000h – 0FFFFFh	32KB	Upper 1/32
1	1	0	0	1	0	000000h – 000FFFh	4KB	Lower 1/256
1	1	0	1	0	0	000000h – 001FFFh	8KB	Lower 1/128
1	1	0	1	1	0	000000h – 003FFFh	16KB	Lower 1/64
1	1	1	0	X	0	000000h – 007FFFh	32KB	Lower 1/32
1	X	1	1	1	0 thru 15	000000h – 0FFFFFh	1MB	ALL

Notes:
1. X = don't care
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

7.1.13 Status Register Memory Protection (CMP = 1)

STATUS REGISTER(1)					W25Q80EW (8M-BIT) MEMORY PROTECTION(2)			
SEC	TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	0 thru 15	000000h – 0FFFFFh	1MB	ALL
0	0	0	0	1	0 thru 14	000000h – 0EFFFFh	960KB	Lower 15/16
0	0	0	1	0	0 thru 13	000000h – 0DFFFFh	896KB	Lower 7/8
0	0	0	1	1	0 thru 11	000000h – 0BFFFFh	768KB	Lower 3/4
0	0	1	0	0	0 thru 7	000000h – 07FFFFh	512KB	Lower 1/2
0	1	0	0	1	1 thru 15	010000h – 0FFFFFh	960KB	Upper 15/16
0	1	0	1	0	2 thru 15	020000h – 0FFFFFh	896KB	Upper 7/8
0	1	0	1	1	4 thru 15	040000h – 0FFFFFh	768KB	Upper 3/4
0	1	1	0	0	8 thru 15	080000h – 0FFFFFh	512KB	Upper 1/2
0	X	1	0	1	NONE	NONE	NONE	NONE
0	X	1	1	X	NONE	NONE	NONE	NONE
1	0	0	0	1	0 thru 15	000000h – 0FEFFFh	1,020KB	Lower 255/256
1	0	0	1	0	0 thru 15	000000h – 0FDFFFh	1,016KB	Lower 127/128
1	0	0	1	1	0 thru 15	000000h – 0FBFFFh	1,008KB	Lower 63/64
1	0	1	0	X	0 thru 15	000000h – 0F7FFFh	992KB	Lower 31/32
1	1	0	0	1	0 thru 15	001000h – 0FFFFFh	1,020KB	Upper 255/256
1	1	0	1	0	0 thru 15	002000h – 0FFFFFh	1,016KB	Upper 127/128
1	1	0	1	1	0 thru 15	004000h – 0FFFFFh	1,008KB	Upper 63/64
1	1	1	0	X	0 thru 15	008000h – 0FFFFFh	992KB	Upper 31/32
1	X	1	1	1	NONE	NONE	NONE	NONE

Notes:
1. X = don't care
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

7.1.14 INSTRUCTIONS

The instruction set of the W25Q80EW consists of thirty four basic instructions that are fully controlled through the SPI bus (see Instruction Set table1-3). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

The QPI instruction set of the W25Q80EW consists of 32 basic instructions that are fully controlled through the SPI bus (see Instruction Set Table 3). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked through IO[3:0] pins provides the instruction code. Data on all four IO pins are sampled on the rising edge of clock with most significant bit (MSB) first. All QPI instructions, addresses, data and dummy bytes are using all four IO pins to transfer every byte of data with every two serial clocks (CLK).

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in figures 4 through 36. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

7.1.15 Manufacturer and Device Identification

MANUFACTURER ID	**(MF7-MF0)**	
Winbond Serial Flash	EFh	
Device ID	**(ID7-ID0)**	**(ID15-ID0)**
Instruction	**ABh, 90h, 92h, 94h**	**9Fh**
W25Q80EW	13h	6014

7.1.16 Instruction Set Table 1 (Standard SPI Instructions)(1)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock(1-1-1)	**8**	**8**	**8**	**8**	**8**	**8**	**8**
Write Enable	**06h**						
Volatile SR Write Enable	**50h**						
Write Disable	**04h**						
Release Power-down / ID	**ABh**	Dummy	Dummy	Dummy	(ID7-ID0)(2)		
Manufacturer/Device ID	**90h**	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)	
JEDEC ID	**9Fh**	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Read Unique ID	**4Bh**	Dummy	Dummy	Dummy	Dummy	(UID63-0)	
Read Data	**03h**	A23-A16	A15-A8	A7-A0	(D7-D0)		
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Page Program	**02h**	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)	
Sector Erase (4KB)	**20h**	A23-A16	A15-A8	A7-A0			
Block Erase (32KB)	**52h**	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	**D8h**	A23-A16	A15-A8	A7-A0			
Chip Erase	**C7h/60h**						
Read Status Register-1	**05h**	(S7-S0)(2)					
Write Status Register-1(4)	**01h**	(S7-S0)(4)					
Read Status Register-2	**35h**	(S15-S8)(2)					
Write Status Register-2	**31h**	(S15-S8)					
Read SFDP Register	**5Ah**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Erase Security Register(5)	**44h**	A23-A16	A15-A8	A7-A0			
Program Security Register(5)	**42h**	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(5)	
Read Security Register(5)	**48h**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Erase / Program Suspend(6)	**75h**						
Erase / Program Resume(6)	**7Ah**						
Power-down	**B9h**						
Enter QPI Mode	**38h**						
Enable Reset	**66h**						
Reset Device	**99h**						

7.1.17 Instruction Set Table 2 (Dual/Quad SPI Instructions)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Number of Clock(1-1-2)	**8**	**8**	**8**	**8**	**4**	**4**	**4**	**4**	**4**
Fast Read Dual Output	**3Bh**	A23-A16	A15-A8	A7-A0	Dummy	Dummy	(D7-D0)(7)		
Number of Clock(1-2-2)	**8**	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Fast Read Dual I/O	**BBh**	A23-A16(6)	A15-A8(6)	A7-A0(6)	Dummy(14)	(D7-D0)(7)			
Mftr./Device ID Dual I/O	**92h**	A23-A16(6)	A15-A8(6)	00(6)	Dummy(14)	(MF7-MF0)	(ID7-ID0)(7)		
Number of Clock(1-1-4)	**8**	**8**	**8**	**8**	**2**	**2**	**2**	**2**	**2**
Quad Input Page Program	**32h**	A23-A16	A15-A8	A7-A0	(D7-D0)(9)	(D7-D0)(3)	…		
Fast Read Quad Output	**6Bh**	A23-A16	A15-A8	A7-A0	Dummy	Dummy	Dummy	Dummy	(D7-D0)(10)
Number of Clock(1-4-4)	**8**	**2**(8)	**2**(8)	**2**(8)	**2**	**2**	**2**	**2**	**2**
Mftr./Device ID Quad I/O	**94h**	A23-A16	A15-A8	00	Dummy(14)	Dummy	Dummy	(MF7-MF0)	(ID7-ID0)
Fast Read Quad I/O	**EBh**	A23-A16	A15-A8	A7-A0	Dummy(14)	Dummy	Dummy	(D7-D0)	
Set Burst with Wrap	**77h**	Dummy	Dummy	Dummy	W8-W0				

7.1.18 Instruction Set Table 3 (QPI Instructions) (1)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock (4-4-4)	**2**	**2**	**2**	**2**	**2**	**2**	**2**
Write Enable	**06h**						
Volatile SR Write Enable	**50h**						
Write Disable	**04h**						
Release Power-down / ID	**ABh**	Dummy	Dummy	Dummy	(ID7-ID0)(2)		
Manufacturer/Device ID	**90h**	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)	
JEDEC ID	**9Fh**	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Set Read Parameters	**C0h**	P7-P0					
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	Dummy(12)	(D7-D0)	…
Burst Read with Wrap(5,6)	**0Ch**	A23-A16	A15-A8	A7-A0	Dummy(12)	(D7-D0)	…
Fast Read Quad I/O	**EBh**	A23-A16	A15-A8	A7-A0	M7-M0(12)	(D7-D0)	…
Page Program	**02h**	A23-A16	A15-A8	A7-A0	D7-D0(9)	D7-D0(3)	…
Sector Erase (4KB)	**20h**	A23-A16	A15-A8	A7-A0			
Block Erase (32KB)	**52h**	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	**D8h**	A23-A16	A15-A8	A7-A0			
Chip Erase	**C7h/60h**						
Read Status Register-1	**05h**	(S7-S0)(2)					
Write Status Register-1(4)	**01h**	(S7-S0)(4)					
Read Status Register-2	**35h**	(S15-S8)(2)					
Write Status Register-2	**31h**	(S15-S8)					
Erase / Program Suspend	**75h**						
Erase / Program Resume	**7Ah**						
Power-down	**B9h**						
Enable Reset	**66h**						
Reset Device	**99h**						
Exit QPI Mode	**FFh**						

Note:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "***D7-D0***" indicate data output from the device on either 1, 2 or 4 IO pins. . "D7-D0" indicates single I/O pin; "D7-D0 /2" indicates 2 I/O pins; "D7-D0 /4" indicates 4 I/O pins.
2. The Status Register contents and Device ID will repeat continuously until /CS terminates the instruction.
3. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Registers, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
4. Write Status Register-1 (01h) can also be used to program Status Register-1&2, see section 8.2.5.
5. Security Register Address:
   Security Register 1: A23-16 = 00h; A15-8 = 10h; A7-0 = byte address
   Security Register 2: A23-16 = 00h; A15-8 = 20h; A7-0 = byte address
   Security Register 3: A23-16 = 00h; A15-8 = 30h; A7-0 = byte address
6. Dual SPI address input format:
   IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
   IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1
7. Dual SPI data input/output format:
   IO0 = (D6, D4, D2, D0)
   IO1 = (D7, D5, D3, D1)
8. Quad SPI address input format:
   IO0 = A20, A16, A12, A8, A4, A0, M4, M0
   IO1 = A21, A17, A13, A9, A5, A1, M5, M1
   IO2 = A22, A18, A14, A10, A6, A2, M6, M2
   IO3 = A23, A19, A15, A11, A7, A3, M7, M3

   Set Burst with Wrap input format:
   IO0 = x, x, x, x, x, x, W4, x
   IO1 = x, x, x, x, x, x, W5, x
   IO2 = x, x, x, x, x, x, W6, x
   IO3 = x, x, x, x, x, x, x, x
9. Quad SPI data input/output format:
   IO0 = (D4, D0, ...)
   IO1 = (D5, D1, ...)
   IO2 = (D6, D2, ...)
   IO3 = (D7, D3, ...)
10. Fast Read Quad I/O data output format:
    IO0 = (x, x, x, x, D4, D0, D4, D0)
    IO1 = (x, x, x, x, D5, D1, D5, D1)
    IO2 = (x, x, x, x, D6, D2, D6, D2)
    IO3 = (x, x, x, x, D7, D3, D7, D3)
11. QPI Command, Address, Data input/output format:

CLK # 0	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*	*11*
IO0 = C4,	C0,	A20,	A16,	A12,	A8,	A4,	A0,	D4,	D0,	D4,	D0
IO1 = C5,	C1,	A21,	A17,	A13,	A9,	A5,	A1,	D5,	D1,	D5,	D1
IO2 = C6,	C2,	A22,	A18,	A14,	A10,	A6,	A2,	D6,	D2,	D6,	D2
IO3 = C7,	C3,	A23,	A19,	A15,	A11,	A7,	A3,	D7,	D3,	D7,	D3

12. The number of dummy clocks for QPI Fast Read, QPI Fast Read Quad I/O & QPI Burst Read with Wrap is controlled by read parameter P7 – P4.
13. The wrap around length for QPI Burst Read with Wrap is controlled by read parameter P3 – P0.
14. The first dummy is M7-M0 should be set to Fxh

7.2 Instruction Descriptions

7.2.1 Write Enable (06h)

The Write Enable instruction (Figure 4) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Registers instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code "06h" into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

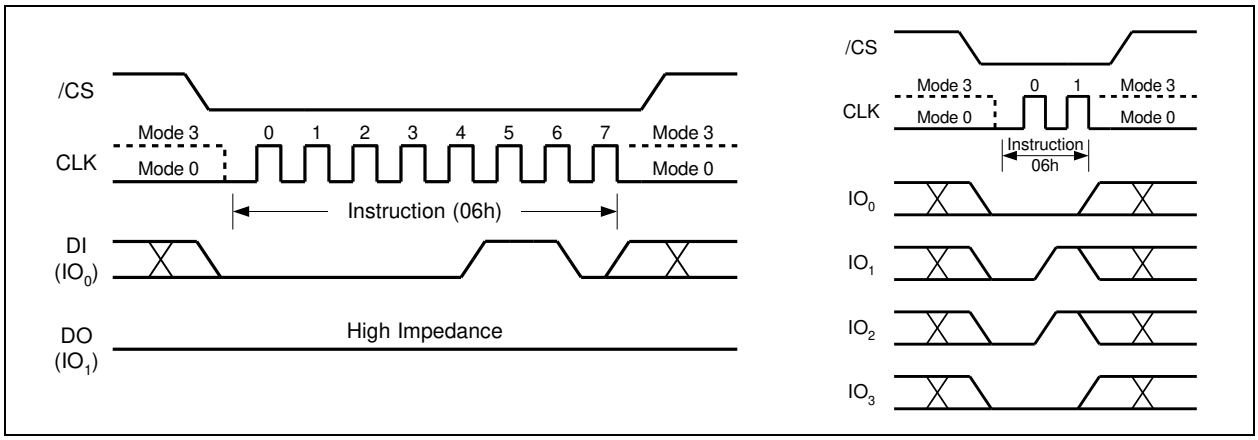

Figure 5. Write Enable Instruction for SPI Mode (left) or QPI Mode (right)

7.2.2 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in section 8.1 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction. Write Enable for Volatile Status Register instruction (Figure 5) will not set the Write Enable Latch (WEL) bit, it is only valid for the Write Status Register instruction to change the volatile Status Register bit values.

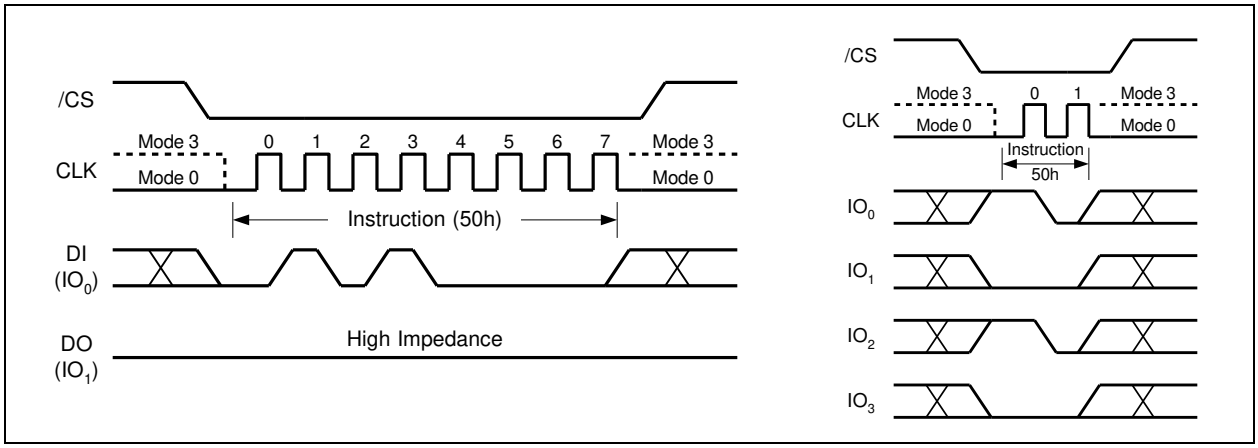

Figure 6. Write Enable for Volatile Status Register Instruction for SPI Mode (left) or QPI Mode (right)

7.2.3 Write Disable (04h)

The Write Disable instruction (Figure 6) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Erase/Program Security Registers, Page Program, Quad Page Program, Sector Erase, Block Erase and Chip Erase instructions.

Write Disable instruction can also be used to invalidate the Write Enable for Volatile Status Register instruction.

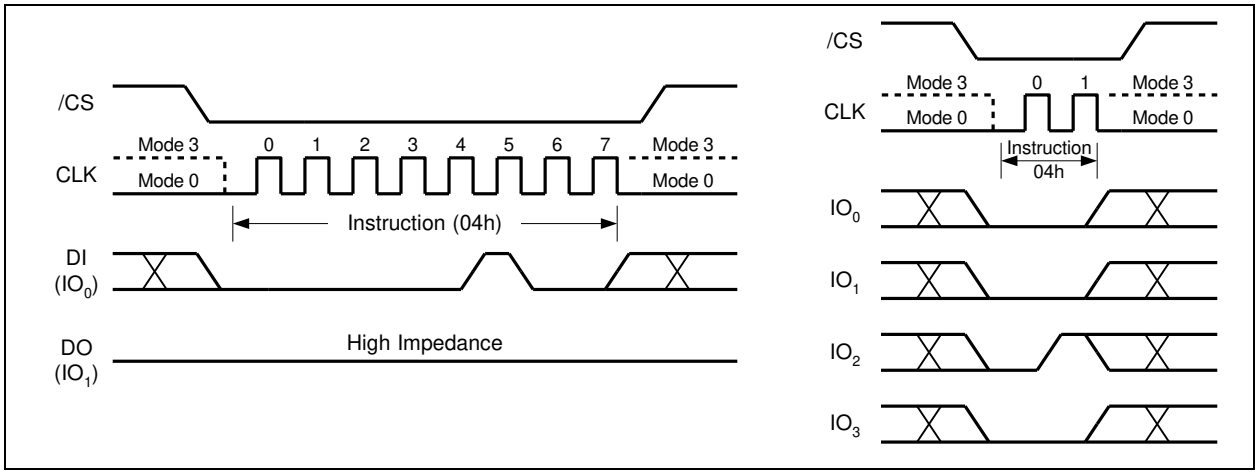

Figure 7. Write Disable Instruction for SPI Mode (left) or QPI Mode (right)