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1M-BIT, 2M-BIT, 4M-BIT AND 8M-BIT SERIAL FLASH MEMORY WITH 4KB SECTORS AND DUAL OUTPUT SPI

winbond

Table of Contents

1. GENERAL DESCRIPTION

The W25X10A (1M-bit), W25X20A (2M-bit), W25X40A (4M-bit) and W25X80A (8M-bit) Serial Flash memories provide a storage solution for systems with limited space, pins and power. The 25X series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code download applications as well as storing voice, text and data. The devices operate on a single 2.7V to 3.6V power supply with current consumption as low as 5mA active and 1µA for power-down. All devices are offered in space-saving packages.

The W25X10A/20A/40A/80A array is organized into 512/1024/2048/4096 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time using the Page Program instruction. Pages can be erased in groups of 16 (sector erase), groups of 256 (block erase) or the entire chip (chip erase). The W25X10A/20A/40A/80A has 32/64/128/256 erasable sectors and 2/4/8/16 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See figure 2.)

The W25X10A/20A/40A/80A supports the standard Serial Peripheral Interface (SPI), and a high performance dual output SPI using four pins: Serial Clock, Chip Select, Serial Data I/O and Serial Data Out. SPI clock frequencies of up to 100MHz are supported allowing equivalent clock rates of 200MHz when using the Fast Read Dual Output instruction. These transfer rates are comparable to those of 8 and 16-bit Parallel Flash memories.

A Hold pin, Write Protect pin and programmable write protect, with top or bottom array control features, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device identification.

2. FEATURES

- **Family of Serial Flash Memories**
  - W25X10A: 1M-bit / 128K-byte (131,072)
  - W25X20A: 2M-bit / 256K-byte (262,144)
  - W25X40A: 4M-bit / 512K-byte (524,288)
  - W25X80A: 8M-bit / 1M-byte (1,048,576)
  - 256-bytes per programmable page
  - Uniform 4K-byte Sectors / 64K-byte Blocks
- **SPI with Single or Dual Outputs**
  - Clock, Chip Select, Data I/O, Data Out
  - Optional Hold function for SPI flexibility
- **Data Transfer up to 200M-bits / second**
  - Clock operation to 100MHz
  - Fast Read Dual Output instruction
  - Auto-increment Read capability
- **Software and Hardware Write Protection**
  - Write-Protect all or portion of memory
  - Enable/Disable protection with /WP pin
  - Top or bottom array protection
- **Flexible Architecture with 4KB sectors**
  - Sector Erase (4K-bytes)
  - Block Erase (64K-byte)
  - Page program up to 256 bytes <2ms
  - More than 100,000 erase/write cycles
  - More than 20-year data retention
- **Low Power Consumption, Wide Temperature Range**
  - Single 2.7 to 3.6V supply
  - 5mA active current, 1µA Power-down (typ)
  - -40° to +85°C operating range
- **Space Efficient Packaging**
  - 8-pin SOIC 150-mil(1)
  - 8-pin SOIC 208-mil (W25X40A/80A)
  - 8-pin PDIP 300-mil
  - 8-pad WSON 6x5-mm

Note 1: See “Valid Part Number and Top Side Marking” Section, Note 2 for special ordering information.

3. PIN CONFIGURATION SOIC 150-MIL

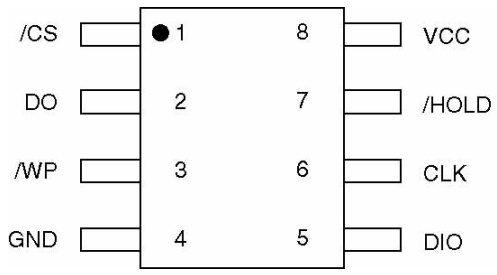

Figure 1a. W25X10A, W25X20A, W25X40A and W25X80A Pin Assignments, 8-pin SOIC (Package Code SN)

4. PIN CONFIGURATION SOIC 208-MIL

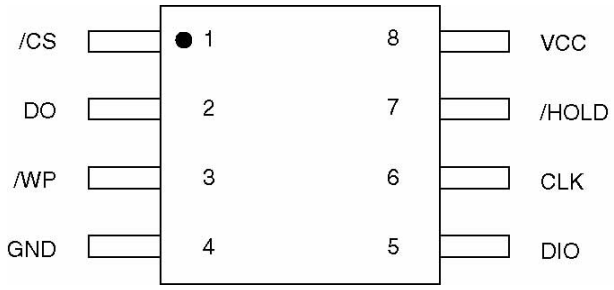

Figure 1b. W25X40A and W25X80A Pin Assignments, 8-pin SOIC (Package Code SS)

5. PIN CONFIGURATION PDIP 300-MIL

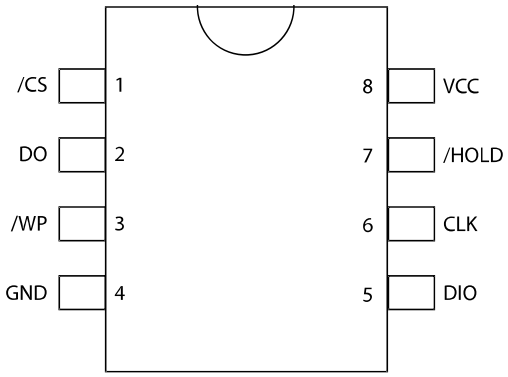

Figure 1c. W25X40A and W25X80A Pin Assignments, 8-pin PDIP (Package Code DA)

6. PAD CONFIGURATION WSON 6X5-MM

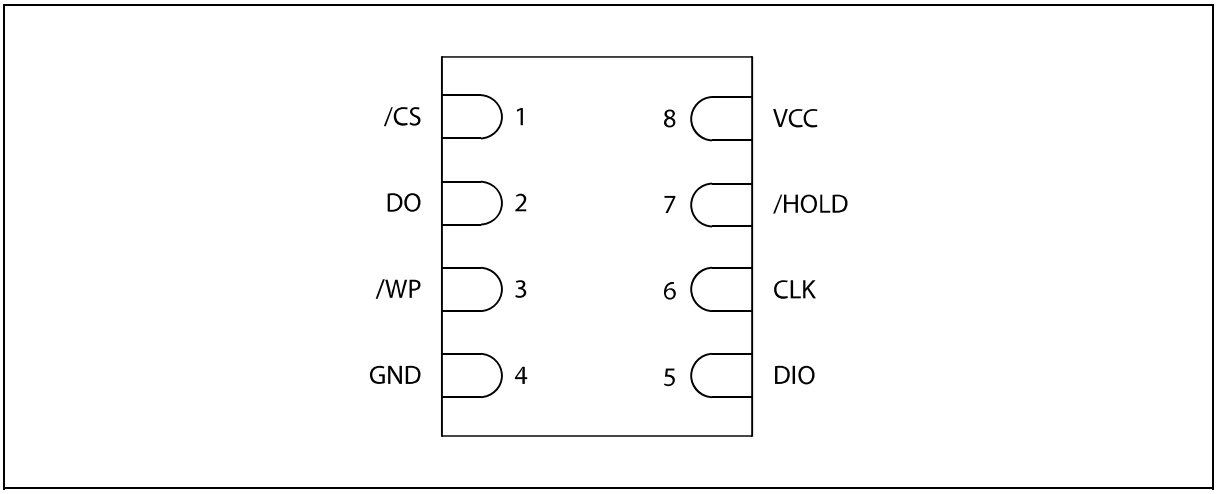

Figure 1d. W25X10A, W25X20A, W25X40A and W25X80A Pad Assignments, 8-pad WSON (Package Code ZP)

7. PIN DESCRIPTION

SOIC 150-mil, SOIC 208-mil, PDIP 300-mil, and WSON 6x5-mm

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO	O	Data Output
3	/WP	I	Write Protect Input
4	GND		Ground
5	DIO	I/O	Data Input / Output
6	CLK	I	Serial Clock Input
7	/HOLD	I	Hold Input
8	VCC		Power Supply

7.1 Package Types

All parts are offered in an 8-pin plastic 150-mil width SOIC (package code SN)(1) as shown in figure 1a and the 8-pad 6x5-mm WSON (package code ZP) as shown in figure 1c, and 1d respectively. The W25X40A and W25X80A are offered in both the 8-pin plastic 208-mil width SOIC (package code SS) as shown in figure 1b and the 8-pin 300-mil DIP (package code DA). Package diagrams and dimensions are illustrated at the end of this datasheet.

7.2 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO) pin is at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up (see "Write Protection" and figure 20). If needed a pull-up resister on /CS can be used to accomplish this.

7.3 Serial Data Output (DO)

The SPI Serial Data Output (DO) pin provides a means for data and status to be serially read from (shifted out of) the device. Data is shifted out on the falling edge of the Serial Clock (CLK) input pin.

7.4 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (BP2, BP1, and BP0) bits and Status Register Protect (SRP) bit, a portion or the entire memory array can be hardware protected. The /WP pin is active low.

7.5 HOLD (/HOLD)

The Hold (/HOLD) pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DIO and CLK pins will be ignored (don't care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. ("See Hold function")

7.6 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

7.7 Serial Data Input / Output (DIO)

The SPI Serial Data Input/Output (DIO) pin provides a means for instructions, addresses and data to be serially written to (shifted into) the device. Data is latched on the rising edge of the Serial Clock (CLK) input pin. The DIO pin is also used as an output when the Fast Read Dual Output instruction is executed.

Note 1: See "Valid Part Number and Top Side Marking" Section, Note 2 for special ordering information.

8. BLOCK DIAGRAM

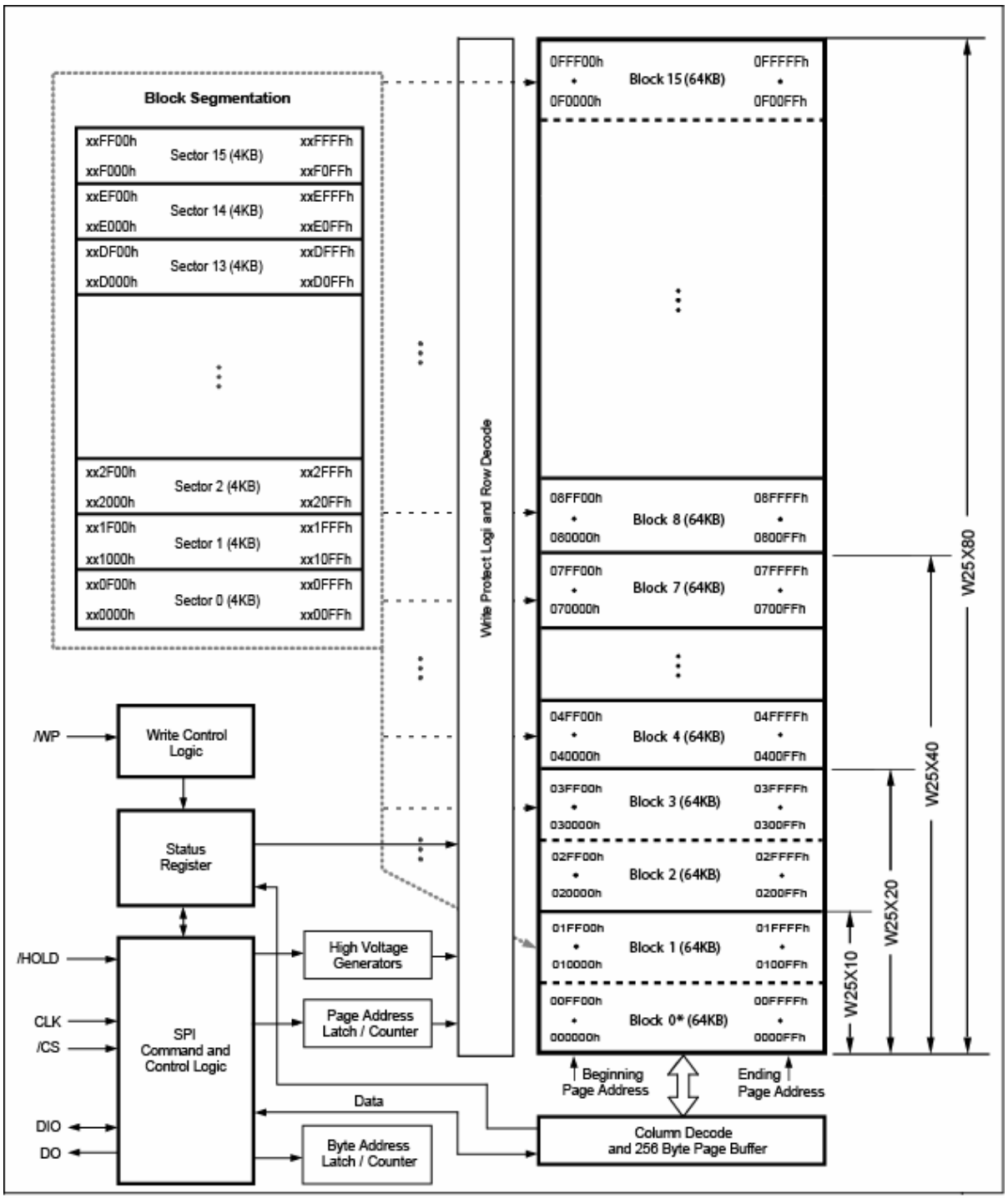

Figure 2. W25X10A, W25X20A, W25X40A and W25X80A Block Diagram

9. FUNCTIONAL DESCRIPTION

9.1 SPI OPERATIONS

9.1.1 SPI Modes

The W25X10A/20A/40A/80A is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input/Output (DIO) and Serial Data Output (DO). Both SPI bus operation Modes 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the CLK signal is normally low. For Mode 3 the CLK signal is normally high. In either case data input on the DIO pin is sampled on the rising edge of the CLK. Data on the DO and DIO pins are clocked out on the falling edge of CLK.

9.1.2 Dual Output SPI

The W25X10A/20A/40A/80A supports Dual output operation when using the “Fast Read with Dual Output” (3B hex) instruction. This feature allows data to be transferred from the Serial Flash memory at twice the rate possible with the standard SPI. This instruction is ideal for quickly downloading code from Flash to RAM upon power-up (code-shadowing) or for applications that cache code-segments to RAM for execution. The Dual output feature simply allows the SPI input pin to also serve as an output during this instruction. All other operations use the standard SPI interface with single output signal.

9.1.3 Hold Function

The /HOLD signal allows the W25X10A/20A/40A/80A operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again.

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will terminate after the next falling edge of CLK.

During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input/Output (DIO) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active (low) for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

9.2 WRITE PROTECTION

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern the W25X10A/20A/40A/80A provides several means to protect data from inadvertent writes.

9.2.1 Write Protect Features

- Device resets when VCC is below threshold.
- Time delay write disable after Power-up.
- Write enable/disable instructions.
- Automatic write disable after program and erase.
- Software write protection using Status Register.
- Hardware write protection using Status Register and /WP pin.
- Write Protection using Power-down instruction.

Upon power-up or at power-down the W25X10A/20A/40A/80A will maintain a reset condition while VCC is below the threshold value of V_{WI}, (See Power-up Timing and Voltage Levels and Figure 20). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds V_{WI}, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP) and Block Protect (TB, BP2, BP1, and BP0) bits. These Status Register bits allow a portion or all of the memory to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register for further information.

Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

10. CONTROL AND STATUS REGISTERS

The Read Status Register instruction can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled, and the state of write protection. The Write Status Register instruction can be used to configure the device write protection features. See Figure 3.

10.1 STATUS REGISTER

10.1.1 BUSY

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction. During this time the device will ignore further instructions except for the Read Status Register instruction (see t_W, t_{PP}, t_{SE}, t_{BE}, and t_{CE} in AC Characteristics). When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

10.1.2 Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to a 1 after executing a Write Enable Instruction. The WEL status bit is cleared to a 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register.

10.1.3 Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, and BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see t_W in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected. The Block Protect bits can not be written to if the Status Register Protect (SRP) bit is set to 1 and the Write Protect (/WP) pin is low.

10.1.4 Top/Bottom Block Protect (TB)

The Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The TB bit is non-volatile and the factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction provided that the Write Enable instruction has been issued. The TB bit can not be written to if the Status Register Protect (SRP) bit is set to 1 and the Write Protect (/WP) pin is low.

10.1.5 Reserved Bits

Status register bit location S6 is reserved for future use. Current devices will read 0 for this bit location. It is recommended to mask out the reserved bit when testing the Status Register. Doing this will ensure compatibility with future devices.

10.1.6 Status Register Protect (SRP)

The Status Register Protect (SRP) bit is a non-volatile read/write bit in status register (S7) that can be used in conjunction with the Write Protect (/WP) pin to disable writes to status register. When the SRP bit is set to a 0 state (factory default) the /WP pin has no control over status register. When the SRP pin is set to a 1, the Write Status Register instruction is locked out while the /WP pin is low. When the /WP pin is high the Write Status Register instruction is allowed.

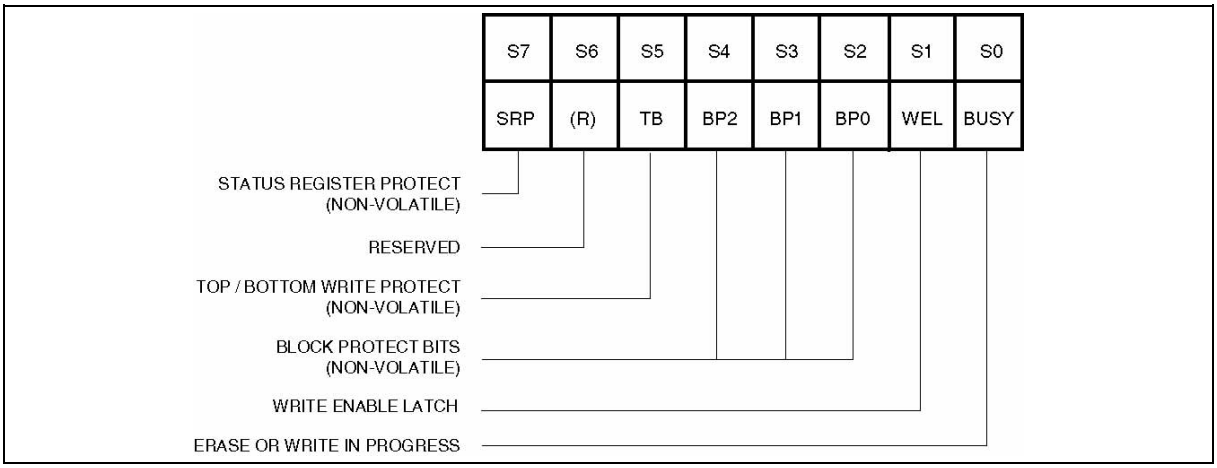

Figure 3. Status Register Bit Locations

10.1.7 Status Register Memory Protection

STATUS REGISTER(1)				W25X80A (8M-BIT) MEMORY PROTECTION			
TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
x	0	0	0	NONE	NONE	NONE	NONE
0	0	0	1	15	0F0000h - 0FFFFFh	64KB	Upper 1/16
0	0	1	0	14 and 15	0E0000h - 0FFFFFh	128KB	Upper 1/8
0	0	1	1	12 thru 15	0C0000h - 0FFFFFh	256KB	Upper 1/4
0	1	0	0	8 thru 15	080000h - 0FFFFFh	512KB	Upper 1/2
1	0	0	1	0	000000h - 00FFFFh	64KB	Lower 1/16
1	0	1	0	0 and 1	000000h - 01FFFFh	128KB	Lower 1/8
1	0	1	1	0 thru 3	000000h - 03FFFFh	256KB	Lower 1/4
1	1	0	0	0 thru 7	000000h - 07FFFFh	512KB	Lower 1/2
x	1	0	1	0 thru 15	000000h - 0FFFFFh	1MB	ALL
x	1	1	x	0 thru 15	000000h - 0FFFFFh	1MB	ALL

STATUS REGISTER(1)				W25X40A (4M-BIT) MEMORY PROTECTION			
TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
x	0	0	0	NONE	NONE	NONE	NONE
0	0	0	1	7	070000h - 07FFFFh	64KB	Upper 1/8
0	0	1	0	6 and 7	060000h - 07FFFFh	128KB	Upper 1/4
0	0	1	1	4 thru 7	040000h - 07FFFFh	256KB	Upper 1/2
1	0	0	1	0	000000h - 00FFFFh	64KB	Lower 1/8
1	0	1	0	0 and 1	000000h - 01FFFFh	128KB	Lower 1/4
1	0	1	1	0 thru 3	000000h - 03FFFFh	256KB	Lower 1/2
x	1	x	x	0 thru 7	000000h - 07FFFFh	512KB	ALL

STATUS REGISTER(1)				W25X20A (2M-BIT) MEMORY PROTECTION			
TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
x	x	0	0	NONE	NONE	NONE	NONE
0	x	0	1	3	030000h - 03FFFFh	64KB	Upper 1/4
0	x	1	0	2 and 3	020000h - 03FFFFh	128KB	Upper 1/2
1	x	0	1	0	000000h - 00FFFFh	64KB	Lower 1/4
1	x	1	0	0 and 1	000000h - 01FFFFh	128KB	Lower 1/2
x	x	1	1	0 thru 3	000000h - 03FFFFh	256KB	ALL

STATUS REGISTER(1)				W25X10A (1M-BIT) MEMORY PROTECTION			
TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
x	x	0	0	NONE	NONE	NONE	NONE
0	x	0	1	1	010000h - 01FFFFh	64KB	Upper 1/2
1	x	0	1	0	000000h - 00FFFFh	64KB	Lower 1/2
x	x	1	x	0 and 1	000000h - 01FFFFh	128KB	ALL

Note: x = don't care

10.2 INSTRUCTIONS

The instruction set of the W25X10A/20A/40A/80A consists of fifteen basic instructions that are fully controlled through the SPI bus (see Instruction Set table). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DIO input provides the instruction code. Data on the DIO input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in figures 4 through 19. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (CS driven high after a full 8-bits have been clocked) otherwise the instruction will be terminated. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

10.2.1 Manufacturer and Device Identification

MANUFACTURER ID	**(M7-M0)**	
Winbond Serial Flash	EFh	
Device ID	**(ID7-ID0)**	**(ID15-ID0)**
Instruction	**ABh, 90h**	**9Fh**
W25X10A	10h	3011h
W25X20A	11h	3012h
W25X40A	12h	3013h
W25X80A	13h	3014h

10.2.2 Instruction Set [1]

INSTRUCTION NAME	BYTE 1 CODE	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	N-BYTES
Write Enable	06h						
Write Disable	04h						
Read Status Register	05h	(S7–S0)[1]					[2]
Write Status Register	01h	S7–S0					
Read Data	03h	A23–A16	A15–A8	A7–A0	(D7–D0)	(Next byte)	continuous
Fast Read	0Bh	A23–A16	A15–A8	A7–A0	dummy	(D7–D0)	(Next Byte) continuous
Fast Read Dual Output	3Bh	A23–A16	A15–A8	A7–A0	dummy	I/O = (D6,D4,D2,D0) O = (D7,D5,D3,D1)	(one byte per 4 clocks, continuous)
Page Program	02h	A23–A16	A15–A8	A7–A0	(D7–D0)	(Next byte)	Up to 256 bytes
Block Erase (64KB)	D8h	A23–A16	A15–A8	A7–A0			
Sector Erase (4KB)	20h	A23–A16	A15–A8	A7–A0			
Chip Erase	C7h/60h						
Power-down	B9h						
Release Power-down / Device ID	ABh	dummy	dummy	dummy	(ID7-ID0)[4]		
Manufacturer/ Device ID [3]	90h	dummy	dummy	00h	(M7-M0)	(ID7-ID0)	
JEDEC ID	9Fh	(M7-M0) Manufacturer	(ID15-ID8) Memory Type	(ID7-ID0) Capacity			

Notes:
1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data being read from the device on the DO pin.
2. The Status Register contents will repeat continuously until /CS terminates the instruction.
3. See Manufacturer and Device Identification table for Device ID information.
4. The Device ID will repeat continuously until /CS terminates the instruction.

10.2.3 Write Enable (06h)

The Write Enable instruction (Figure 4) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code "06h" into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

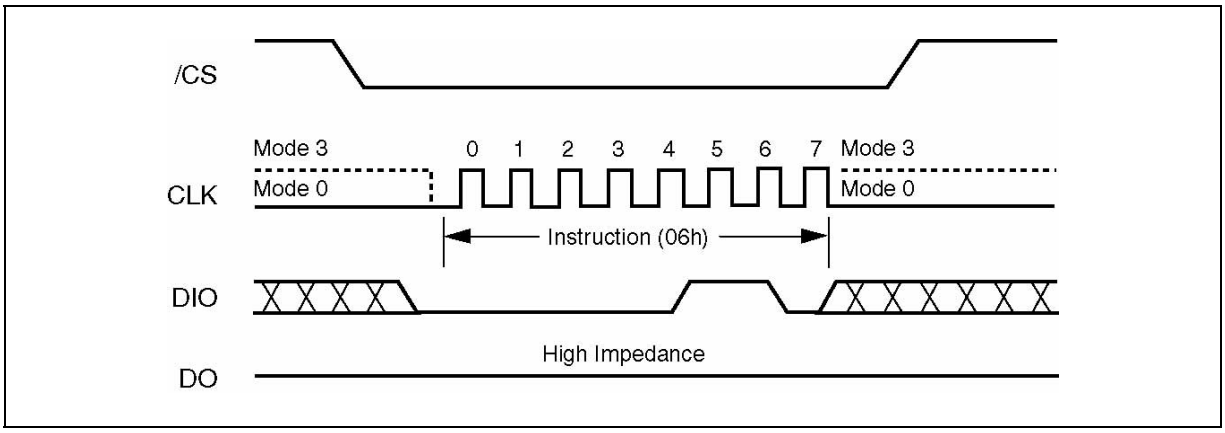

Figure 4. Write Enable Instruction Sequence Diagram

10.2.4 Write Disable (04h)

The Write Disable instruction (Figure 5) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code "04h" into the DIO pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase instructions.

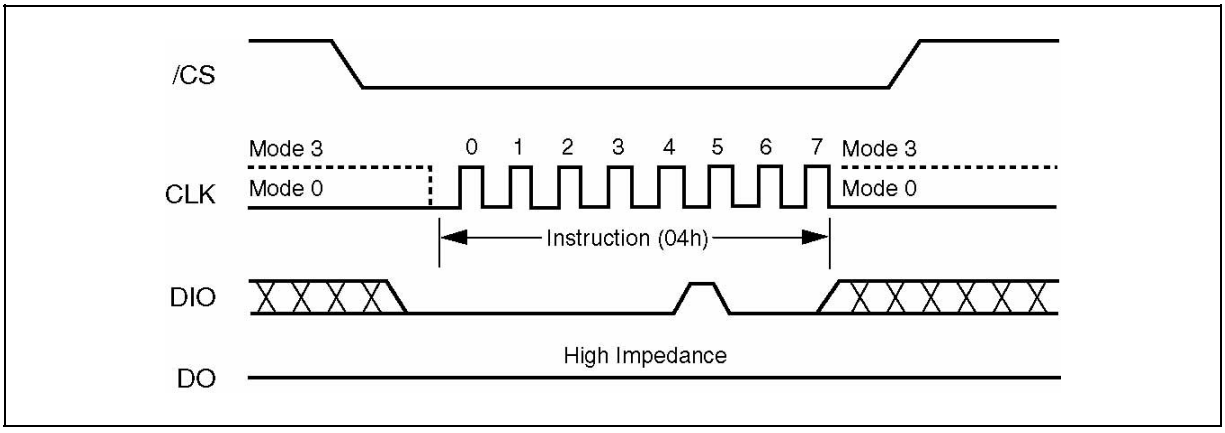

Figure 5. Write Disable Instruction Sequence Diagram

10.2.5 Read Status Register (05h)

The Read Status Register instruction allows the 8-bit Status Register to be read. The instruction is entered by driving /CS low and shifting the instruction code “05h” into the DIO pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in figure 6. The Status Register bits are shown in figure 3 and include the BUSY, WEL, BP2-BP0, TB and SRP bits (see description of the Status Register earlier in this datasheet).

The Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 6. The instruction is completed by driving /CS high.

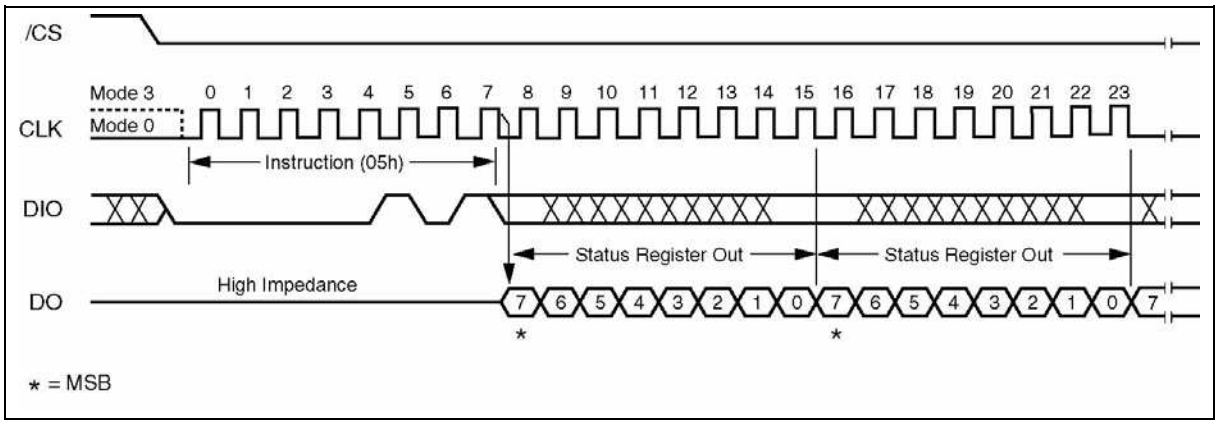

Figure 6. Read Status Register Instruction Sequence Diagram

10.2.6 Write Status Register (01h)

The Write Status Register instruction allows the Status Register to be written. A Write Enable instruction must previously have been executed for the device to accept the Write Status Register Instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code “01h”, and then writing the status register data byte as illustrated in figure 7. The Status Register bits are shown in figure 3 and described earlier in this datasheet.

Only non-volatile Status Register bits SRP, TB, BP2, BP1 and BP0 (bits 7, 5, 4, 3 and 2) can be written to. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Write Status Register instruction will not be executed. After /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of tW (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

The Write Status Register instruction allows the Block Protect bits (TB, BP2, BP1 and BP0) to be set for protecting all, a portion, or none of the memory from erase and program instructions. Protected areas become read-only (see Status Register Memory Protection table). The Write Status Register instruction also allows the Status Register Protect bit (SRP) to be set. This bit is used in conjunction with the Write Protect (/WP) pin to disable writes to the status register. When the SRP bit is set to a 0 state (factory default) the /WP pin has no control over the status register. When the SRP pin is set to a 1, the Write Status Register instruction is locked out while the /WP pin is low. When the /WP pin is high the Write Status Register instruction is allowed.

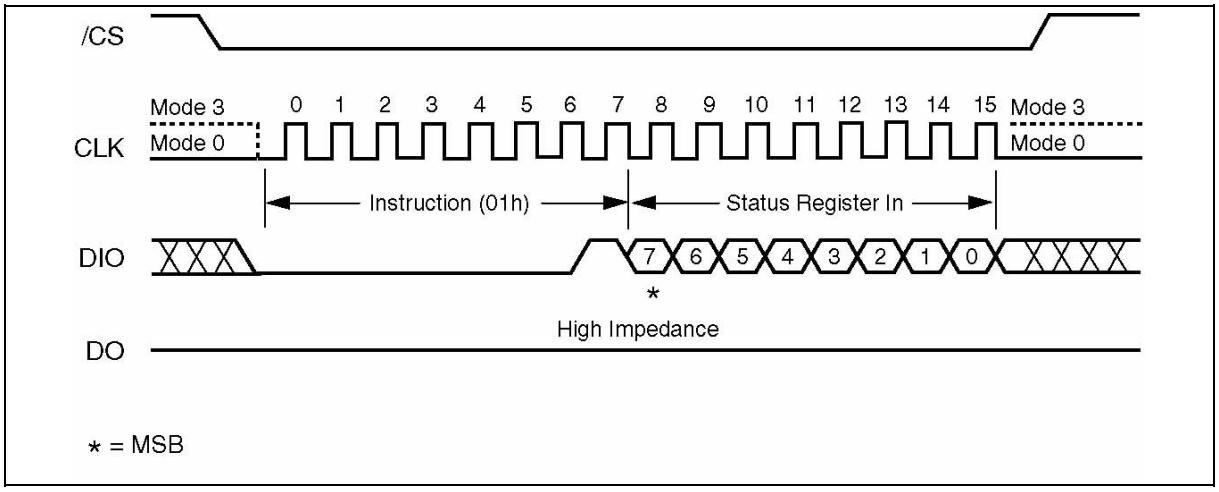

Figure 7. Write Status Register Instruction Sequence Diagram

10.2.7 Read Data (03h)

The Read Data instruction allows one more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DIO pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high. The Read Data instruction sequence is shown in figure 8. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (see AC Electrical Characteristics).

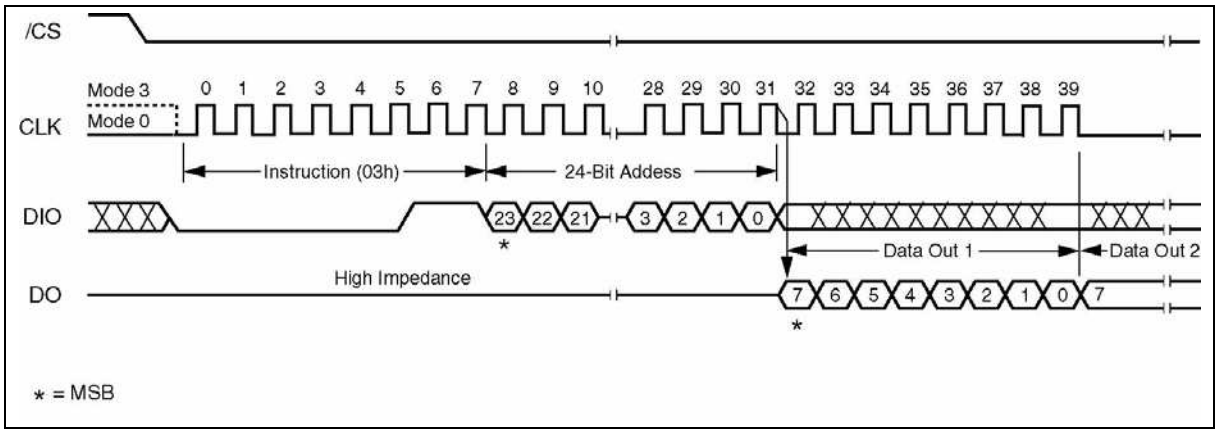

Figure 8. Read Data Instruction Sequence Diagram

10.2.8 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in figure 9. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DIO pin is a “don’t care”.

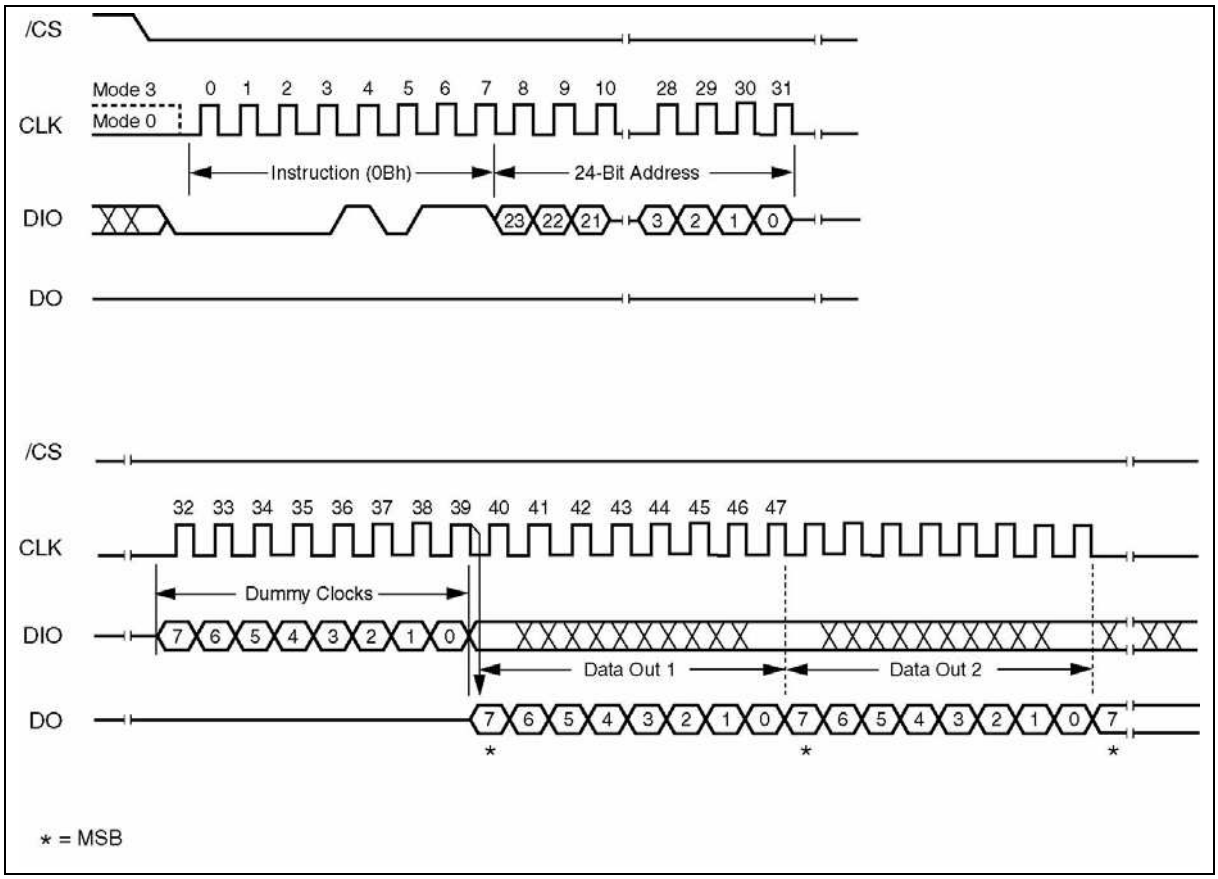

Figure 9. Fast Read Instruction Sequence Diagram

10.2.9 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins, DO and DIO, instead of just DO. This allows data to be transferred from the W25X10A/20A/40A/80A at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of F_R (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in figure 10. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the DIO pin should be high-impedance prior to the falling edge of the first data out clock.

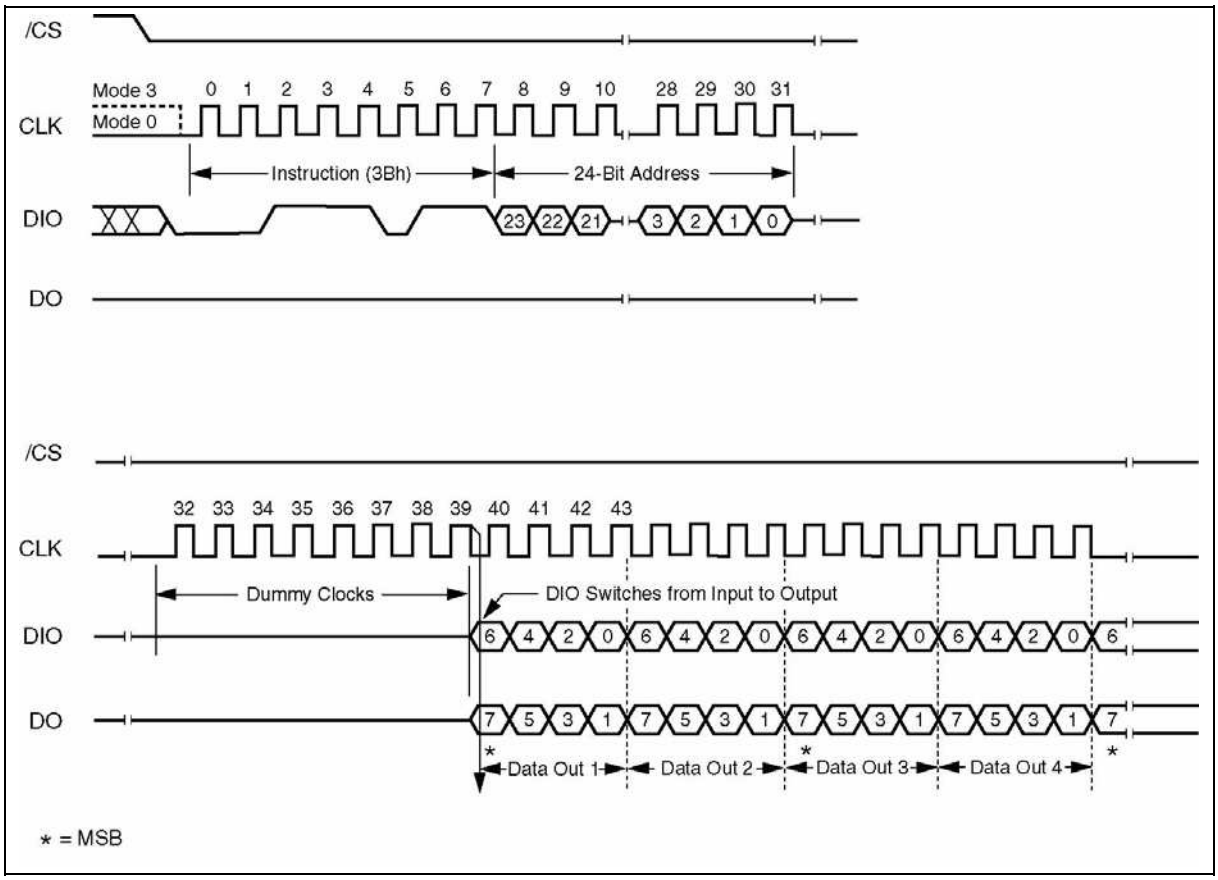

Figure 10. Fast Read Dual Output Instruction Sequence Diagram

10.2.10 Page Program (02h)

The Page Program instruction allows up to 256 bytes of data to be programmed at previously erased to all 1s (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DIO pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceed the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks can not exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of tpp (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

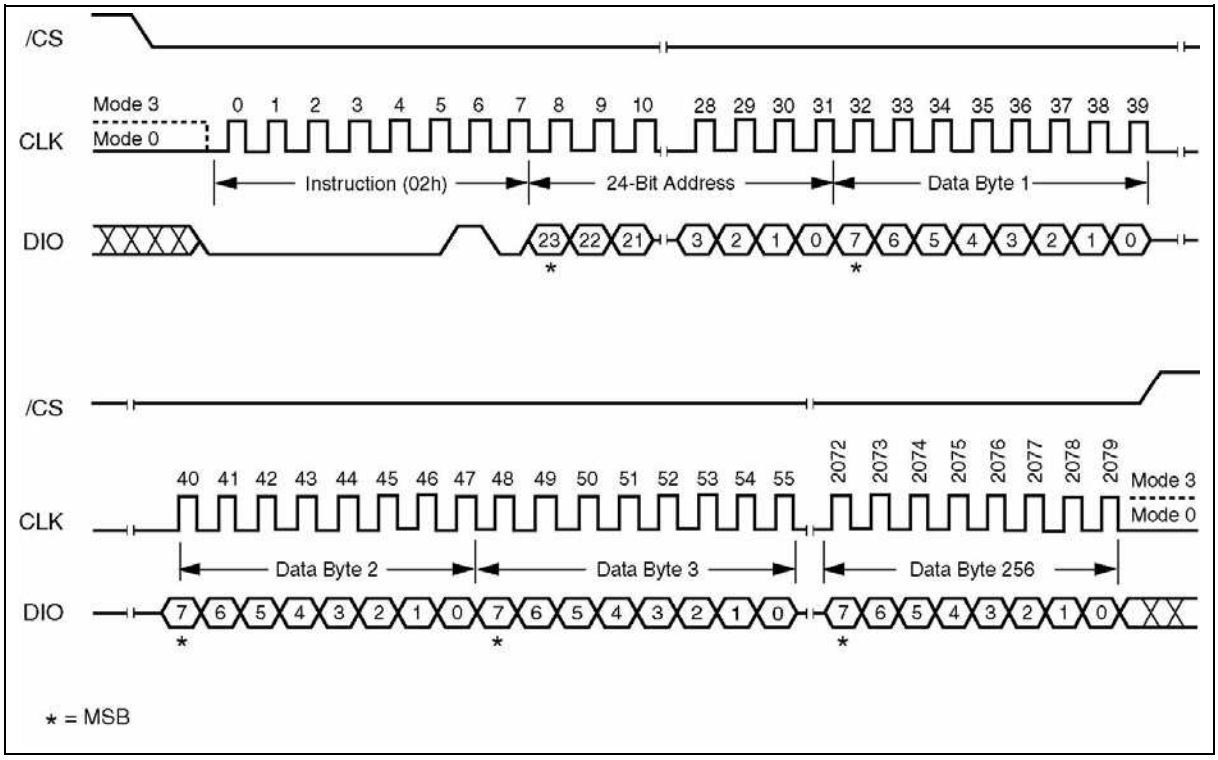

Figure 11. Page Program Instruction Sequence Diagram

10.2.11 Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "20h" followed a 24-bit sector address (A23-A0) (see Figure 2). The Sector Erase instruction sequence is shown in figure 12.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of t_{SE} (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

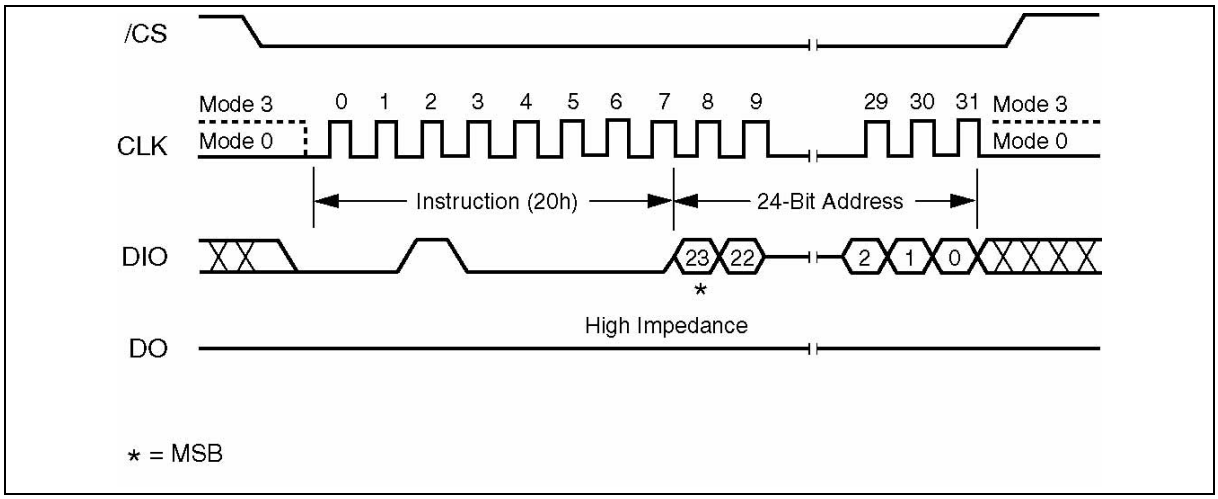

Figure 12. Sector Erase Instruction Sequence Diagram

10.2.12 Block Erase (D8h)

The Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "D8h" followed a 24-bit block address (A23-A0) (see Figure 2). The Block Erase instruction sequence is shown in figure 13.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE} (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

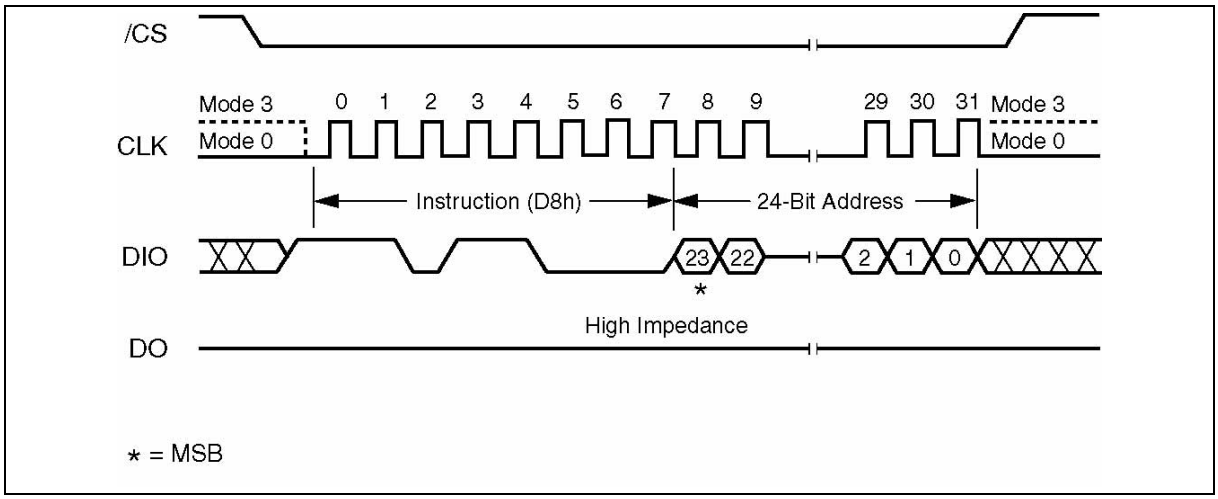

Figure 13. Block Erase Instruction Sequence Diagram

10.2.13 Chip Erase (C7h or 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in figure 14.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of t_{CE} (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any page is protected by the Block Protect (BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

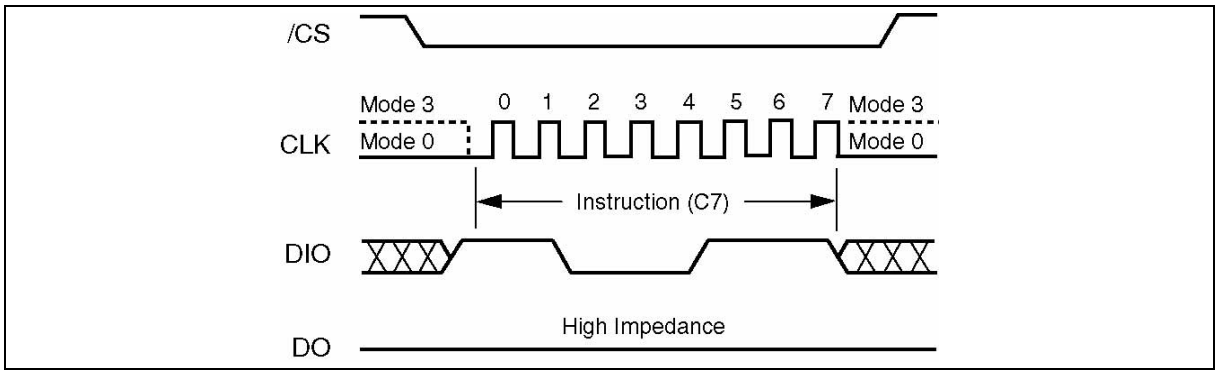

Figure 14. Chip Erase Instruction Sequence Diagram