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W25X10CL



2.5 / 3 / 3.3 V

1M-BIT

**SERIAL FLASH MEMORY WITH
4KB SECTORS AND DUAL I/O SPI**



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1. GENERAL DESCRIPTION

The W25X10CL (1M-bit) Serial Flash memories provide a storage solution for systems with limited space, pins and power. The 25X series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code download applications as well as storing voice, text and data. The devices operate on a single 2.3V to 3.6V power supply with current consumption as low as 1mA active and 1 μ A for power-down. All devices are offered in space-saving packages.

The W25X10CL arrays are organized into 512 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. The W25X10CL have 32 erasable sectors, 4 erasable 32KB blocks and 2 erasable 64KB blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See figure 2.)

The W25X10CL support the standard Serial Peripheral Interface (SPI), and a high performance dual output as well as Dual I/O SPI: Serial Clock, Chip Select, Serial Data DI (I/O0), DO (I/O1). SPI clock frequencies up to 104MHz are supported allowing equivalent clock rates of 208MHz when using the Fast Read Dual Output instruction. These transfer rates are comparable to those of 8 and 16-bit Parallel Flash memories. The Continuous Read Mode allows for efficient memory access with as few as 16-clocks of instruction-overhead to read a 24-bit address, allowing true XIP (execute in place) operation.

A Hold pin, Write Protect pin and programmable write protect, with top or bottom array control features, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device identification with a 64-bit Unique Serial Number.

2. FEATURES

- **Family of Serial Flash Memories**
 - W25X10CL: 1M-bit/128K-byte (131,072)
 - 256-bytes per programmable page
 - Uniform erasable 4KB, 32KB & 64KB regions.
- **SPI with Single / Dual Outputs / I/O**
 - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
 - Dual SPI: CLK, /CS, IO0, IO1, /WP, /Hold
- **Data Transfer up to 208M-bits / second**
 - Clock operation to 104MHz
 - 208MHz equivalent Dual I/O SPI
 - Auto-increment Read capability
- **Efficient “Continuous Read Mode”**
 - Low Instruction overhead
 - Continuous Read
 - As few as 16 clocks to address memory
 - Allows true XIP (execute in place) operation
- **Software and Hardware Write Protection**
 - Write-Protect all or portion of memory
 - Enable/Disable protection with /WP pin
 - Top or bottom array protection
- **Flexible Architecture with 4KB sectors**
 - Uniform Sector/Block Erase (4/32/64-kbytes)
 - Page program up to 256 bytes <1ms
 - More than 100,000 erase/write cycles
 - More than 20-year data retention
- **Low Power, Wide Temperature Range**
 - Single 2.3V to 3.6V supply
 - 1mA active current, <1 μ A Power-down(typ.)
 - -40° to +85°C operating range
- **Space Efficient Packaging**
 - 8-pin SOIC
 - 8-pad USON 2x3-mm
 - Contact Winbond for KGD and other options



3. PIN CONFIGURATION SOIC 150-MIL

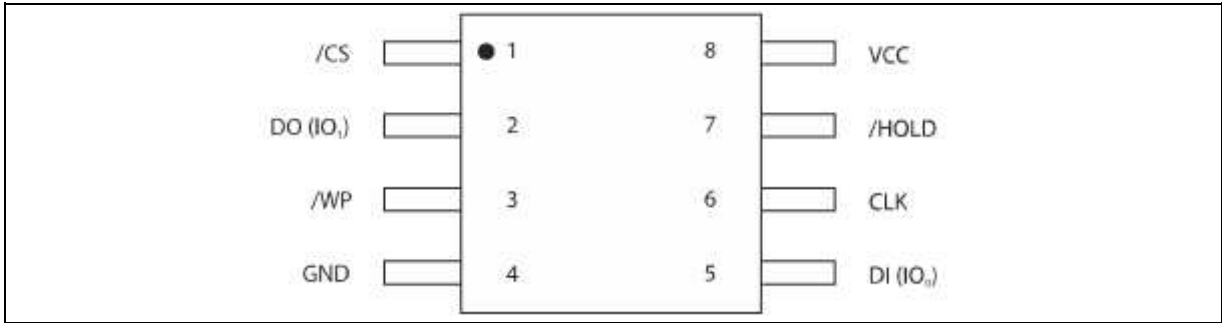


Figure 1a. W25X10CL Pin Assignments, 8-pin SOIC 150-mil (Package Code SN)

4. PAD CONFIGURATION USON 2X3-MM

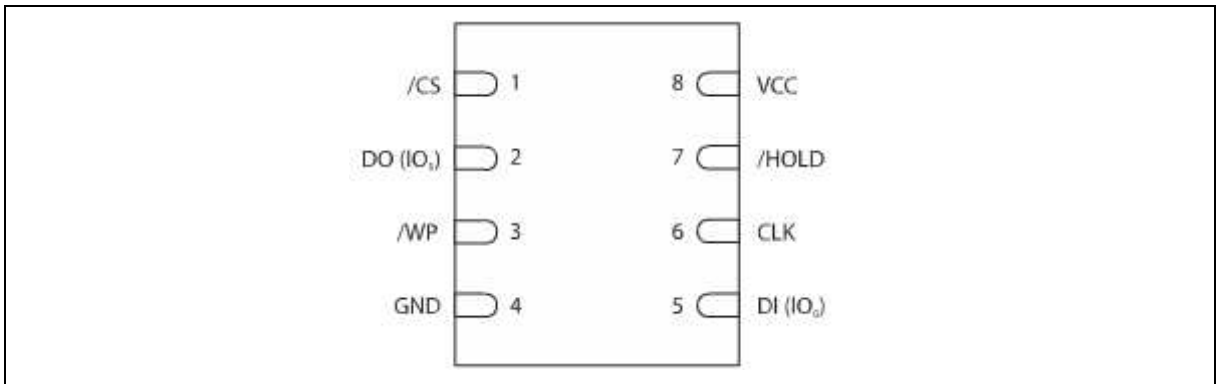


Figure 1b. W25X10CL Pad Assignments USON 2x3-MM (Package Code UX)

5. PIN DESCRIPTION SOIC AND USON 2X3-MM

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Input / Output ⁽¹⁾
3	/WP	I	Write Protect Input
4	GND		Ground
5	DI (IO0)	I/O	Data Input / Output ⁽¹⁾
6	CLK	I	Serial Clock Input
7	/HOLD	I	Hold Input
8	VCC		Power Supply

Note:

1 IO0 and IO1 are used for Standard and Dual SPI instructions



5.1 Package Types

W25X10CL are offered in 8-pin plastic 150-mil width SOIC (package code SN), and 2x3-mm USON (package code UX). Refer to see figures 1a and 1b, respectively.

5.2 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up (see "Power-up Timing and Write inhibit threshold" and Figure 26). If needed, a pull-up resistor on /CS can be used to accomplish this.

5.3 Serial Data Input, Output and IOs (DI, DO, IO0 and IO1)

The W25X10CL support standard SPI and Dual SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.

5.4 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (TB, BP1 and BP0) bits and Status Register Protect (SRP) bit, a portion or the entire memory array can be hardware protected. The /WP pin is active low.

5.5 HOLD (/HOLD)

The Hold (/HOLD) pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals.

5.6 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations.



6. BLOCK DIAGRAM

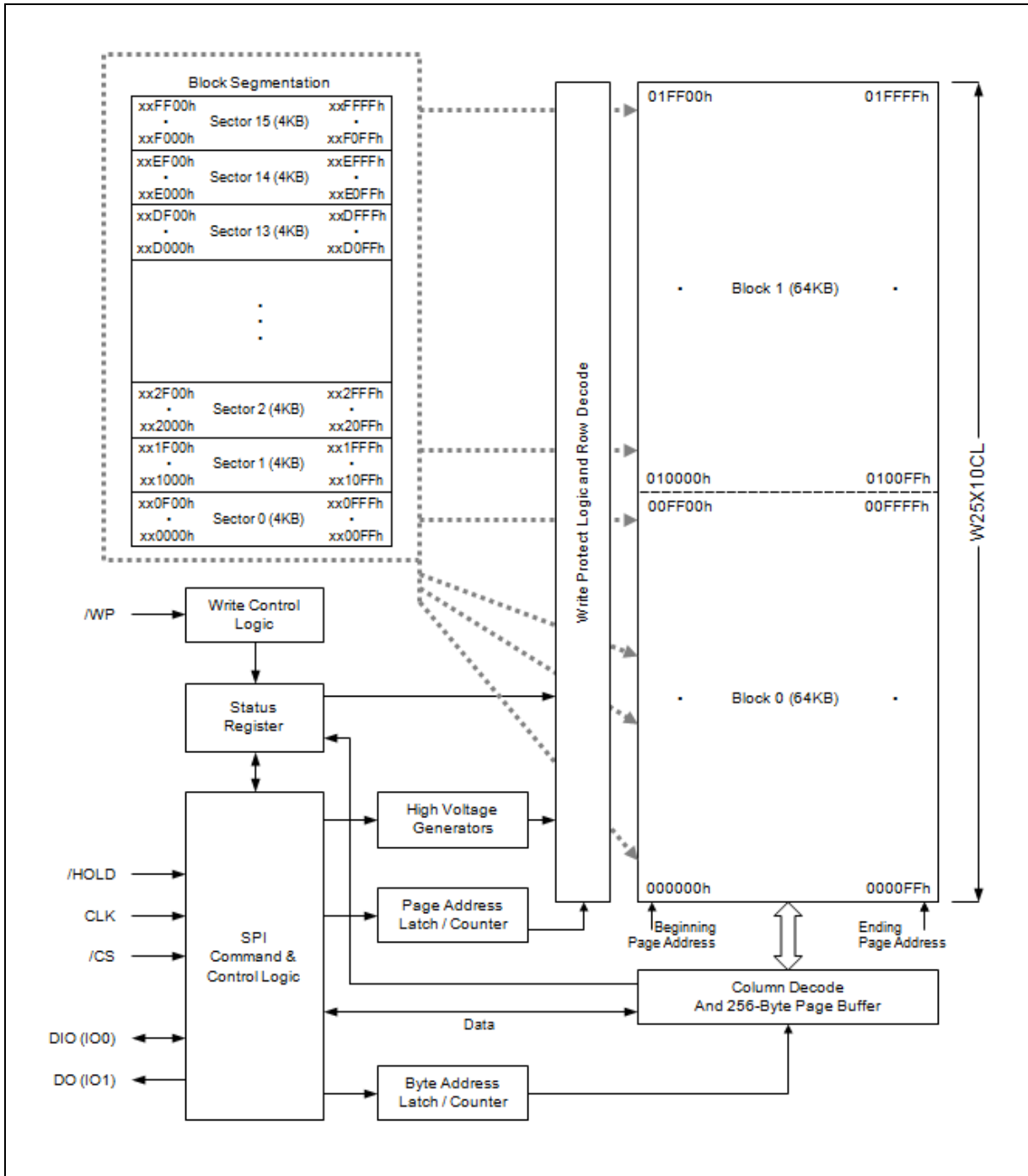


Figure 2. W25X10CL Serial Flash Memory Block Diagram



7. FUNCTIONAL DESCRIPTION

7.1 SPI OPERATIONS

7.1.1 Standard SPI Instructions

The W25X10CL are accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge CLK.

SPI bus operation Modes 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3 the CLK signal is normally high on the falling and rising edges of /CS.

7.1.2 Dual SPI Instructions

The W25X10CL support Dual SPI operation when using the “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)” instructions. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

7.1.3 Hold Function

The /HOLD signal allows the W25X10CL operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again.

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will terminate after the next falling edge of CLK.

During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input/Output (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active (low) for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.



7.2 WRITE PROTECTION

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the W25X10CL provide several means to protect data from inadvertent writes.

7.2.1 Write Protect Features

- Device resets when VCC is below threshold.
- Time delay write disable after Power-up.
- Write enable/disable instructions.
- Automatic write disable after program and erase.
- Software and Hardware (/WP pin) write protection using Status Register.
- Write Protection using Power-down instruction.

Upon power-up or at power-down, the W25X10CL will maintain a reset condition while VCC is below the threshold value of V_{WI} , (See Power-up Timing and Voltage Levels and Figure 26). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds V_{WI} , all program and erase related instructions are further disabled for a time delay of t_{PUW} . This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached. If needed, a pull-up resistor on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP) and Block Protect (TB, BP1 and BP0) bits. These allow a portion small as 4KB sector or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.



8. CONTROL AND STATUS REGISTERS

The Read Status Register instruction can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled, and the state of write protection. The Write Status Register instruction can be used to configure the device write protection features.

8.1 STATUS REGISTER

8.1.1 BUSY

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction. During this time the device will ignore further instructions except for the Read Status Register instruction (see *tw*, *tPP*, *tSE*, *tBE*, and *tCE* in AC Characteristics). When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

8.1.2 Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to a 1 after executing a Write Enable Instruction. The WEL status bit is cleared to a 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions finished: Write Disable, Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register.

8.1.3 Block Protect Bits (BP1, BP0)

The Block Protect Bits (BP1 and BP0) are non-volatile read/write bits in the status register (S3 and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see *tw* in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected. The Block Protect bits cannot be written to if the Status Register Protect (SRP) bit is set to 1 and the Write Protect (/WP) pin is low.

8.1.4 Top/Bottom Block Protect (TB)

The Top/Bottom bit (TB) controls if the Block Protect Bits (BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The TB bit is non-volatile and the factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction provided that the Write Enable instruction has been issued. The TB bit cannot be written to if the Status Register Protect (SRP) bit is set to 1 and the Write Protect (/WP) pin is low.



8.1.5 Reserved Bits

Status register bit location S6 and S4 are reserved for future use. Current devices will read 0 for this bit location. It is recommended to mask out the reserved bit when testing the Status Register. Doing this will ensure compatibility with future devices.

8.1.6 Status Register Protect (SRP)

The Status Register Protect (SRP) bit is a non-volatile read/write bit in status register (S7) that can be used in conjunction with the Write Protect (/WP) pin to disable writes to status register. When the SRP bit is set to a 0 state (factory default) the /WP pin has no control over status register. When the SRP pin is set to a 1, the Write Status Register instruction is locked out while the /WP pin is low. When the /WP pin is high the Write Status Register instruction is allowed.

SRP	/WP	Status Register	Description
0	X	Software Protection	/WP pin has no control, The Status register can be written to after a Write Enable instruction WEL = 1. [Factory Default]
1	0	Hardware Protected	When /WP pin is low the Status Register locked and can't be written to.
1	1	Hardware Unprotected	When /WP pin is high the status register is unlocked and can be written to after a Write Enable instruction WEL = 1.

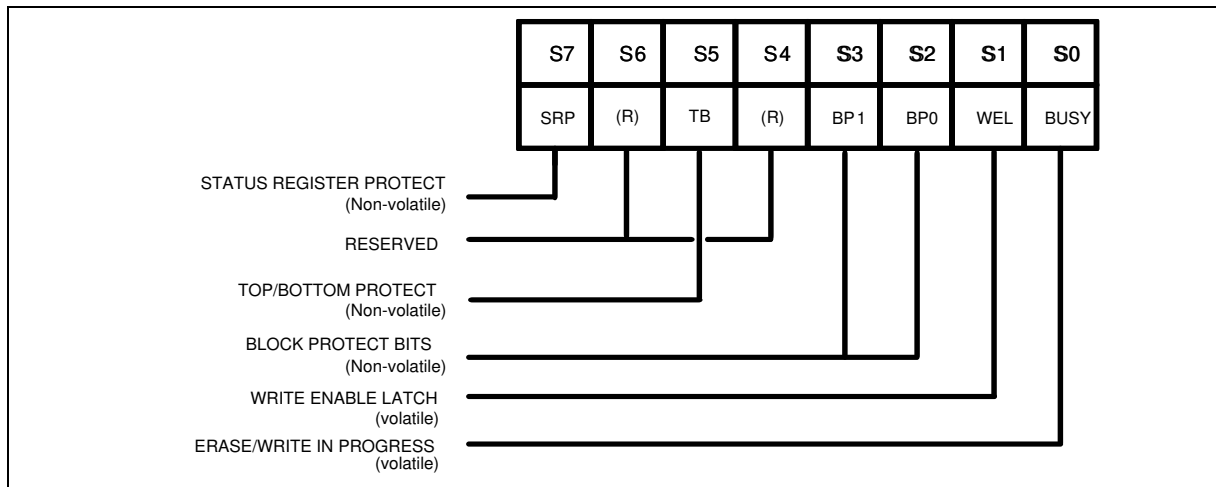


Figure 3. Status Register Bit Locations



8.1.7 Status Register Memory Protection

STATUS REGISTER ⁽¹⁾			W25X10CL (1M-BIT) MEMORY PROTECTION			
TB	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
x	0	0	NONE	NONE	NONE	NONE
0	0	1	1	010000h - 01FFFFh	64KB	Upper 1/2
1	0	1	0	000000h - 00FFFFh	64KB	Lower 1/2
x	1	x	0 and 1	000000h - 01FFFFh	128KB	ALL

Note:

1. x = don't care
2. If any erase or program command specifies a memory region that contains protected data portion, this command will be ignore.

**INSTRUCTIONS**

The instruction set of the W25X10CL consists of twenty basic instructions that are fully controlled through the SPI bus (see Instruction Set table). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in figures 4 through 25. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (CS driven high after a full 8-bits have been clocked) otherwise the instruction will be terminated. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

8.1.8 Manufacturer and Device Identification

MANUFACTURER ID	(M7-M0)	
Winbond Serial Flash	EFh	
Device ID	(ID7-ID0)	(ID15-ID0)
Instruction	ABh, 90h, 92h	9Fh
W25X10CL	10h	3011h



8.1.9 Instruction Set ⁽¹⁾

INSTRUCTION NAME	BYTE 1 (CODE)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	N-BYTES
Write Enable	06h						
Write Enable for Volatile Status Register	50h						
Write Disable	04h						
Read Status Register	05h	(S7-S0) ⁽¹⁾					(2)
Write Status Register	01h	(S7-S0)					
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	continuous
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(Next Byte) continuous
Fast Read Dual Output	3Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0, ...) ⁽⁵⁾	(one byte per 4 clocks, continuous)
Fast Read Dual I/O	BBh	A23-A8 ⁽⁶⁾	A7-A0, M7-M0 ⁽⁶⁾	(D7-D0, ...) ⁽⁵⁾			
Page Program	02h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	Up to 256 bytes
Sector Erase (4KB)	20h	A23-A16	A15-A8	A7-A0			
Block Erase (32KB)	52h	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	D8h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/60h						
Power-down	B9h						
Release Power-down / Device ID	ABh	dummy	dummy	dummy	(ID7-ID0) ⁽⁴⁾		
Manufacturer/ Device ID ⁽³⁾	90h	dummy	dummy	00h	(M7-M0)	(ID7-ID0)	
Manufacturer/Device ID by Dual I/O	92h	A23-A8	A7-A0, M[7:0]	(MF[7:0], ID[7:0])			
JEDEC ID	9Fh	(M7-M0) Manufacturer	(ID15-ID8) Memory Type	(ID7-ID0) Capacity			
Read Unique ID	4Bh	dummy	dummy	dummy	dummy	(ID63-ID0)	

Notes:

- 1 Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “()” indicate data being read from the device on the DO pin.
- 2 The Status Register contents will repeat continuously until /CS terminates the instruction.
- 3 See Manufacturer and Device Identification table for Device ID information.
- 4 The Device ID will repeat continuously until /CS terminates the instruction.
- 5 Dual Output and Dual I/O data
 IO0 = (D6, D4, D2, D0)
 IO1 = (D7, D5, D3, D1)
- 6 Dual Input Address
 IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
 IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1



8.1.10 Write Enable (06h)

The Write Enable instruction (Figure 4) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

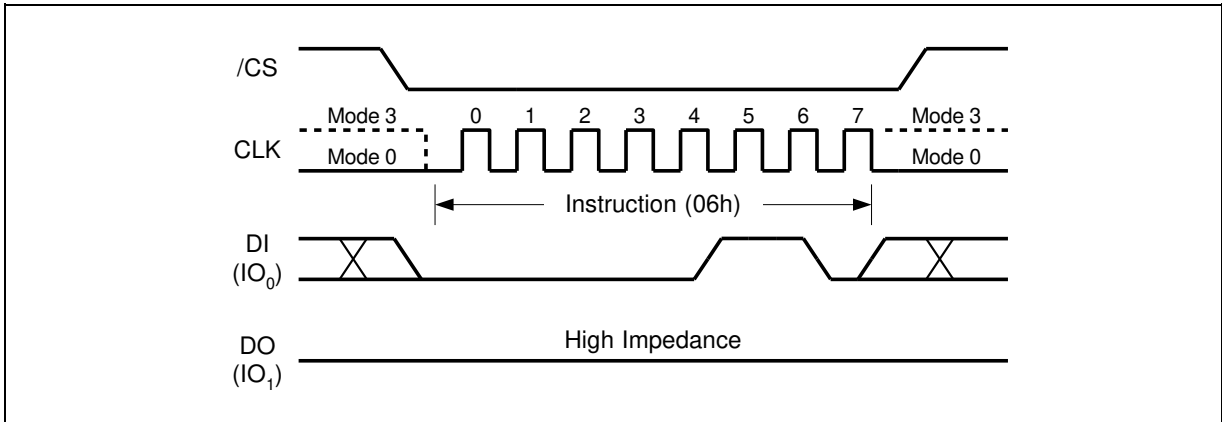


Figure 4. Write Enable Instruction Sequence Diagram

8.1.11 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in section 8.1 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction. Write Enable for Volatile Status Register instruction (Figure 5) will not set the Write Enable Latch (WEL) bit, it is only valid for the Write Status Register instruction to change the volatile Status Register bit values.

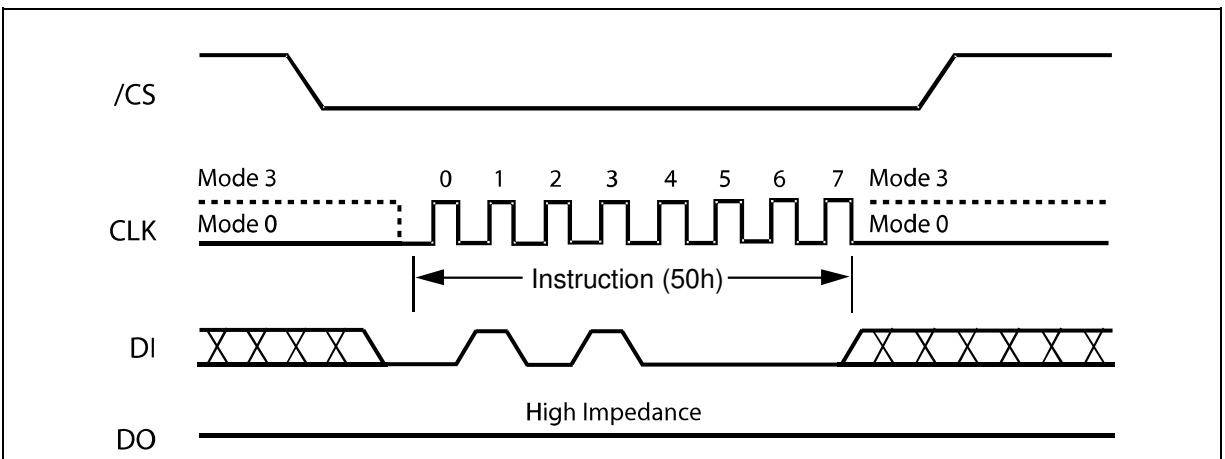


Figure 5. Write Enable for Volatile Status Register Instruction Sequence Diagram



8.1.12 Write Disable (04h)

The Write Disable instruction (Figure 6) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase instructions. Write Disable instruction can also be used to invalidate the Write Enable for Volatile Status Register instruction

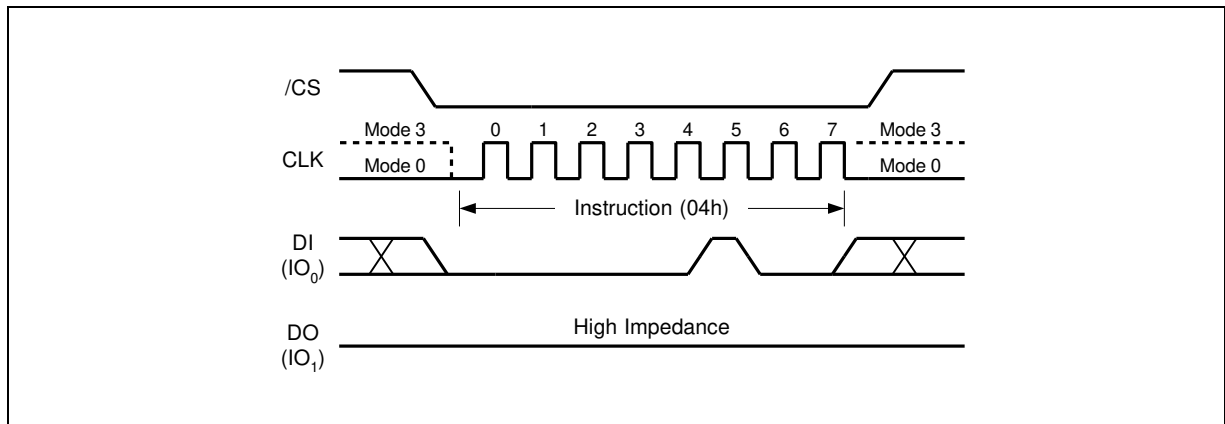


Figure 6. Write Disable Instruction Sequence Diagram

8.1.13 Read Status Register (05h)

The Read Status Register instruction allows the 8-bit Status Register to be read. The instruction is entered by driving /CS low and shifting the instruction code “05h” into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in figure 6. The Status Register bits are shown in figure 3 and include the BUSY, WEL, BP1, BP0, TB and SRP bits (see description of the Status Register earlier in this datasheet).

The Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 7. The instruction is completed by driving /CS high.

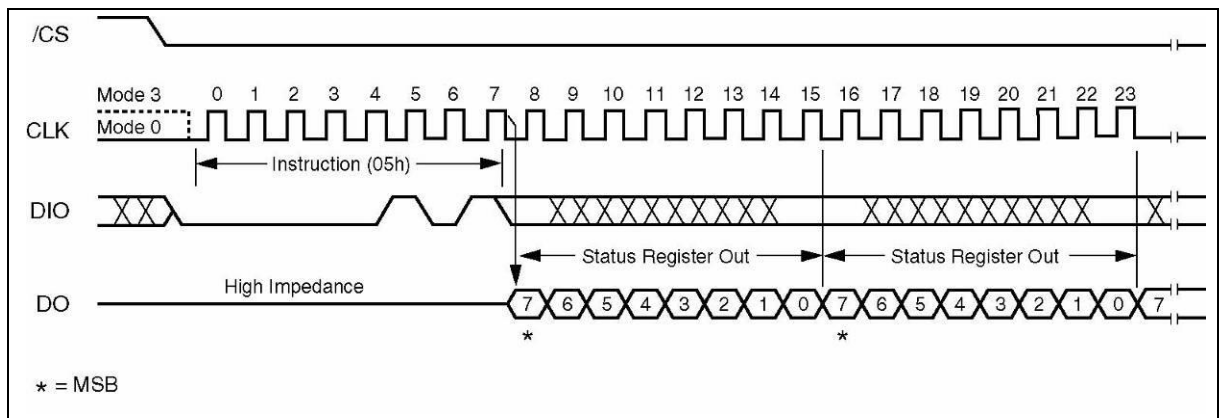


Figure 7. Read Status Register Instruction Sequence Diagram



8.1.14 Write Status Register (01h)

The Write Status Register instruction allows the Status Register to be written. A Write Enable instruction must previously have been executed for the device to accept the Write Status Register Instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code “01h”, and then writing the status register data byte as illustrated in figure 8. The Status Register bits are shown in figure 3 and described earlier in this datasheet.

Only non-volatile Status Register bits SRP, TB, BP1 and BP0 (bits 7, 5, 3 and 2) can be written to. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Write Status Register instruction will not be executed. After /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of t_w (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

The Write Status Register instruction allows the Block Protect bits (TB, BP1 and BP0) to be set for protecting all, a portion, or none of the memory from erase and program instructions. Protected areas become read-only (see Status Register Memory Protection table). The Write Status Register instruction also allows the Status Register Protect bit (SRP) to be set. This bit is used in conjunction with the Write Protect (/WP) pin to disable writes to the status register. When the SRP bit is set to a 0 state (factory default) the /WP pin has no control over the status register. When the SRP pin is set to a 1, the Write Status Register instruction is locked out while the /WP pin is low. When the /WP pin is high the Write Status Register instruction is allowed.

During volatile Status Register write operation (50h combined with 01h), after /CS is driven high, the Status Register bits will be refreshed to the new values within the time period of t_{SHSL2} (See AC Characteristics). BUSY bit will remain 0 during the Status Register bit refresh period.

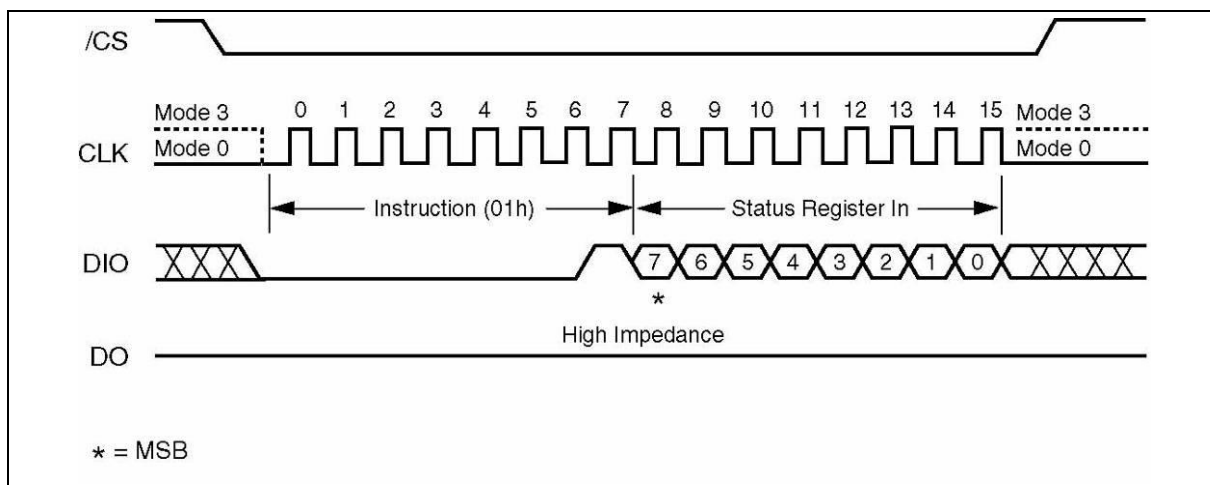


Figure 8. Write Status Register Instruction Sequence Diagram



8.1.15 Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high.

The Read Data instruction sequence is shown in figure 9. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of fR (see AC Electrical Characteristics).

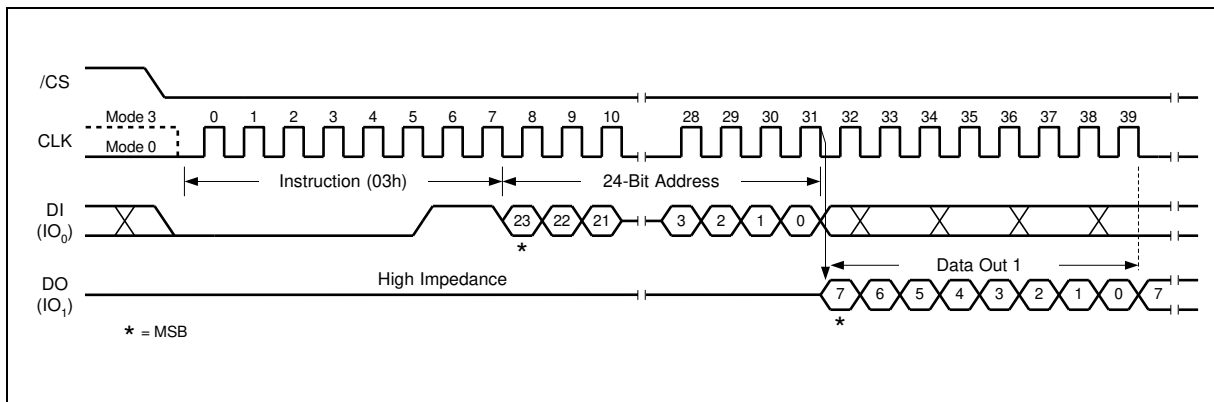


Figure 9. Read Data Instruction Sequence Diagram



8.1.16 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in figure 10. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DI pin is a “don’t care”.

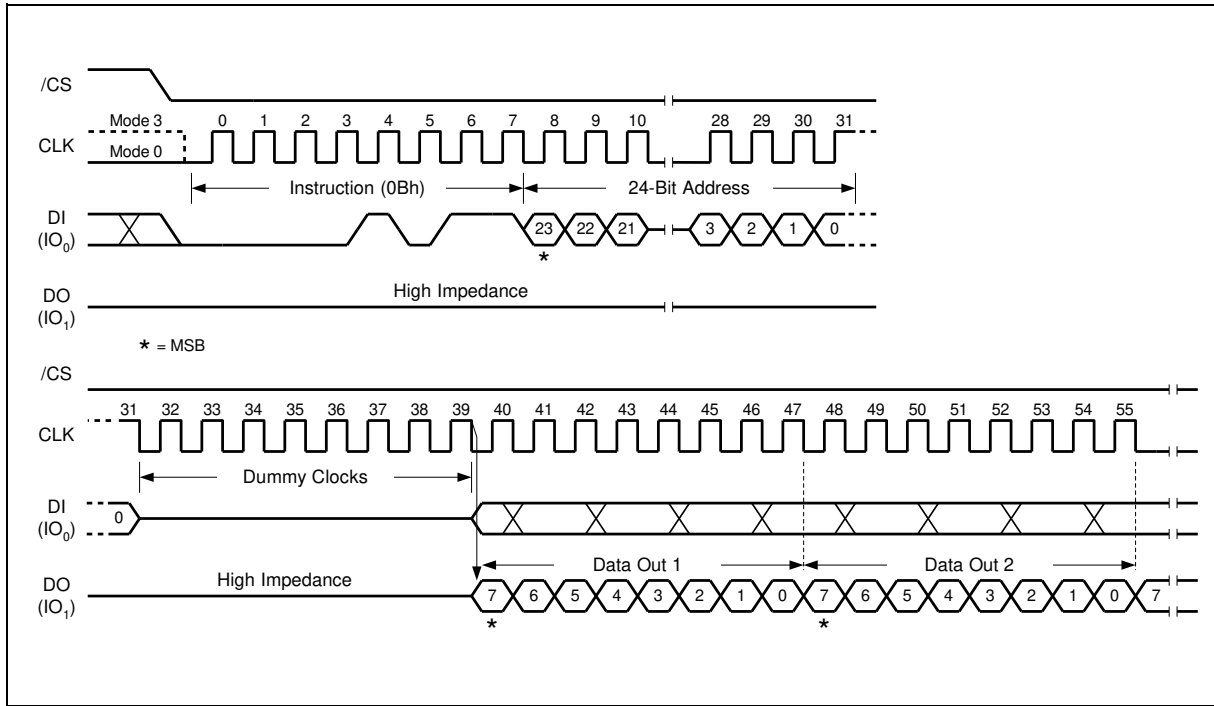


Figure 10. Fast Read Instruction Sequence Diagram



8.1.17 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins, IO₀ and IO₁. This allows data to be transferred from the W25X10CL at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in figure 11. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don't care”. However, the IO₀ pin should be high-impedance prior to the falling edge of the first data out clock.

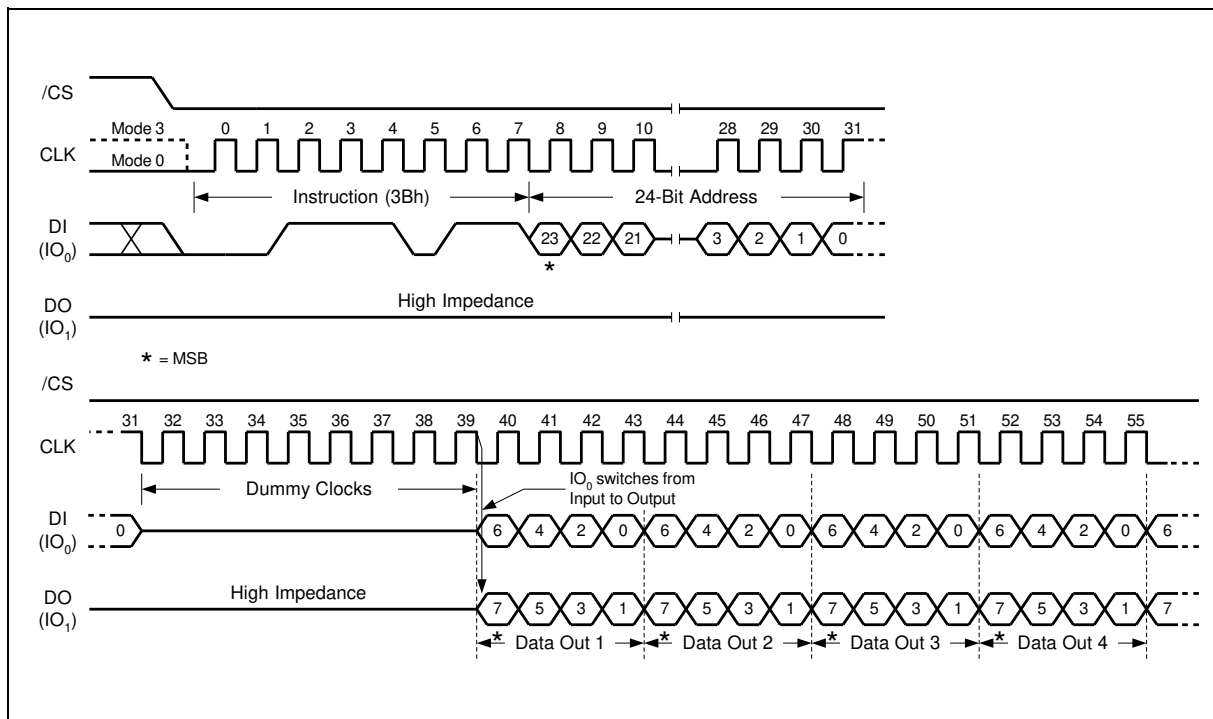


Figure 11. Fast Read Dual Output Instruction Sequence Diagram



8.1.18 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, IO₀ and IO₁. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

Fast Read Dual I/O with “Continuous Read Mode”

The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the “Continuous Read Mode” bits (M7-0) after the input Address bits (A23-0), as shown in figure 12a. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don’t care (“x”). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the “Continuous Read Mode” bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BBh instruction code, as shown in figure 12b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the “Continuous Read Mode” bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. A “Continuous Read Mode” Reset instruction can also be used to reset (M7-0) before issuing normal instructions (See 9.2.12 for detail descriptions).

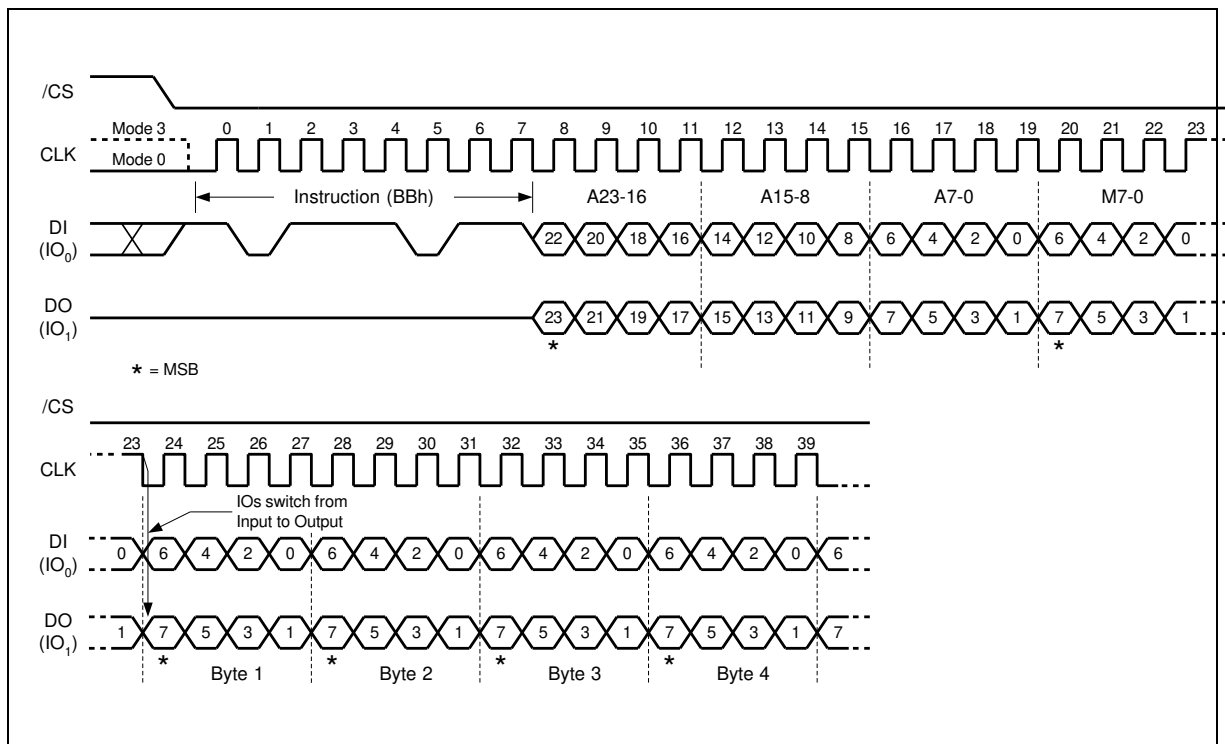


Figure 12a. Fast Read Dual I/O Instruction Sequence (Initial instruction or previous M5-4 ≠ 10)

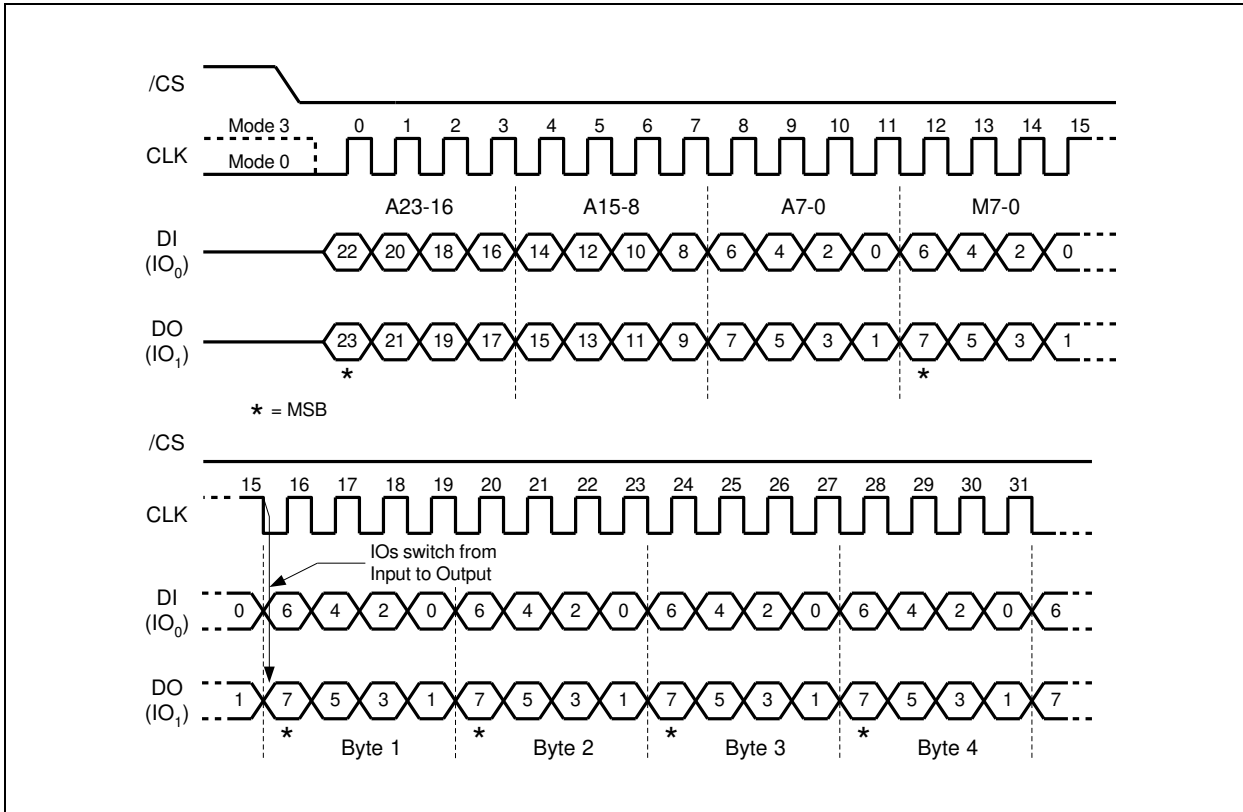


Figure 12b. Fast Read Dual I/O Instruction Sequence (Previous instruction set M5-4 = 10)



8.1.19 Continuous Read Mode Bits (M7-0)

The “Continuous Read Mode” bits are used in conjunction with the “Fast Read Dual I/O” instruction to provide the highest random Flash memory access rate with minimum SPI instruction overhead, thus allow true XIP (execute in place) to be performed on serial flash devices.

M7-0 need to be set by the Dual I/O Read instruction. M5-4 are used to control whether the 8-bit SPI instruction code BBh is needed or not for the next command. When M5-4 = (1,0), the next command will be treated same as the current Dual I/O Read command without needing the 8-bit instruction code; when M5-4 do not equal to (1,0), the device returns to normal SPI mode, all commands can be accepted. M7-6 and M3-0 are reserved bits for future use, either 0 or 1 values can be used.

8.1.20 Continuous Read Mode Reset (FFFFh)

Continuous Read Mode Reset instruction can be used to set M4 = 1, thus the device will release the Continuous Read Mode and return to normal SPI operation, as shown in figure 13.

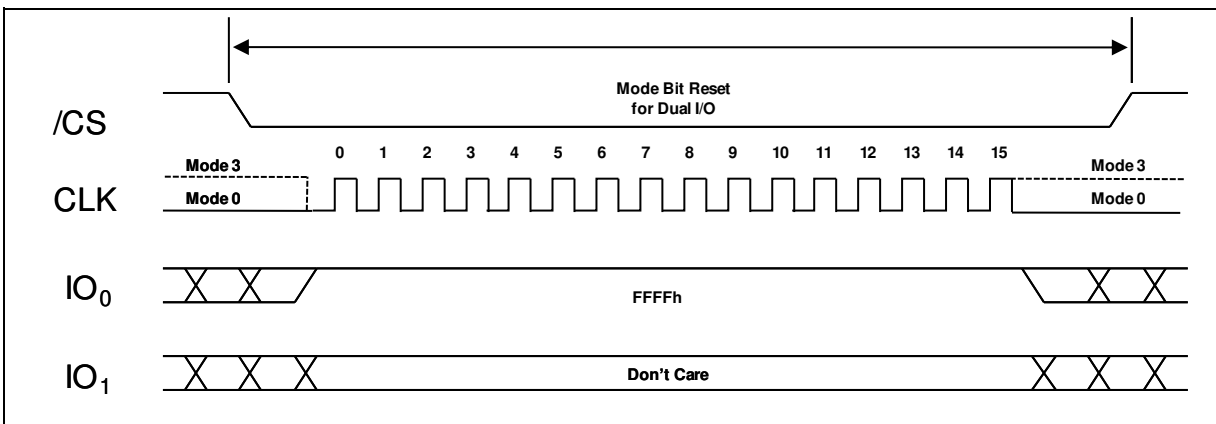


Figure 13. Continuous Read Mode Reset for Fast Read Dual I/O

Since W25X10CL does not have a hardware Reset pin, so if the controller resets while W25X10CL are set to Continuous Mode Read, the W25X10CL will not recognize any initial standard SPI instructions from the controller. To address this possibility, it is recommended to issue a Continuous Read Mode Reset instruction as the first instruction after a system Reset. Doing so will release the device from the Continuous Read Mode and allow Standard SPI instructions to be recognized.

To reset “Continuous Read Mode” during Dual I/O operation, sixteen clocks are needed to shift in instruction “FFFFh”.



8.1.21 Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL = 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks cannot exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of t_{pp} (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (BP1, and BP0) bits (see Status Register Memory Protection table).

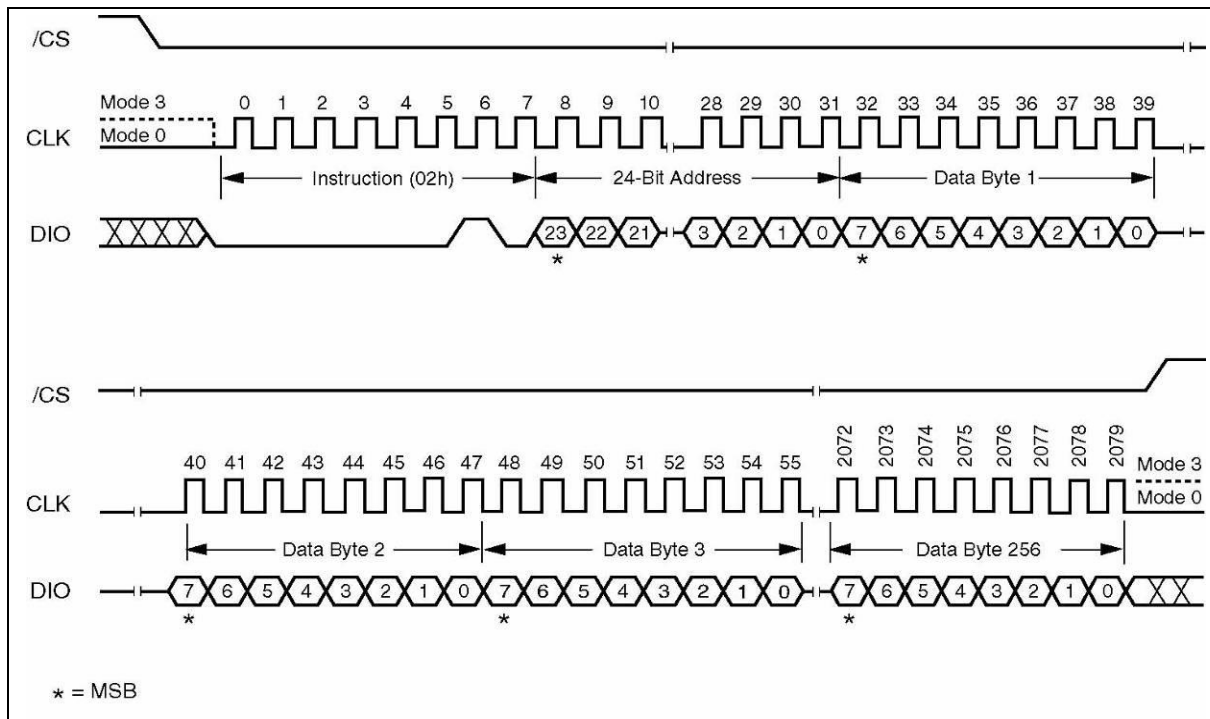


Figure 14. Page Program Instruction Sequence Diagram



8.1.22 Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “20h” followed a 24-bit sector address (A23-A0) (see Figure 2). The Sector Erase instruction sequence is shown in figure 15.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of tSE (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP1, and BP0) bits (see Status Register Memory Protection table).

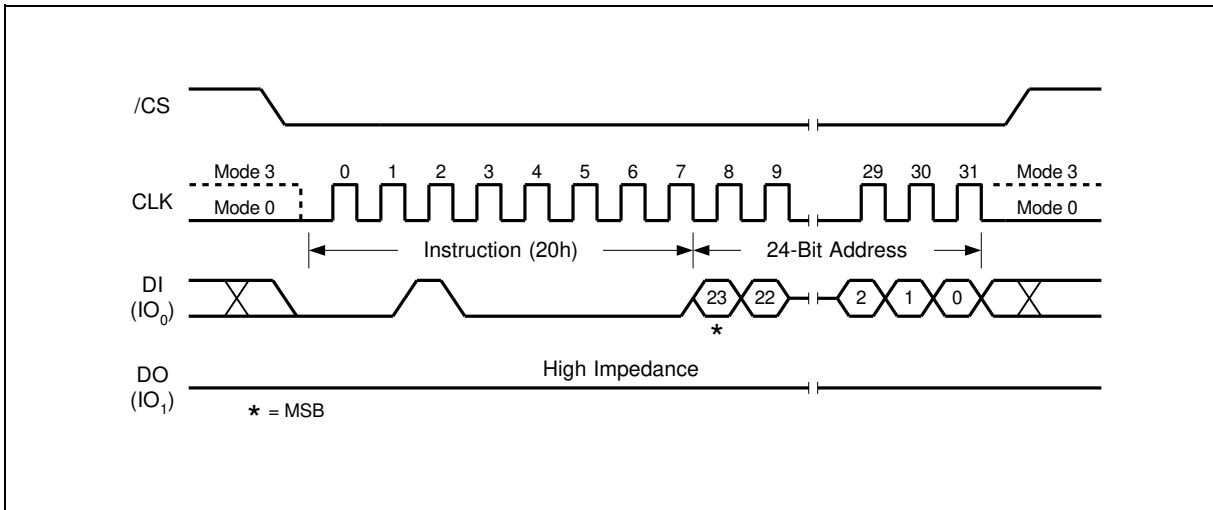


Figure 15. Sector Erase Instruction Sequence Diagram