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32M-BIT
3.0-VOLT PARALLEL FLASH MEMORY WITH PAGE MODE

Publication Release Date: August 2, 2013
Revision H

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1 GENERAL DESCRIPTION

The W29GL032C Parallel Flash memory provides a storage solution for embedded system applications that require better performance, lower power consumption and higher density. This device has a random access speed of 70ns and a fast page access speed of 25ns, as well as significantly faster program and erase times than the products comparable on the market today. The W29GL032C also offers special features such as Compatible Manufacturer ID that makes the device industry standard compatible without the need to change firmware.

2 FEATURES

- **32k-Word/64k-Byte uniform sector architecture**
  - Total 64 uniform sectors
  - Total 63 uniform sectors + eight 4k-Word/8k-Byte sectors
- **16-Word/32-Byte write buffer**
  - Reduces total program time for multiple-word updates
- **8-Word/16-Byte page read buffer**
- **Secured Silicon Sector area**
  - Programmed and locked by the customer or during production.
  - 128-word/256-byte sector for permanent, safe identification using an 8-word/16-byte random electronic serial number.
- **Enhanced Sector Protect using Dynamic and Individual mechanisms**
- **Polling/Toggling methods are used to detect the status of program and erase operation**
- **Suspend and resume commands used for program and erase operations**
- **More than 100,000 erase/program cycles**
- **More than 20-year data retention**
- **Low power consumption**
- **Deep power down mode**
- **Wide temperature ranges**
- **Compatible manufacturer ID for drop-in replacement**
  - No firmware change is required
- **Faster Erase and Program time**
  - Erase is 1.5x faster than industry standard
  - Program is 2x faster than industry standard
  - Allows for improved production throughput and faster field updates
- **CFI (Common Flash Interface) support**
- **Single 3V Read/Program/Erase (2.7 - 3.6V)**
- **Enhanced Variable IO control**
  - All input levels (address, control, and DQ) and output levels are determined by voltage on the EVIO input. EVIO ranges from 1.65 to VCC
- **#WP/ACC Input**
  - Accelerates programming time (when VHH is applied) for greater throughput during system production
  - Protects first or last sector regardless of sector protection settings
- **Hardware reset input (#reset) resets device**
- **Ready/#Busy output (RY/#BY) detects completion of program or erase cycle**
- **Packages**
  - Uniform Sector (H/L)
    56-pin TSOP
    64-ball LFBGA
  - Boot Sector (T/B)
    48-pin TSOP
    48-ball TFBGA
    64-ball LFBGA

3 PIN CONFIGURATIONS

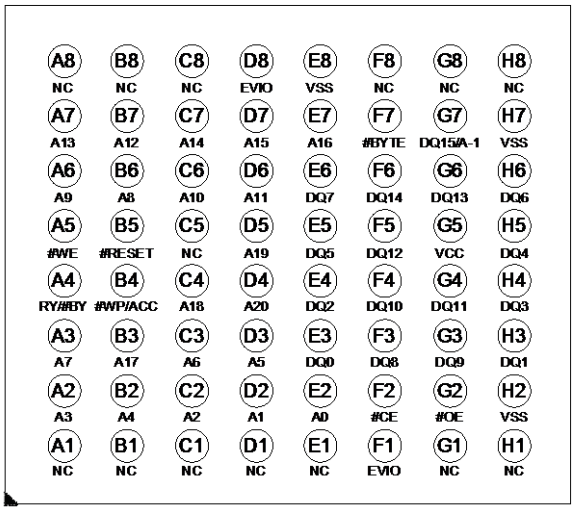

Figure 3-1 LFBGA64 TOP VIEW (FACE DOWN)

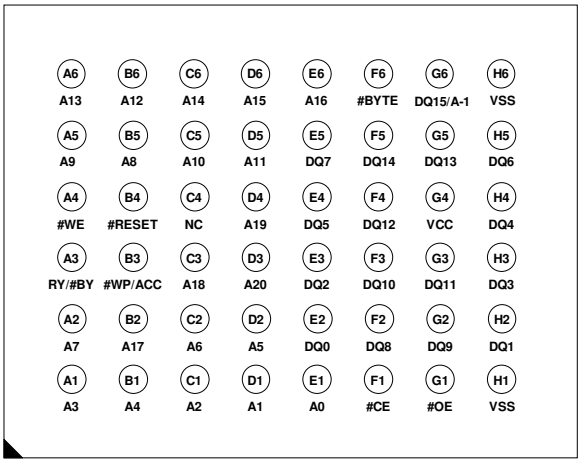

Figure 3-3 TFBGA48 TOP VIEW (FACE DOWN)

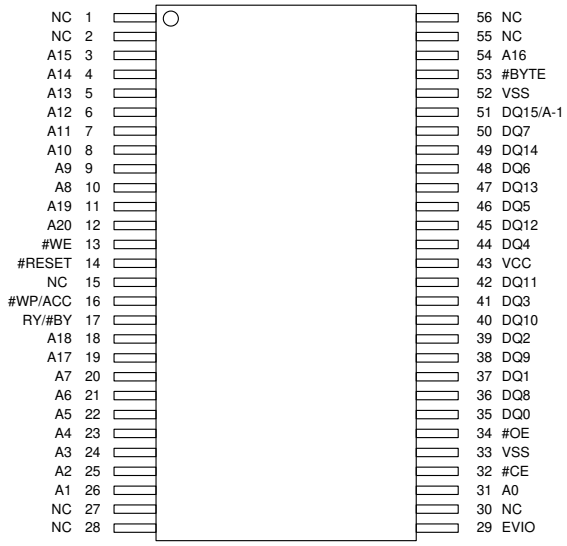

Figure 3-2 56-PIN STANDARD TSOP (TOP VIEW)

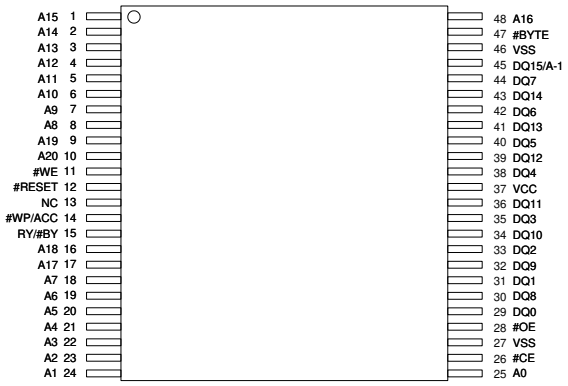

Figure 3-4 48-PIN STANDARD TSOP (TOP VIEW)

4 BLOCK DIAGRAM

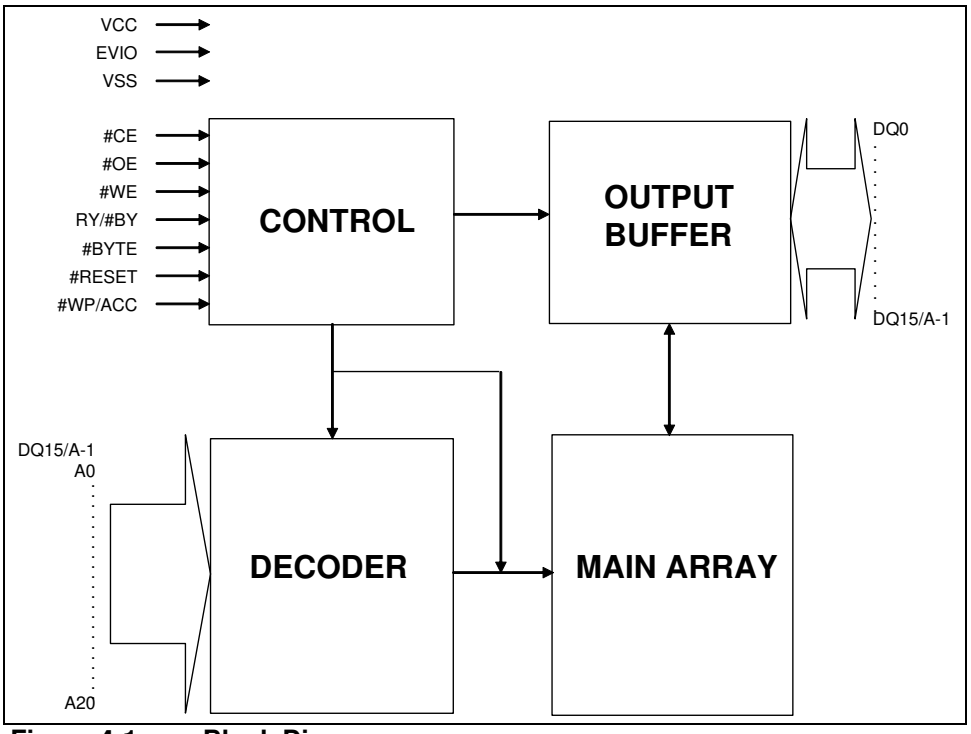

Figure 4-1 Block Diagram

5 PIN DESCRIPTION

SYMBOL	PIN NAME	
A0-A20	Address Inputs	
DQ0-DQ14	Data Inputs/Outputs	
DQ15/A-1	Word mode	DQ15 is Data Input/Output
	Byte mode	A-1 is Address Input
#CE	Chip Enable	
#OE	Output Enable	
#WE	Write Enable	
#WP/ACC	Hardware Write Protect/ Acceleration Pin	
#BYTE	Byte Enable	
#RESET	Hardware Reset	
RY/#BY	Ready/Busy Status	
V_{CC}	Power Supply	
E_{VIO}	Enhanced Variable IO Supply (No connect for top/bottom LFBGA64 configurations)	
VSS	Ground	
NC	No Connection	

Table 5-1 Pin Description

6 ARRAY ARCHITECTURE

6.1 H/L Sector Address Table

Sector	Sector Address A20-A15	Sector Size (KByte/KWord)	X8 Start / Finish		X16 Start / Finish	
SA00	000000	64/32	000000h	00FFFFh	000000h	007FFFh
SA01	000001	64/32	010000h	01FFFFh	008000h	00FFFFh
.	.	.	.	.	.	.
SA62	111110	64/32	3E0000h	3EFFFFh	1F0000h	1F7FFFh
SA63	111111	64/32	3F0000h	3FFFFFh	1F8000h	1FFFFFh

Table 6-1 High/Low Sector Table

Note: The address range is [A20:A-1] in byte mode (#BYTE = VIL) or [A20:A0] in word mode (#BYTE = VIH)

6.2 Top Sector Address Table

Sector	Sector Address A20-A12	Sector Size (KByte/KWord)	X8 Start / Finish		X16 Start / Finish	
SA00	000000xxx	64/32	000000h	00FFFFh	000000h	007FFFh
SA01	000001xxx	64/32	010000h	01FFFFh	008000h	00FFFFh
.	.	.	.	.	.	.
SA62	111110xxx	64/32	3E0000h	3EFFFFh	1F0000h	1F7FFFh
SA63	111111000	8/4	3F0000h	3F1FFFh	1F8000h	1F8FFFh
.	.	.	.	.	.	.
SA70	111111111	8/4	3FE000h	3FFFFFh	1FF000h	1FFFFFh

Table 6-2 Top Boot Sector Table

Note: The address range is [A20:A-1] in byte mode (#BYTE = VIL) or [A20:A0] in word mode (#BYTE = VIH)

6.3 Bottom Sector Address Table

Sector	Sector Address A20-A12	Sector Size (KByte/KWord)	X8 Start / Finish		X16 Start / Finish	
SA00	000000000	8/4	000000h	001FFFh	000000h	000FFFh
.	.	.	.	.	.	.
SA07	000000111	8/4	00E000h	00FFFFh	007000h	007FFFh
SA08	000001xxx	64/32	010000h	01FFFFh	008000h	00FFFFh
.	.	.	.	.	.	.
SA70	111111xxx	64/32	3F0000h	3FFFFFh	1F8000h	1FFFFFh

Table 6-3 Bottom Boot Sector Table

Note: The address range is [A20:A-1] in byte mode (#BYTE = VIL) or [A20:A0] in word mode (#BYTE = VIH)

7 FUNCTIONAL DESCRIPTION

7.1 Device Bus Operation

Mode Select	#Reset	#CE	#WE	#OE	Address(4)	Data I/O DQ[7:0]	#BYTE VIL Data I/O DQ[15:8]	#BYTE VIH	#WP/ACC
Device Reset	L	X	X	X	X	High-Z	High-Z	High-Z	L/H
Standby Mode	VCC±0.3V	VCC±0.3V	X	X	X	High-Z	High-Z	High-Z	H
Output Disable	H	L	H	H	X	High-Z	High-Z	High-Z	L/H
Read Mode	H	L	H	L	AIN	DOUT	DQ[14:8]=High-Z DQ15=A-1	DOUT	L/H
Write	H	L	L	H	AIN	DIN		DIN	Note(1,2)
Accelerated Program	H	L	L	H	AIN	DIN		DIN	VHH

Table 7-1 Device Bus Operation

Notes:

1. For High/Low configuration, either the first or last sector was protected if #WP/ACC=VIL.
   For Top/Bottom Boot configuration, either the top or bottom two sectors are protected if #WP/ACC=VIL.
2. When #WP/ACC = VIH, the protection conditions of the outmost sector depends on previous protection conditions. Refer to the enhanced protect feature.
3. DQ[15:0] are input (DIN) or output (DOUT) pins according to the requests of instruction sequence, sector protection, or data polling algorithm.
4. In Word Mode (#BYTE=VIH), the addresses are A20 to A0. In Byte Mode (#BYTE=VIL), the addresses are A20 to A-1 (DQ15),.

Description		Control Inputs #CE	#WE	#OE	A20 ~12	A11 ~10	A9	A8 ~7	A6	A5 ~4	A3 ~2	A1	A0	DQ[7:0] T/B	DQ[7:0] H/L	DQ[15:8] BYTE	DQ[15:8] WORD
Read Silicon ID MFR Code		L	H	L	X	X	VHH	X	L	X	L	L	L	01		X	00
Device ID	Cycle 1	L	H	L	X	X	VHH	X	L	X	L	L	H	7E		X	22
	Cycle 2	L	H	L	X	X	VHH	X	L	X	H	H	L	1A	1D	X	22
	Cycle 3	L	H	L	X	X	VHH	X	L	X	H	H	H	01(T) 00(B)	00	X	22
Sector Lock Status Verification(1)		L	H	L	SA	X	VHH	X	L	X	L	H	L	01/00		X	X
Secure Sector (H) (2)		L	H	L	X	X	VHH	X	L	X	L	H	H	9A/1A		X	X
Secure Sector (L) (2)		L	H	L	X	X	VHH	X	L	X	L	H	H	8A/0A		X	X

Table 7-2 Device Bus Operation (continue)

Notes:

1. Sector unprotected code:00h. Sector protected code:01h.
2. Factory locked code: #WP protects high address sector: 9Ah. #WP protects low address sector: 8Ah. Factory unlocked code: #WP protects high address sector: 1Ah. #WP protects low address sector: 0Ah

7.2 Instruction Definitions

The device operation can be initiated by writing specific address and data commands or sequences into the instruction register. The device will be reset to reading array data when writing incorrect address and data values or writing them in the improper sequence.

The addresses will be latched on the falling edge of #WE or #CE, whichever happens later; while the data will be latched on the rising edge of #WE or #CE, whichever happens first. Please refer to timing waveforms.

7.2.1 Reading Array Data

The default state after power up or a reset operation is the Read mode.

To execute a read operation, the chip is enabled by setting #CE and #OE active and #WE high. At the same time, the required address or status register location is provided on the address lines. The system reads the addressed location contents on the Data IO pins after the t_{CE} and t_{OE} timing requirements have been met. Output data will not be accessible on the Data IO pins if either the device or it's outputs are not enabled by #CE or #OE being High, and the outputs will remain in a tri-state condition.

When the device completes an embedded memory operation (i.e., Program, automatic Chip Erase or Sector Erase) successfully, it will return to the Read mode and from any address in the memory array the data can be read. However, If the embedded operation fails to complete, by verifying the status register bit DQ5 (exceeds time limit flag) going high during the operations, at this time system should execute a Reset operation causing the device to return to Read mode.

Some operating states require a reset operation to return to Read mode such as:

- Time-out condition during a program or erase failed condition, indicated by the status register bit DQ5 going High during the operation. Failure during either of these states will prevent the device from automatically returning to Read mode.
- During device Auto Select mode or CFI mode, a reset operation is required to terminate their operation.

In the above two situations, the device will not return to the Read mode unless a reset operation is executed (either hardware reset or software reset instruction) or the system will not be able to read array data.

The device will enter Erase-Suspended Read mode if the device receives an Erase Suspend instruction while in the Sector Erase state. The erase operation will pause (after a time delay not exceeding 20µs) prior to entering Erase-Suspend Read mode. At this time data can be programmed or read from any sector that is not being erased. Another way to verify device status is to read the addresses inside the sectors being erased. This will only provide the contents of the status register.

Program operation during Erase-Suspend Read mode of valid sector(s) will automatically return to the Erase-Suspend Read mode upon successful completion of the program operation.

An Erase Resume instruction must be executed to exit the Erase-Suspended Read mode, at which time suspended erase operations will resume. Erase operation will resume where it left off and continue until successful completion unless another Erase Suspend instruction is received.

7.2.2 Page Mode Read

The Page Mode Read has page sizes of 16 bytes or 8 words. The higher addresses A[20:3] accesses the desired page. To access a particular word or byte in a page, it is selected by A[2:0] for word mode and A[2:0,A-1] for byte mode. Page mode can be turned on by keeping "page-read address" constant and changing the "intra-read page" addresses. The page access time is t_{AA} or t_{CE}, followed by t_{PA} for the page read time. When #CE toggles, access time is t_{AA} or t_{CE}.

7.2.3 Device Reset Operation

Pulling the #RESET pin Low for a period equal to or greater than t_{RP} will return the device to Read mode. If the device is performing a program or erase operation, the reset operation will take at most a period of t_{READY1} before the device returns to Read mode. The RY/#BY pin will remain Low (Busy Status) until the device returns to Read mode.

Note, the device draws larger current if the #RESET pin is held at voltages greater that GND+0.3V and less than or equal to V_{IL}. When the #RESET pin is held a GND±0.3V, the device only consumes Reset (I_{CC5}) current.

It is recommended to tie the system reset signal to the #RESET pin of the flash memory. This allows the device to be reset with the system and puts it in a state where the system can immediately begin reading boot code from it.

Executing the Reset instruction will reset the device back to the Read mode in the following situations:

- During an erase instruction sequence, before the full instruction set is completed.
- Sector erase time-out period
- Erase failed, while DQ5 is High.
- During program instruction sequence, before the full instruction set is completed, including the erase-suspended program instruction.
- Program failed, while DQ5 is High as well as the erase-suspended program failure.
- Auto-select mode
- CFI mode
- The user must issue a reset instruction to reset the device back to the Read mode when the device is in Auto-Select mode or CFI mode, or when there is a program or erase failure (DQ5 is High).
- When the device is performing a Programming (not program fail) or Erasing (Not erase fail) function, the device will ignore reset commands.

7.2.4 Standby Mode

Standby mode is entered when both #RESET and #CE are driven to V_{CC} ±300mV (inactive state). (Note, if both pins are not within the E_{VIO} ±0.3V, but at V_{IH}, standby current will be greater.) At this time output pins are placed in the high impedance state regardless of the state of the #WE or #OE pins and the device will draw minimal standby current (I_{CC4}). If the device is deselected during erase or program operation, the device will draw active current until the operation is completed.

7.2.5 Output Disable Mode

The #OE pin controls the state of the Data IO pins. If #OE is driven High (V_{IH}), all Data IO pins will remain at high impedance and if driven Low, the Data IO pins will drive data (#OE has no affect on the RY/#BY output pin).

7.2.6 Write Operation

To execute a write operation, Chip Enable (#CE) pin is driven Low and the Output Enable (#OE) is pulled high to disable the Data IO pins to a high impedance state. The desired address and data should be present on the appropriate pins. Addresses are latched on the falling edge of either #WE or #CE and Data is latched on the rising edge or either #CE or #WE. To see an example, please refer to timing diagrams in Figure 8-5, Figure 8-15 or Figure 8-16. If an invalid write instruction, not defined in this datasheet is written to the device, it may put the device in an undefined state.

7.2.7 Byte/Word Selection

To choose between the Byte or Word mode, the #BYTE input pin is used to select how the data is input/output on the Data IO pins and the organization of the array data. If the #BYTE pin is driven High, Word mode will be selected and all 16 Data IO pins will be active. If the #BYTE is pulled Low, Byte mode will be active and only Data IO DQ[7:0] will be active. The remaining Data IO pins (DQ[14:8]) will be in a high impedance state and DQ15 becomes the A-1 address input pin.

7.2.8 Automatic Programming of the Memory Array

To program the memory array in Byte or Word mode, refer to the Instruction Definition Tables for correct cycle defined instructions that include the 2 unlocking instruction cycles, the A0h program cycle instruction and subsequent cycles containing the specified address location and the byte or word desired data content, followed by the start of the embedded algorithm to automatically program the array.

Once the program instruction sequence has been executed, the internal state machine commences execution of the algorithms and timing necessary for programming and cell verification. Included in this operation is generating suitable program pulses, checking cell threshold voltage (V_T) margins, and if any cells do not pass verification or have acceptable margins, repetitive program pulse sequence will be cycled again. The internal process mechanisms will protect cells that do pass margin and verification tests from being over-programmed by prohibiting further program pulses to passing cells as failing cells continue to be run through the internal programming sequence until the pass.

This feature allows the user to only perform the auto-programming sequence once and the device state machine takes care of the program and verification process.

Array bits during programming can only change a bit status of “1” (erase state) to a “0” (programmed state). It is not possible to do the reverse with a programming operation. This can only be done by first performing an erase operation. Keep in mind, the internal write verification only checks and detects errors in cases where a “1” is not successfully programmed to “0”.

During the embedded programming algorithm process any commands written to the device will be ignored, except hardware reset or program suspend instruction. Hardware reset will terminate the program operation after a period of time, not to exceed 10µs. If in the case a Program Suspend was executed, the device will enter the programs suspend read mode. When the embedded program algorithm is completed or the program is terminated by a hardware reset, the device will return to Read mode.

The user can check for completion by reading the following bits in the status register, once the embedded program operation has started:

Status	DQ7	DQ6	DQ5	DQ1	RY/#BY[1]
In progress	DQ7#	Toggling	0	0	0
Exceeded time limit	DQ7#	Toggling	1	N/A	0

Table 7-3 Polling During Embedded Program Operation

Note:
1. RY/#BY is an open drain output pin and should be connected to VCC through a high value pull-up resistor.

7.2.9 Erasing the Memory Array

Sector Erase and Chip Erase are the two possible types of erase operations executed on the memory array. Sector Erase operation erases one or more selected sectors and this can be simultaneous. Chip Erase operation erases the entire memory array, except for any protected sectors.

7.2.9.1 Sector Erase

The sector erase operation returns all selected sectors in memory to the “1” state, effectively clearing all data. This action requires six instruction cycles to commence the erase operation. The unlock sequence is the first two cycles, followed by the configuration cycle, the fourth and fifth are also ”unlock cycles”, and the Sector Erase instruction is the sixth cycle. An internal 50µs time-out counter is started once the sector erase instruction sequence has been completed. During this time, additional sector addresses and Sector Erase commands may be issued, thus allowing for multiple sectors to be selected and erased simultaneously. Once the 50µs time-out counter has reached its limit, no additional command instructions will be accepted and the embedded sector erase algorithm will commence.

Note, that the 50µs time-out counter restarts after every sector erase instruction sequence. The device will abort and return to Read mode, if any instruction other than Sector Erase or Erase Suspend is attempted during the time-out period.

Once the embedded sector erase algorithm begins, all instructions except Erase Suspend or Hardware Reset will be ignored. The hardware reset will abort the erase operation and return the device to the Read mode.

The embedded sector erase algorithm status can be verified by the following:

Status	DQ7	DQ6	DQ5	DQ3[1]	DQ2	RY/#BY[2]
Time-out period	0	Toggling	0	0	Toggling	0
In progress	0	Toggling	0	1	Toggling	0
Exceeded time limit	0	Toggling	1	1	Toggling	0

Table 7-4 Polling During Embedded Sector Erase Operation

Note:

1. The DQ3 status bit is the 50µs time-out indicator. When DQ3=0, the 50µs time-out counter has not yet reached zero and the new Sector Erase instruction maybe issued to specify the address of another sector to be erased. When DQ3=1, the 50µs time-out counter has expired and the Sector Erase operation has already begun. Erase Suspend is the only valid instruction that maybe issued once the embedded erase operation is underway.
2. RY/#BY is an open drain output pin and should be connected to VCC through a high value pull-up resistor.
3. When an attempt is made to erase only protected sector(s), the erase operation will abort thus preventing any data changes in the protected sector(s). DQ7 will output “0” and DQ6 will toggle briefly (100µs or less) before aborting and returning the device to Read mode. If unprotected sectors are also specified, however, they will be erased normally and the protected sector(s) will remain unchanged.
4. DQ2 is a localized indicator showing a specified sector is undergoing erase operation or not. DQ2 toggles when user reads at the addresses where the sectors are actively being erased (in erase mode) or to be erased (in erase suspend mode).

7.2.9.2 Chip Erase

The Chip Erase operation returns all memory locations containing a bit state of “0” to the “1” state, effectively clearing all data. This action requires six instruction cycles to commence the erase operation. The unlock sequence is the first two cycles, followed by the configuration cycle, the fourth and fifth are also ”unlock cycles”, and the sixth cycle initiates the chip erase operation.

Once the chip erase algorithm begins, no other instruction will be accepted. However, if a hardware reset is executed or the operating voltage is below acceptable levels, the chip erase operation will be terminated and automatically returns to Read mode.

The embedded chip erase algorithm status can be verified by the following:

Status	DQ7	DQ6	DQ5	DQ2	RY/#BY[1]
In progress	0	Toggling	0	Toggling	0
Exceeded time limit	0	Toggling	1	Toggling	0

Table 7-5 Polling During Embedded Chip Erase Operation

Note:
1. RY/#BY is an open drain pin and should be connected to VCC through a high value pull-up resistor.

7.2.10 Erase Suspend/Resume

If there is a sector erase operation in progress, an Erase Suspend instruction is the only valid instruction that may be issued. Once the Erase Suspend instruction is executed during the 50µs time-out period following a Sector Erase instruction, the time-out period will terminate right away and the device will enter Erase-Suspend Read mode. If an Erase Suspend instruction is executed after the sector erase operation has started, the device will not enter Erase-Suspended Read mode until approximately 20µs (5µs typical) time has elapsed. To determine the device has entered the Erase-Suspend Read mode, use DQ6, DQ7 and RY/#BY status to verify the state of the device.

Once the device has entered Erase-Suspended Read mode, it is possible to read or program any sector(s) except those being erased by the erase operation. Only the contents of the status register is present when attempting to read a sector that has been scheduled to erase or be programmed when in the suspend mode. A resume instruction must be executed and recommend checking DQ6 toggle bit status, before issuing another erase instruction.

The status register bits can be verified to determine the current status of the device:

Status	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	RY/#BY
Erase suspend read in erase suspended sector	1	No toggle	0	N/A	Toggle	N/A	1
Erase suspend read in non-erase suspended sector	Data	Data	Data	Data	Data	Data	1
Erase suspend program in non-erase suspended sector	DQ7#	Toggle	0	N/A	N/A	N/A	0

Table 7-6 Polling During Embedded Erase Suspend

Instruction sets such as read silicon ID, sector protect verify, program, CFI query and erase resume can also be executed during Erase-Suspend mode, except sector and chip erase.

7.2.11 Sector Erase Resume

Only in the Erase-Suspended Read mode can the Sector Erase Resume instruction be a valid command. Once erase resumes, another Erase Suspend instruction can be executed, but allow a 400µs interval between Erase Resume and the next Erase Suspend instruction.

7.2.12 Program Suspend/Resume

Once a program operation is in progress, a Program Suspend is the only valid instruction that maybe executed. Verifying if the device has entered the Program-Suspend Read mode after executing the Program-Suspend instruction, can be done by checking the RY/#BY and DQ6. Programming should halt within 15µs maximum (5µs typical).

Any sector(s) can be read except those being program suspended. Trying to read a sector being program suspended is invalid. Before another program operation can be executed, a Resume instruction must be performed and DQ6 toggling bit status has to be verified. Use the status register bits shown in the following table to determine the current state of the device:

Status	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	RY/#BY
Program suspend read in program suspended sector	Invalid						1
Program suspend read in non-program suspended sector	Data	Data	Data	Data	Data	Data	1

Table 7-7 Polling During Embedded Program Suspend

Instruction sets such as read silicon ID, sector protect verify, program, CFI query can also be executed during Program/Erase-Suspend mode.

7.2.13 Program Resume

The program Resume instruction is valid only when the device is in Program-Suspended mode. Once the program resumes, another Program Suspend instruction can be executed. Insure there is at least a 5µs interval between Program Resume and the next Suspend instruction.

7.2.14 Programming Operation

Write Buffer Programming Operation, programs 32-bytes or 16-words in a two step programming operation. To begin execution of the Write Buffer Programming, start with the first two unlock cycles, the third cycle writes the programming Sector Address destination followed by the Write Buffer Load Instruction (25h). The fourth cycle repeats the Sector Address, while the write data is the number of intended word locations to be written minus one. (Example, if the number of word locations to be written is 9, then the value would be 8h.) The 5th cycle is the first starting address/data set. This will be the first pair to be programmed and consequentially, sets the “write-buffer-page” address. Repeat Cycle 5 format for each additional address/data sets to be written to the buffer. Keep in mind all sets must remain within the write buffer page address range. If not, operation will ABORT.

The “write-buffer-page” is selected by choosing address A[20:4].

The second step will be to program the contents of the write buffer page. This is done with one cycle, containing the sector address that was used in step one and the “Write to Buffer Program Confirm” instruction (29h).

Standard suspend/resume commands can be used during the operation of the write-buffer. Also, once the write buffer programming operation is finished, it’ll return to the normal READ mode.

Write buffer programming can be conducted in any sequence. However the CFI functions, autoselect, Secured Silicon sector are not functional when program operation is in progress. Multiple write buffer programming operations on the same write buffer address range without intervention erase is accessible. Any bit in a write buffer address range cannot be programmed from 0 back to 1.

7.2.15 Buffer Write Abort

Write Buffer Programming Sequence will ABORT, if the following condition takes place:

- The word count minus one loaded is bigger than the page buffer size (32) during, “Number of Locations to Program.”
- Sector Address written is not the same as the one specified during the Write-Buffer-Load instruction.
- If the Address/Data set is not inside the Write Buffer Page range which was set during cycle 5’s first initial write-buffer-page select address/data set.
- No “Program Confirm Instruction” after the assigned number of “data load” cycles.

After Write Buffer Abort, the status register will be DQ1=1, DQ7 = DATA# (last address loaded), DQ6=toggle, DQ5=0. This status represents a Write Buffer Programming Operation was ABORTED. A Write-to-Buffer-Abort Reset instruction sequence has to be written to reset the device back to the read array mode.

DQ1 is the bit for Buffer Write Abort. When DQ1=1, the device will abort from buffer write operation and go back to read status register shown in the following table:

Status	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	RY/#BY
Buffer Write Busy	DQ7#	Toggle	0	N/A	N/A	0	0
Buffer Write Abort	DQ7#	Toggle	0	N/A	N/A	1	0
Buffer Write Exceeded Time Limit	DQ7#	Toggle	1	N/A	N/A	0	0

Table 7-8 Polling Buffer Write Abort Flag

7.2.16 Accelerated Programming Operation

The device will enter the Accelerated Programming mode by applying high voltage (V_{HH}) to the #WP/ACC pin. Accelerated Programming mode allows the system to skip the normal unlock sequences instruction and program byte/word locations directly. The current drawn from the #WP/ACC pin during accelerated programming is no more than I_{ACC1}. Important Note: Do not exceed 10 accelerated programs per sector. (#WP/ACC should not be held at VHH for any other function except for programming or damage to the device may occur.)

7.2.17 Automatic Select Bus Operation

There are basically two methods to access Automatic Selection Operations; Automatic Select Instructions through software commands and High Voltage applied to A9. See Automatic Select Instruction Sequence later on in this section for details of equivalent instruction operations that do not require the use of V_{HH}. The following five bus operations require A9 to be raised to V_{HH}.

7.2.17.1 Sector Lock Status Verification

To verify the protected state of any sector using bus operations, execute a Read Operation with V_{HH} applied to A9, the sector address present on address pins A[20:12], address pins A6, A3, A2, and A0 held Low, and address pins A1 held High. If DQ0 is Low, the sector is considered not protected, and if DQ0 is High, the sector is considered to be protected.

7.2.17.2 Read Silicon Manufacturer ID Code

Winbond’s 29GL family of Parallel Flash memories feature an Industry Standard compatible Manufacturer ID code of 01h. To verify the Silicon Manufacturer ID code, execute a Read Operation with VHH applied to the A9 pin and address pins A6, A3, A2, A1 and A0 are held Low. The ID code can then be read on data bits DQ[7:0].

7.2.17.3 Read Silicon Device ID Code

To verify the Silicon Device ID Codes, execute a Read Operation with V_{HH} applied to the A9 pin and address pins A6, A3, A2, A1, and A0 have several bit combinations to return the Winbond Device ID codes of 7Eh, 21h or 01h, which is shown on the data bits DQ[7:0]. See Table 7-2.

7.2.17.4 Read Indicator Bit DQ7 for Security Sector High and Low Address

To verify that the Security Sector has been factory locked, execute a Read Operation with V_{HH} applied to A9, address pins A6, A3, and A2 are held Low, and address pins A1 and A0 are held High. If the Security Sector has been factory locked, the code 9Ah(Highest Address Sector) or 8Ah(Lowest Address Sector) will be shown on the data bits DQ[7:0]. Otherwise, the factory unlocked code of 1Ah(H)/0A(L) will be shown.

7.2.18 Automatic Select Operations

The Automatic Select instruction show in Table 7-13 can be executed if the device is in one of the following modes; Read, Program Suspended, Erase-Suspended Read, or CFI. At which time the user can issue (two unlock cycles followed by the Automatic Select instruction 90h) to enter Automatic Select mode. Once in the Automatic Select mode, the user can query the Manufacturer ID, Device ID, Security Sector locked status, or Sector protected status multiple times without executing the unlock cycles and a Automatic Select instruction (90h) again.

Once in Automatic Select mode, executing a Reset instruction (F0h) will return the device back to the valid mode from which it left when the Automatic Select mode was first executed.

Another way previously mentioned to enter Automatic Select mode is to use one of the bus operation shown Table 7-2 in Device Bus Operation. Once the high voltage (V_{HH}) is removed from the A9 pin, the device will return back to the valid mode from which it left when the Automatic Select mode was first executed.

7.2.19 Automatic Select Instruction Sequence

Accessing the manufacturer ID, device ID, and verifying whether or not secured silicon is locked and whether or not a sector protected is the purpose of Automatic Select mode. There are four instruction cycles that comprise the Automatic Select mode. The first two cycles are write unlock commands, followed by the Automatic Select instruction (90h). The fourth cycle is a read cycle, and the user may read at any address any number of times without entering another instruction sequence. To exit the Automatic Select mode and back to read array, the Reset instruction is necessary. No other instructions are allowed except the Reset Instruction once Automatic Select mode has been selected. Refer to the following table for more detailed information.

			Address	Data (hex)	Representation
Manufacturer ID		Word	X00	01	
		Byte	X00	01	
Device ID	H/L	Word	X01/0E/0F	227E/221D/2201	
		Byte	X02/1C/1E	7E/1D/01	
	T/B	Word	X01/0E/0F	227E/221A/2201(T)/2200(B)	
		Byte	X02/1C/1E	7E/1A/01(T)/00(B)	
Secure Silicon		Word	X03	9A/1A(H)	Factory locked/unlocked
				8A/0A(L)	
		Byte	X06	9A/1A(H)	Factory locked/unlocked
				8A/0A(L)	
Sector Protect Verify		Word	(Sector address) X02	00/01	Unprotected/protected
		Byte	Sector address) X04	00/01	Unprotected/protected

Table 7-9 Auto Select for MFR/Device ID/Secure Silicon/Sector Protect Read

7.2.20 Enhanced Variable IO (EVIO) Control

The Enhanced Variable IO (EVIO) control allows the host system to set the voltage levels that the device generates and tolerates on all inputs and outputs (address, control, and DQ signals). EVIO range is 1.65 to VCC.

For example, a EVIO of 1.65-3.6 volts allows for I/O at the 1.8 or 3 volt levels, driving and receiving signals to and from other 1.8 or 3 V devices on the same data bus.

7.2.21 Hardware Data Protection Options

Hardware Data Protection is the second of the two main sector protections offered by the W29GL032.

7.2.21.1 #WP/ACC Option

By setting the #WP/ACC pin to VIL, the highest or lowest sector (device specific) is protected from all erase/program operations. If #WP/ACC is set High, the highest and Lowest sector revert back to the previous protected/unprotected state.

Note: The max input load current can increase, if #WP/ACC pin is at VIH when the device is put into standby mode.

7.2.21.2 VCC Write Protect

This device will not accept any write instructions when VCC is less that VWPT (VCC Write Protect Threshold)). This prevents data from inadvertently being altered during power-up, power-down, a temporary power loss or to the low level of VCC. If VCC is lower that VWPT, the device automatically resets itself and will ignore write cycles until VCC is greater than VWPT. Once VCC rises above VWPT, insure that the proper signals are on the control pins to avoid unexpected program or erase operations.

7.2.21.3 Write Pulse “Glitch” Protection

Pulses less than 5ns are viewed as glitches for control signals #CE, #WE, and #OE and will not be considered for valid write cycles.

7.2.21.4 Power-up Write Inhibit

The device ignores the first instruction on the rising edge of #WE, if upon powering up the device, #WE and #CE are set at VIL and #OE is set at VIH.

7.2.21.5 Logical Inhibit

A write cycle is ignored when either #CE is at VIH, #WE is at VIH, or #OE is at VIL. A valid write cycle requires both #CE and #WE are at VIL with #OE at VIH.

7.2.22 Inherent Data Protection

The device built-in mechanism will reset to Read mode during power up to avoid accidental erasure or programming.

7.2.22.1 Instruction Completion

Invalid instruction sets will result in the memory returning to read mode. Only upon a successful completion of a valid instruction set will the device begin its erase or program operation..

7.2.22.2 Power-up Sequence

The device is placed in Read mode, during power-up sequence.

7.2.23 Power Supply Decoupling

To reduce noise effects, a 0.1µF capacitor is recommended to be connected between VCC and GND.

7.3 Enhanced Sector Protect/Un-protect

This device is set from the factory in the Individual Protection mode of the Enhanced Sector Protect scheme. The user can disable or enable the programming or erasing operation to any individual sector or whole chip. The figure below helps describe an overview of these methods.

The device defaults to the Individual mode and all sectors are unprotected when shipped from the factory.

The following flow chart shows the detailed algorithm of Enhanced Sector Protect:

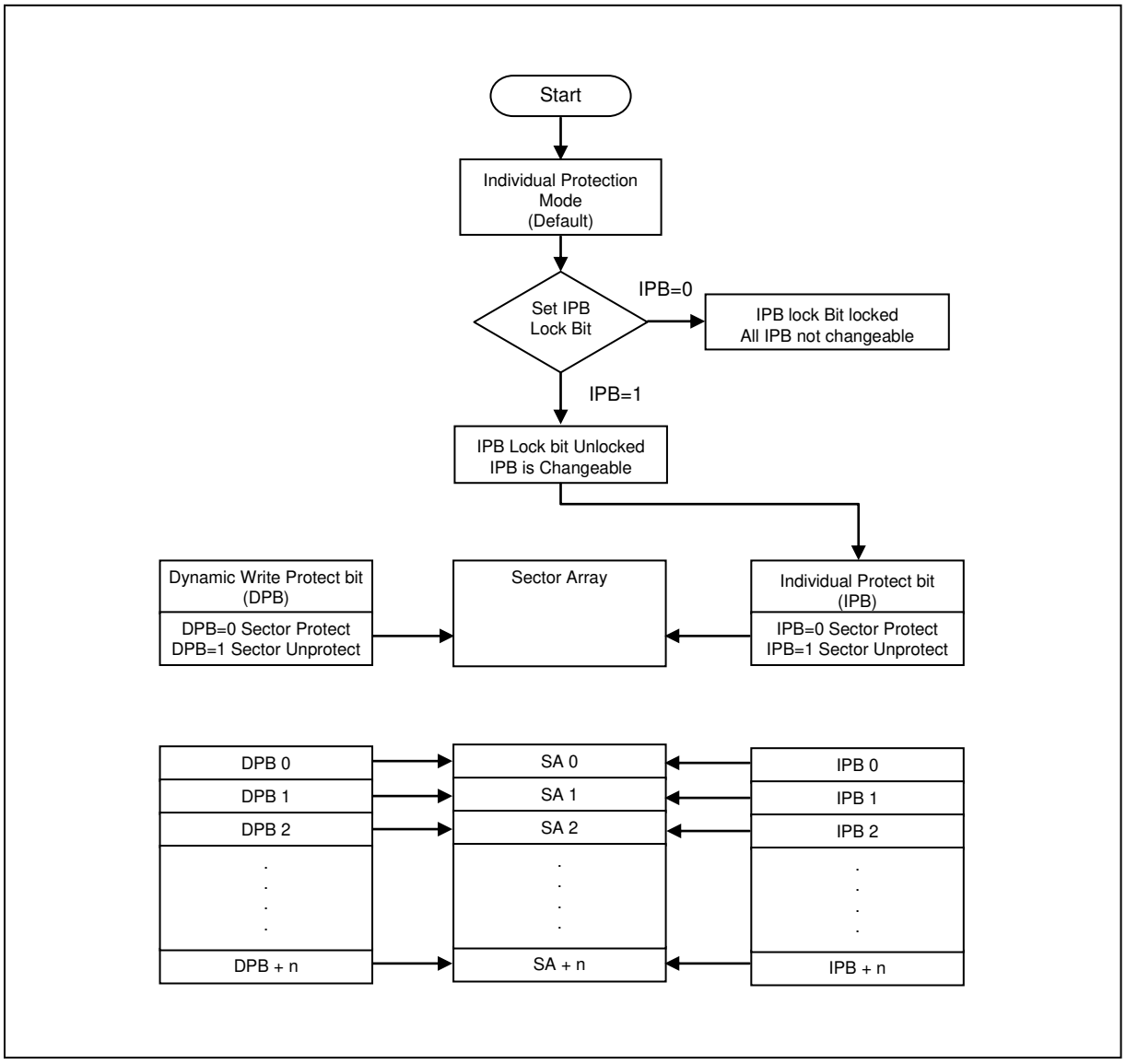

Figure 7-1 Enhanced Sector Protect/Un-protect IPB Program Algorithm

7.3.1 Lock Register

User can choose Secured Silicon Sector Protection Bit for security sector protection method via setting the Lock Register bit, DQ0. Lock Register is a 16-bit one time programmable register. Once programmed DQ0, will be locked in that mode permanently.

Once the Instruction Set Entry instruction sequence for the Lock Register Bits is issued, all sectors read and write functions are disabled until Lock Register Exit sequence has been executed.

The memory sectors and extended memory sector protection is configured using the Lock Register.

DQ[15:1]	DQ0
Don't Care	Secured Silicon Sector Protection Bit

Table 7-10 Lock Register Bits

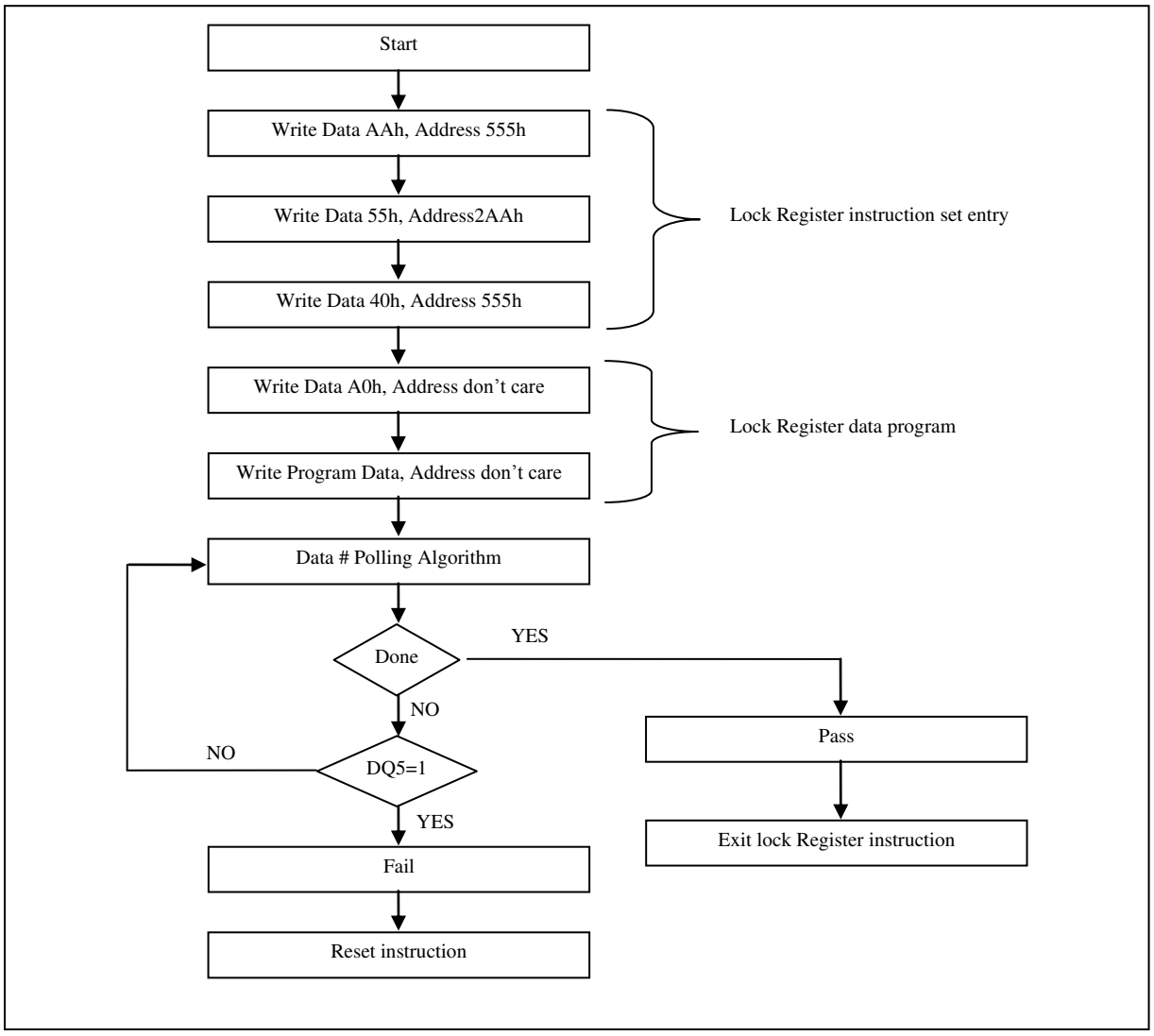

Figure 7-2 Lock Register Program Algorithm

7.3.2 Individual (Non-Volatile) Protection Mode

7.3.2.1 Individual Protection Bits (IPB)

The Individual Protection Bit (IPB) is a nonvolatile bit, one bit per sector, with endurance equal to that of the Flash memory array. Before erasing, IPB preprogramming and verification is managed by the device, so no monitoring is necessary.

The Individual Protection Bits are set sector by sector by the IPB program instruction. Once a IPB is set to "0", the linked sector is protected, blocking any program and/or erase functions on that sector. The IPB cannot be erased individually, but executing the "All IPB Erase" instruction will erase all IPB simultaneously. Read and write functions are disabled when IPB programming is going on for all sectors until this mode exits.

In case one of the protected sectors need to be unprotected, first, the IPB Lock Bit must be set to "1" by performing one of the following: power-cycle the device or perform a hardware reset. Second, an "All IPB Erase instruction needs to be performed. Third, Individual Protection Bits need to be set once again to reflect the desired settings and finally, the IPB Lock Bit needs to be set once again which locks the Individual Protection Bits and the device functions normally once again.

Executing an IPB Read instruction to the device is required to verify the programming state of the IPB for any given sector. Refer to the IPB Program Algorithm flow chart below for details.

Note that

- While IPB Lock Bit is set, Program and/or erase instructions will not be executed and times out without programming and/or erasing the IPB.
- For best protection results, it is recommended to execute the IPB Lock Bit Set instruction early on in the boot code. Also, protect the boot code by holding #WP/ACC = V_{IL}. Note that the IPB and DPB bits perform the same when #WP/ACC = V_{HH}, and when #WP/ACC =V_{IH}.
- While in the IPB command mode, read within that sector will bring the IPB status back for that sector. All Read must be executed by the read mode.
- Issuing the IPB Instruction Set Exit will reset the device to normal read mode enabling reads and writes for the array.

7.3.2.2 Dynamic Protection Bits (DPB)

Dynamic Protection allows the software applications to easily protect sectors against unintentional changes, although, the protection can be readily disabled when changes are needed.

All Dynamic Protection Bits (DPB) are individually linked to their associated sectors and these volatile bits can be modified individually (set or cleared). The DPB provide protection schemes for only unprotected sectors that have their associated IPB cleared. To change a DPB, the "DPB Instruction Set Entry" must be executed first and then either the DPB Set (programmed to "0") or DPB Clear (erased to "1") commands have to be executed. This places each sector in the protected or unprotected state separately. To exit the DPB mode, execute the "DPB Instruction Set Exit" instruction.

Note that

- When the parts are first shipped, the IPB are cleared (erased to "1") and upon power up or reset, the DPB can be set or cleared.

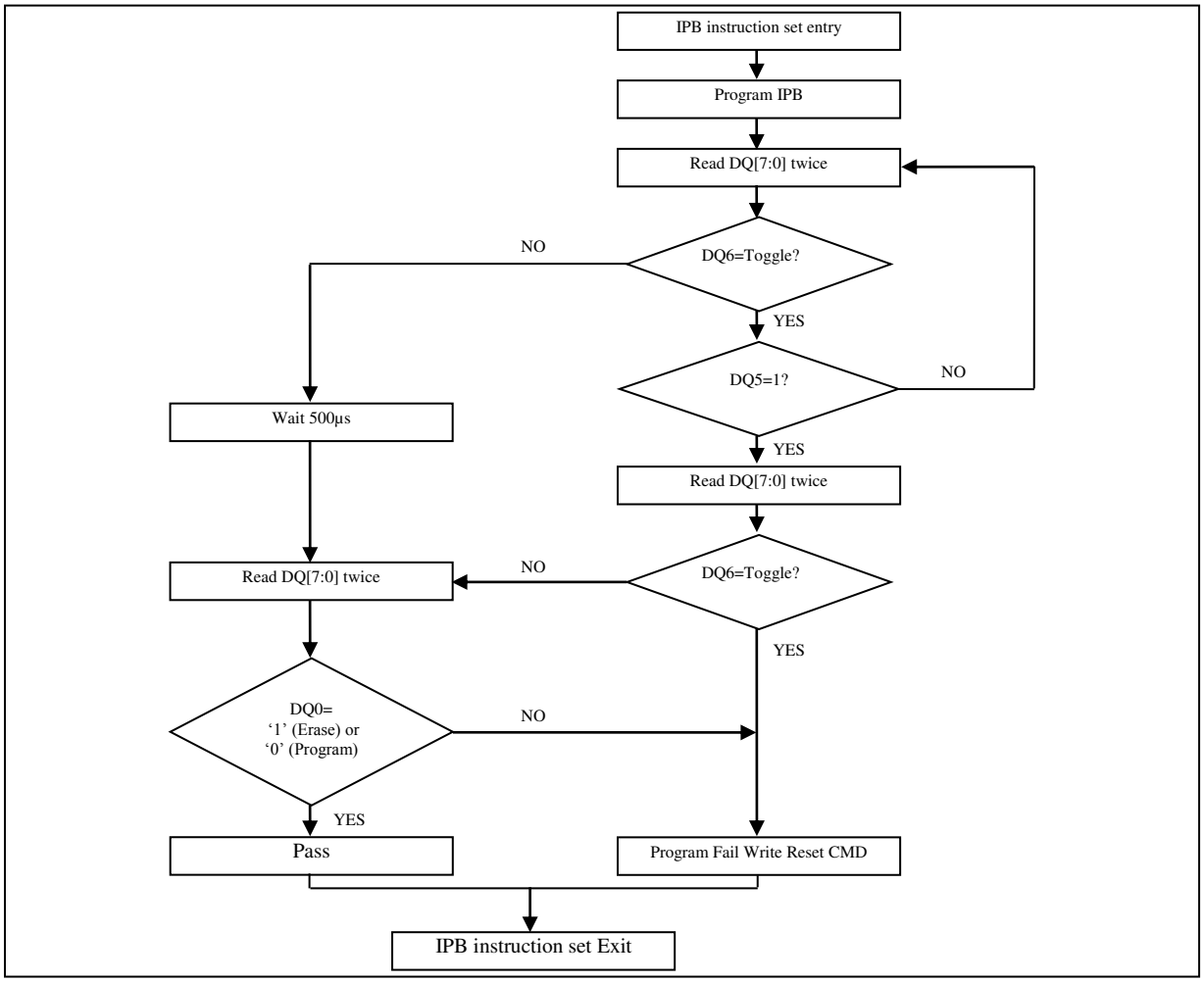

Figure 7-3 IPB Program Algorithm

Note:

1. IPB program/erase status polling flowchart: Check DQ6 toggle, when DQ6 stop toggle, the read status is 00h/01h (00h for program and 01h for erase, otherwise the status is "fail' and "exit".

7.3.2.3 Individual Protection Bit Lock Bit

The Individual Protection Bit Lock Bit (IPBLK) is a global lock bit to control all IPB states. It is a singular volatile bit. If the IPBLK is set ("0"), all IPB are locked and all sectors are protected or unprotected according to their individual IPB. When IPBLK=1 (cleared), all IPB are unlocked and allowed to be set or cleared.

To clear the IPB Lock Bit, a hardware reset or a power-up cycle must be executed.

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Sector Protection Status			Sector Status
DPB	IPBLK	IPB	
clear	clear	clear	Unprotect, DPB and IPB are changeable
clear	clear	set	Protect, DPB and IPB are changeable
clear	set	clear	Unprotect, DPB is changeable
clear	set	set	Protect, DPB is changeable
set	clear	clear	Protect, DPB and IPB are changeable
set	clear	set	Protect, DPB and IPB are changeable
set	set	clear	Protect, DPB is changeable
set	set	set	Protect, DPB is changeable

Table 7-11 Sector Protection Status Table