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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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256M-BIT
3.0-VOLT PARALLEL FLASH MEMORY WITH PAGE MODE

Publication Release Date: Jul 02, 2014
Revision C

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1 GENERAL DESCRIPTION

The W29GL256S Parallel Flash memory provides a storage solution for embedded system applications that require better performance, lower power consumption and higher density. This product fabricated on 58 nm process technology. This device offers a fast page access time as fast as 15ns with a corresponding random access time as fast as 90ns. It features a Write Buffer that allows a maximum of 256 words (512 bytes) to be programmed in one operation, resulting in faster effective programming time than standard programming algorithms. The W29GL256S also offers special features such as Compatible Manufacturer ID that makes the device industry standard compatible without the need to change firmware.

2 FEATURES

- 58 nm Technology
- x16 data bus
- 256-WORD (512-byte) Programming Buffer
  - Programming in Page multiples, up to a maximum of 512 bytes
- Asynchronous 32-byte Page Read
- Single word and multiple program on same word options
- Sector Erase
  - Uniform 128-kbyte sectors
- Enhanced Sector Protection (ESP)
- Volatile and non-volatile protection methods for each sector
- Security Sector Region
- 1024-byte One Time Program (OTP) array divided into two 512-Byte lockable regions
- Suspend and Resume commands for Program and Erase operations
- Status Register, Data Polling, and Ready/Busy pin methods to determine device status
- CFI (Common Flash Interface) support
- Single supply (VCC) for read / program / erase (2.7V to 3.6V)
- Enhanced Variable I/O Feature
  - Enhanced I/O voltage range (EVIO): 1.65V to VCC
- Wide Temperature Range (-40°C to +85°C)
- More than 100,000 erase/program cycles
- 20-year data retention typical
- Packaging Options
  - 56-pin TSOP, 14x20mm
  - 56-ball TFBGA, 7x9mm
  - 64-ball LFBGA, 13x11 mm

3 PIN CONFIGURATION

Figure 3-1 LFBGA64 TOP VIEW (Face Down)

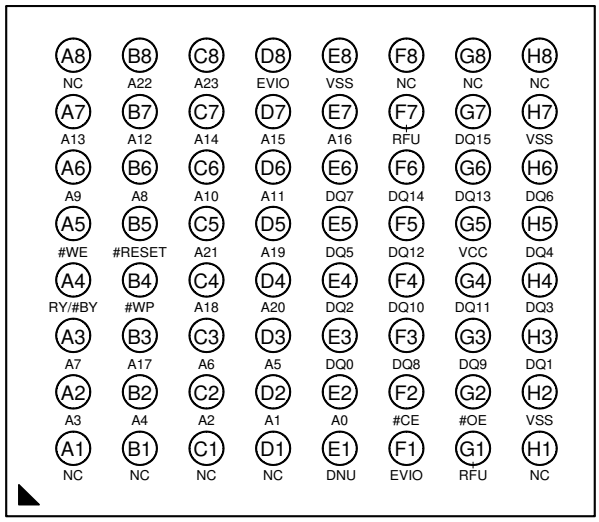


Figure 3-2 56-PIN STANDARD TSOP (Top View)

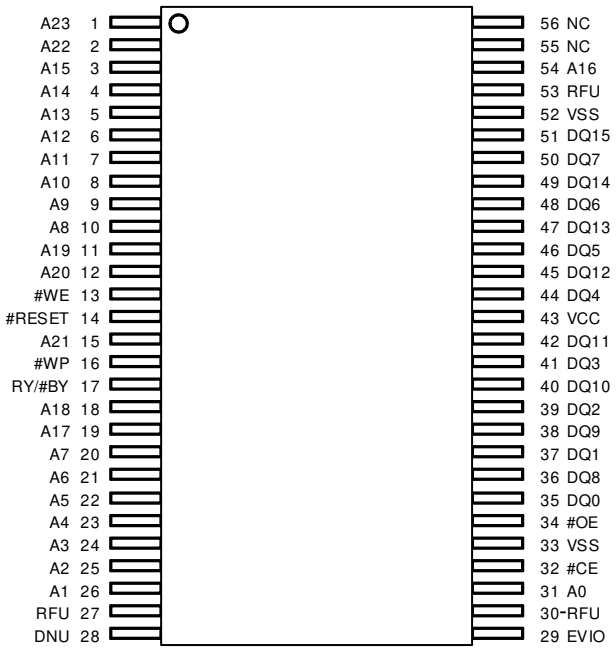
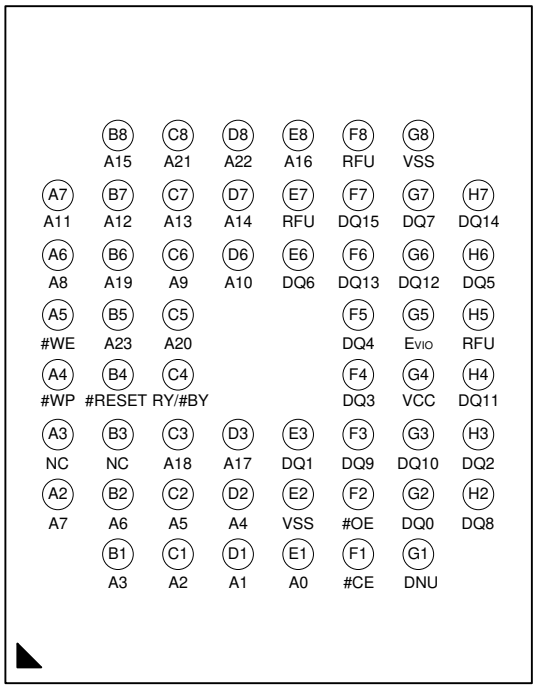
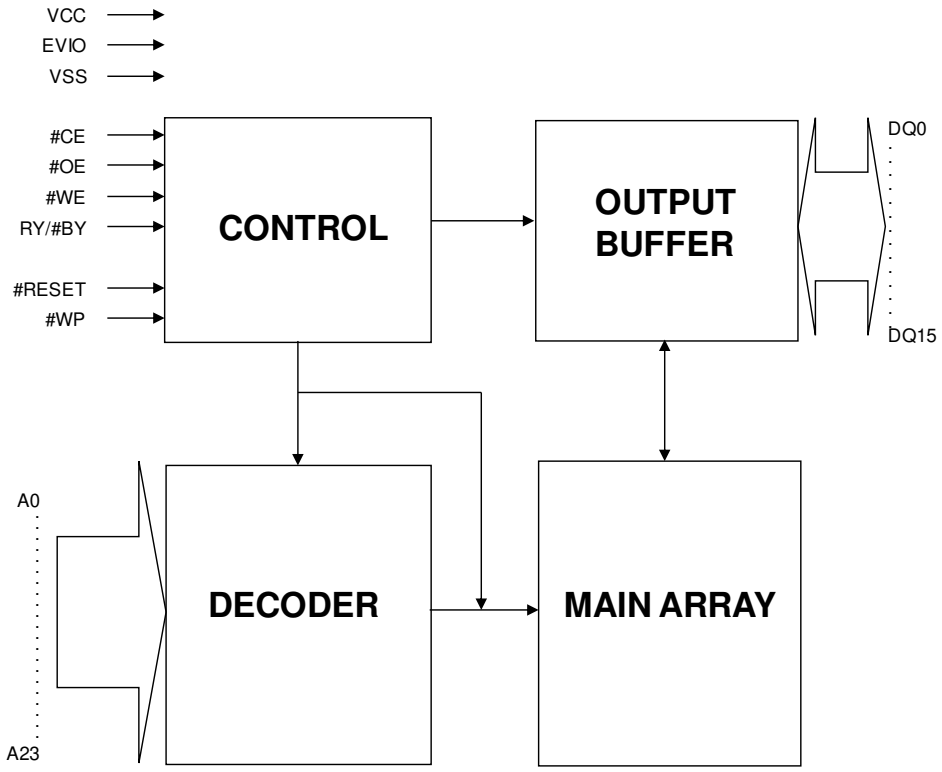


Figure 3-3 TFBGA56 TOP VIEW (Face Down)



4 BLOCK DIAGRAM

Figure 4-1 Simplified Block Diagram



5 PIN DESCRIPTION

Table 5-1 Pin Description

SYMBOL	SIGNAL TYPE	PIN NAME
A0-A23	Input	Address Inputs
DQ0-DQ15	I/O	Data Inputs/Outputs
#CE	Input	Chip Enable, Device selected at V_{IL}
#OE	Input	Output Enable, Output at V_{IL} and HIGH-Z at V_{IH}
#WE	Input	Write Enable, Write Mode at V_{IL} and Read Mode at V_{IH}
#WP	Input	Hardware Write Protect, Highest & Lowest Sector Protect at V_{IL}
#RESET	Input	Hardware Reset, device logic to standby and ready to read.
RY/#BY	Output	Ready/Busy Status, Indicates whether an Embedded Algorithm is in progress or complete. At V_{IL}, the device is actively engaged in an Embedded Algorithm such as erasing or programming. At HIGH-Z, the device is ready for read or a new command write - requires external pull-up resistor to detect the HIGH-Z state. Multiple devices may have their RY/#BY outputs tied together to detect when all devices are ready.
VCC	Power Supply	Power Supply
E_{VIO}	Power Supply	Enhanced Variable IO Supply
VSS	Power Supply	Ground
NC	-	No Connection

6 INTRODUCTION

The W29GL256S is a 3V, 256-Mbit, non-volatile, flash memory device with variable I/O. The device has a bus width of 16-bits (2-Bytes/1-Word) and word address boundaries are what are used. All read accesses provide 16 bits of data on every bus cycle. Every write cycle transfers 16 bits of data on the bus.

XIP and Data Storage flash memories are combined features of the W29GL256S. This enables the ability of fast programming speeds and reduced random access time of XIP flash in higher densities.

Read access to any random location takes 90 ns to 100 ns depending on device I/O power supply voltage. Each random access reads an aligned group of data of 32-bytes called a Page. Other words within the same Page may be read by changing only the low order 4 bits of word address. While in the same Page, access could take between 15 ns to 30 ns. This read operation is referred as Page Mode. Higher word address bits will select a different Page and begin another initial access. All read accesses are asynchronous.

The device control logic is divided into two parallel operating subsections, the Command State Machine (CSM) and the Write State Controller. Device level signals with the host system during read and write transfers are monitored by the CSM as needed for the inputs and drive outputs. CSM delivers data from the current entered address map on read operations; places write address and data information into the Write State Controller command memory; signals the Write State Controller of power level changes, write operations and hardware reset, The Write State Controller looks in the command memory, after a write operation, for correct command sequences and performs Internal Algorithms that are related.

Within the W29GL256S lie internal complex sequential operations or algorithms that are necessary to change the state of non-volatile data in the memory array. The internal Write State Controller manages all device algorithms. The main array data, programming and erasure are the main algorithms that are performed. When the host system sends command instructions to the flash device address space and Write State Controller receives these commands, provides status information during the progress of internal algorithms and performs all the necessary steps to complete the command.

A logical 1 bit is considered an erased cell. Changing a bit from a logical 1 to a logical 0 is considering programming. Note, only an erase operation is able to change a 0 to a 1. A restriction to an erase operation is a minimum of an entire sector (sector erase), which is a 128-kbyte aligned and length group of data is erased or the entire array can be erased (chip erase). Winbond ships the W29GL256S with all sectors erased.

The W29GL256S programming algorithm transfers volatile data from a write buffer to a non-volatile memory array line; this is called Write Buffer Programming. The size of the buffer is 256-Words (512-Bytes). 1 to 256 words can be written at any location in the Write Buffer prior to executing the programming operation. The programming operation can only be performed on an aligned group of 512 bytes in the flash array which is referred to as a Line.

After the completion of any Write Buffer operation or a reset, the buffer is refreshed to all 1's. By default any location that has not be written to a 0 are filled with 1's. Each page of data that was loaded into the Write Buffer during a programming operation, the memory array data is unaffected by 1's in the Write Buffer as it is transferred to a memory array Line.

Program and Erase operations may be affected by the Enhanced Sector Protection (ESP) methods, preventing any erasure or programming in a sector that may have been previously protected.

Table 6-1 W29GL256S Address Map

Addresses	Value	Description
A3 - A0	16	Word Selection
A7 - A0	256	Write Buffer Internal Address
A15 - A4	4096	Page Selection
A15 - A8	256	Write-Buffer-Line Selection
A23 - A16	256	Sector Selection

7 ARRAY ARCHITECTURE

There are several separate address spaces (i.e., Memory Map Overlay) that may appear within the address range of the flash memory device. Only one MMO can exist or be entered at a time.

- Main Memory Array
- This non-volatile area is used for storage of data that may be randomly accessed by asynchronous read operations.
- ID/CFI
- A Winbond factory programmed area for device characteristics information. It contains the Common Flash Interface (CFI) and Device Identification (ID) information tables.
- Security Sector Region (SSR)
- A Non-volatile / One Time Programmable (OTP) memory array used for Winbond factory and customer programmable permanent data.
- Lock Register
- This OTP non-volatile word is used to configure the Enhanced Sector Protection (ESP) features and lock the SSR.
- Individual Protection Bits (IPB):
- A non-volatile flash memory array with one bit for its associated sector. Programming this bit protects that sector from programming and erasure.
- IPB Lock
- Program and erase protection for the IPB bits. When the volatile register bit is enabled no programming or erasing of the IPB bits is prohibited.
- Dynamic Protection Bits (DPB)
- Similar to the IPB scheme, this volatile array with one bit for each sector can protect its associated sector from erasure and programming while the device is powered.
- Status Register
- Internal algorithm status monitoring can be done using this volatile register.
- Data Polling Status:
- Legacy software compatible volatile register used as an alternative to the Status Register to monitor internal algorithm status.

The Main Memory Array is the primary and default address space. This area at any time may be overlaid by one other address space. All the aforementioned address spaces are considered as a Memory Map Overlay (MMO). Each MMO replaces the entire address range of the main array. Addresses outside the current MMO address map are considered as not defined and are reserved for

future use. Read access is possible outside of an MMO address map and will return non-valid (undefined) data.

What appears in the flash device address space at any given time is one of four address map modes:

- Read Mode
- Memory Map Overlay (MMO) Mode
- Status Register (SR) Mode
- Data Polling Mode

In Read Mode the entire Flash Memory Array may be directly read. Read mode is entered during Power Up, after a Hardware Reset, Command Reset completion, or when an internal algorithm is suspended, all of which is controlled by the Write State Controller. While in the Read Mode, command accesses are permitted when an internal algorithm is suspended. There are subsets of commands that will be accepted in Read Mode while an Internal Algorithm is suspended.

The Status Register read command can be issued in any mode. This execution will cause the MMO of the Status Register to appear in the device address space at every word address location. To do this, the device interface waits for a read access, ignoring any write access. The content of the Status Register is presented at the next read access, after which it exits the Status Register MMO, and returns to the previous mode in which the Status Register read command was received.

While the Write State Controller is performing an internal algorithm, such as a non-volatile memory array program or an erase operation, none of the Main Memory Array is accessible because, the entire flash device address space is replaced by the MMO of the Data Polling Status at every word location in the device address space.

While in an internal algorithm operation, only the Status Register Read command or a Program / Erase suspend command will be accepted, ignoring all other commands. Hence, no other MMO may be entered.

The Data Polling MMO is visible during an internal algorithm operation and once a suspend command has been executed it is present up to the moment the device suspends the internal algorithm. When the internal algorithm is suspended the Data Polling MMO is exited and the Main Memory Array data is available again. The Data Polling MMO is activated again when the suspended internal algorithm operation is resumed. At the completion of an internal algorithm operation, the Data Polling MMO is exited and the device goes back to operation from which it was called.

As mentioned previously, only one MMO may exist at any one time. Device commands affect only the currently entered MMO. Not all commands are valid for each MMO. For a listed of valid commands, see the *Command Definition Tables* in MMO sections of the table.

Some MMOs have non-volatile data that can be programmed

- Individual Protection Bits (IPB), also erase capable
- Lock Register
- Security Sector Region

Operating in a non-volatile MMO mode while performing a program or erase command, the MMO is not readable while the internal algorithms is active. As soon as the function has completed, the MMO mode remains active and is again readable. Suspend and Resume commands are ignored for these non-volatile modes while these internal algorithms are active.

7.1 Flash Main Memory Array

The W29GL256S family is comprised of uniform 128KB sector size architecture. The table below shows the sector architecture of the W29GL256S device.

Table 7-1 W29GL256S Sector and Memory Address Map

Sector	Sector Address A23-A16	Sector Size (KByte)	X16 Start / Finish	
SA00	0000000	128	0000000h	000FFFFh
SA01	0000001	128	0010000h	001FFFFh
. . .	. . .	. . .	. . .	. . .
SA254	11111110	128	0FE0000h	0FEFFFFh
SA255	11111111	128	0FF0000h	0FFFFFFh

Note: This table has been reduced to show relative sector information for the entire device's individual sectors and their address ranges (sectors SA02-SA253 are not shown).

7.2 CFI and Device ID (CFI-ID)

There are two methods for systems to identify the type of flash memory installed in the system. The first method is called the Common Flash Interface (CFI). The second method called Autoselect, which is now referred to as Device Identification (ID).

Device Identification (ID), a command is used to enable a Memory Map Overlay where up to 16 word locations can be read to get JEDEC manufacturer identification (ID), device ID, and some configuration and protection status information from the flash memory.

The Common Flash Interface (CFI) command enables a Memory Map Overlay where a table of standard information about how the flash memory is organized and operates can be read.

Typically, these two address spaces have used separate commands and had separate overlays and are non-overlapping, so they actually can be combined in a single overlay. Either of these two commands can be used to access the combined Autoselect (ID) and CFI overlay.

The CFI-ID address map overlays the Flash Array data of the sector selected by the address used in the CFI-ID enter command. While the CFI-ID MMO is entered, the content of all other sectors is undefined. Address map starts at location 0 of the selected sector. Data is considered as undefined past the maximum defined address of the CFI-ID MMO to the maximum address of the selected sector.

To enter the Manufacturer ID (Autoselect) and Common Flash Interface (CFI) MMO command modes see the *Instruction Definition Table*.

Table 7-2 CFI-ID Address Map Overview

Word Address	Description	Read / Write
(SA) + 0000h to 000Fh	Device ID (traditional Autoselect values)	Read Only
(SA) + 0010h to 0079h	CFI data structure	Read Only
(SA) + 0080h to FFFFh	Undefined	Read Only

For the complete address map see the *Device ID and Common Interface Tables.*

7.3 Status Register

The Status Register, Memory Map Overlay (MMO) contains status for Internal Algorithms in a single volatile word format. When the read command for the Status Register is issued, status at the time of captured is presented in the register and the MMO is entered. All word locations in the device address space contain the Status Register information. Status Register exits the MMO mode after the first read access and returns to the address space map in use when the Status Register read command was issued.

7.4 Data Polling Status

The Data Polling Status, Memory Map Overlay (MMO) monitors the progress of Internal Algorithms which is contained in a single volatile word. Following the last write cycle of any command sequence that initiates an Internal Algorithms, the Data Polling Status will be entered. Internal Algorithms are initiated by one of the following commands:

- Blank Check
- Chip Erase
- Sector Erase
- Erase Resume / Program Resume
- Word Program
- Program Buffer to Flash
- Program Resume Enhanced Method
- Lock Register Program
- IPB Program
- All IPB Erase

At all word locations in the device address space, the Data Polling Status word appears. Data Polling Status MMO is exited and the device address space returns to the address map mode where the Internal Algorithms was started at the completion of the Internal Algorithms.

7.5 Sector Protection Control

7.5.1 Lock Register

The Lock Register, Memory Map Overlay (MMO) mode contains a single word of One Time Programmable (OTP) memory. When the MMO mode is entered the Lock Register appears at all word locations in the device address space. Winbond recommends for future compatibility to read or program the Lock Register only at location 0 of the device address space.

7.5.2 Individual Protection Bits (IPB)

The IPB, Memory Map Overlay (MMO) mode contains a non-volatile bit in each sector in the device. When the mode is entered, the IPB bit for a chosen sector appears in the Least Significant Bit (LSB) of each word in that sector. The non-volatile protection status for that sector is displayed by reading any word location, where the LSB indicates whether or not the sector is protected. The sector is protected against programming and erase operations if the bit is has been programmed to a 0. The sector is not protected by the IPB if the bit has been erased to a 1. Note; there are other features of

the Enhanced Sector Protection (ESP) that can protect sectors. Winbond recommends for future compatibility, to read or program the IPB only at word location 0 of the sector.

7.5.3 IPB Lock

The IPB Lock, Memory Map Overlay (MMO) contains a single volatile bit of memory. Programming or erasing of the IPB is controlled by IPB Lock. IPB is protected against programming and erase operations, if the bit is 0. The IPB is not protected, if the bit is 1. When the IPB Lock mode is entered, the IPB Lock bit appears in the Least Significant Bit (LSB) of each word in the device address space. Winbond recommends for future compatibility, to read or program the IPB Lock only at word location 0 of the device.

7.5.4 Dynamic Protection Bits (DPB)

The DPB Memory Map Overlay (MMO) contains one volatile bit of memory for each Sector. The DPB bit for a sector appears in the Least Significant Bit (LSB) of each word in the sector after entering the DPB mode. Reading any word in a sector displays the protection status for that sector. Sectors are protected during program and erase operations, if the DPB is 0 and unprotected if the bit is 1. Note there are other features of ESP that can protect the sector. Winbond recommends for future compatibility to read, set, or clear the DPB only at word location 0 of the sector.

8 FUNCTIONAL DESCRIPTIONS

8.1 Read

8.1.1 Random Read

The memory device is selected by driving Chip Enable (#CE) LOW and the device will leave the Standby mode. If Write Enable (#WE) is disabled, driven HIGH while #CE is LOW, a random read operation is started. The particular data output will depends on the MMO mode and the specific address provided.

The data output is presented on DQ15-DQ0 when #CE is LOW, Output Enable (#OE) is LOW, #WE is HIGH, address is stable, and the asynchronous access times are met. The Address access time (t_{ACC}) is defined to be equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is defined as the delay from a stable #CE to valid data on the outputs. The #OE signal must be LOW for at least the period of the output enable time (t_{OE}), before valid read data is available at the outputs.

Device outputs will provide valid read data from the currently active address map mode at the end of the random read access time from address stable (t_{ACC}), #OE active (t_{OE}), or #CE active (t_{CE}), whichever happens last.

A list of other transitional states during Random Read operation;

- A new random read access begins if #CE remains LOW and any Address[23:4] signals change to a new value.
- In order to get Back to Back accesses, requires an address change to initiate the second access and #CE to remains LOW between accesses Read mode with Outputs Disable, If #CE remains LOW and #OE goes .
- Write mode, if #CE remains LOW, #OE goes HIGH, and #WE goes LOW.
- Standby mode, if #CE returns HIGH.

8.1.2 Page Read

As in the Random Read mode, a random read access sequence is required. Then if #CE remains LOW, #OE remains LOW, Address[23:4] signals remains unchanged, and any of the Address[3:0] signals have change, then a new access within the same Page (32-byte) begins with data appearing on DQ15-DQ0. The Page Read is much faster (t_{PACC}) than a Random Read access. If #CE goes HIGH and returns LOW for another access, a random read access is performed and time is required (t_{ACC} or t_{CE}).

8.2 Device Reset Operations

The Hardware Reset (#RESET) input pin provides a hardware method of resetting the device to a standby mode. Immediately after issuing a Hardware Reset, driving #RESET LOW for at least a period of t_{RP}:

- Any operations in progress are terminated,
- Memory Map Overlays (MMO) is exited.
- All outputs are set to HIGH-Z.
- The Status Register is reset.
- The Write State Controller goes to the standby mode.
- #CE is ignored for a period of (tRPH), during the reset operation.
- #CE must be held HIGH to meet the Reset current specification (I_{CC5}).

Note: An operation that was interrupted should be reinitiated to ensure data integrity. An operation command sequence should be executed once the device is ready.

8.3 Standby Mode

Standby is the default, minimum power condition while the device is not selected (#CE = HIGH). All inputs are ignored in this mode and all outputs, except RY/#BY are at HIGH-Z. The Write State Controller direct output of the RY/#BY determines its state and is not controlled by other devices or interfaces.

8.4 Automatic Sleep

When addresses remain stable for t_{ACC} + 30 ns, the device will automatically enter the Auto Sleep mode and latches the output data. Data on the output pins depends on the level of the #OE signal. The automatic sleep mode is designed to reduce device interface current (I_{CC6}). #OE signal levels are independent of the automatic sleep mode current. The automatic sleep mode current (I_{CC6}) specifications can be found in the *DC Characteristics Tables*.

It's important to note that slow clock durations help reduce current consumption when the Automatic Sleep mode goes active. During slow clock periods, read and write cycles may extend many times their length versus when the clock is operating at high speed. Even when the chip enable is LOW throughout these extended data transfer cycles, the memory device Command State Machine (CSM) will enter the Automatic Sleep mode. This keeps the device in the Automatic Sleep power level for most of the extended duration of the data transfer cycles. Obviously this method is beneficial rather than consuming full read power all the time that the device is selected.

Note, the Write State Controller operates independent of the automatic sleep mode of the Command State Machine (CSM) and will continue to draw current during an active Internal Algorithm. Only when both entities are in their standby modes is the standby level current minimized.

8.5 Output Disable Mode

When the #CE signal is driven LOW, either a controlled read or write data transfer may begin. When there is a period at the start of a data transfer when Chip Enable is LOW, Address has become valid, #WE is HIGH and Output Enable (#OE) is HIGH. During this point a Random Read process is started while the data outputs remain at HIGH-Z (Output Disabled). Driving the #OE signal LOW, the device interface transitions to the Random Read mode and output data is actively driven. If in the event the Write Enable (#WE) signal is driven LOW, the device interface transitions to the Write mode. The host system interface should never drive #OE and #WE LOW at the same time; this will prevent conflicts with the device.

8.6 Program Methods

8.6.1 Asynchronous Write

When #WE goes LOW after CE is LOW, there is a transition from one of the read modes to the Write mode. If #WE is LOW before #CE goes LOW, there is a transition from the Standby mode directly to the Write mode without beginning a read access. At this point setting Output Enable (#OE) HIGH will start a write data transfer.

Address is captured by the falling edge of #WE or #CE, whichever occurs last. Data is captured by the rising edge of #WE or #CE, whichever occurs first.

A #WE controlled Write access is when the #CE goes LOW before #WE goes LOW and stays LOW after #WE goes HIGH. When #WE are HIGH and #CE goes HIGH, there is a transition to the Standby mode. If #CE remains LOW and #WE goes HIGH, there is a transition to the Read with Output Disable state.

A #CE controlled write mode is when #WE is LOW before #CE goes LOW, the write transfer is started by #CE going LOW. Then if #WE goes LOW after #CE goes HIGH, the address and data is latch by the rising edge of #CE.

Another #CE controlled write mode access is when #WE is LOW before #CE goes LOW and remains LOW after #CE goes HIGH. This is a #CE controlled Write transitions to the Standby mode.

An address change is required to initiate a Read access following a Write access, if #CE remains LOW between accesses.

An address change is required to initiate the second write access in a Back to Back write in which #CE remains LOW between accesses.

The Write State Controller command memory array is not readable by the host system and has no MMO. Its purpose is to examine the address and data in each write transfer to determine if the write is a legal command sequence. If the command sequence is correct, the Write State Controller will initiate the appropriate Internal Algorithms.

8.6.2 Word Programming

Word programming programs a single word anywhere in the Main Memory Array.

The Word Programming command is a four write cycle sequence. This is done by writing the unlock write command in the first two cycles, a program set up command in the third cycle and finally, in the

fourth cycle the program address and data are written. This will initiate the Internal Word Program algorithm. No further input controls are required. The Internal Algorithm generates all the programming pulses and programmed cell verifications. When the Internal Word Program algorithm is complete, the Write State Controller then returns to its standby mode.

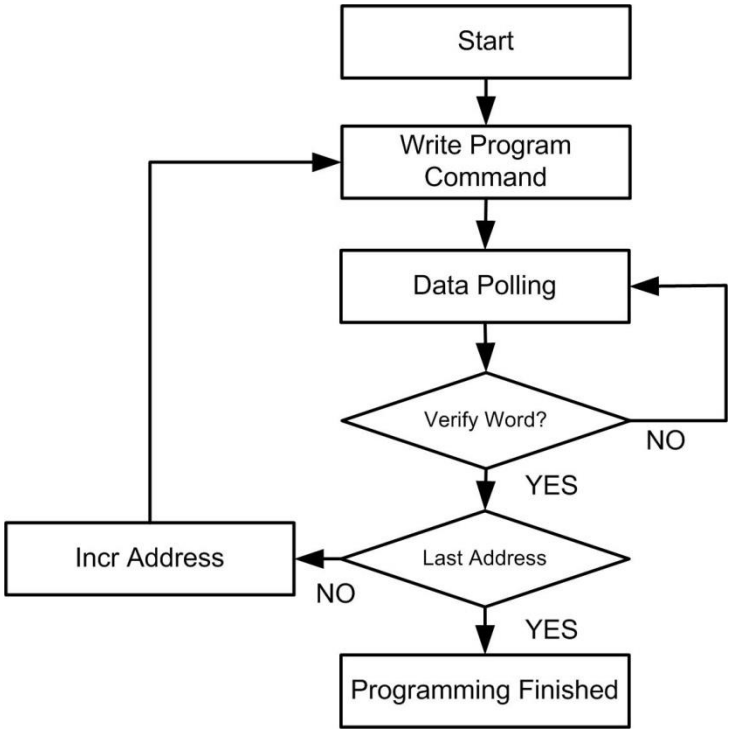
Program operation status can be determined by monitoring the RY/#BY output, reading the Status Register, or by using Data Polling Status.

Program Suspend is the only command that can be written to the device during the Internal Program Algorithm, all others are ignored. However, a hardware reset (#RESET = V_{IL}) will immediately terminates the programming operation. Then after t_{RPH} time, returns the device to read mode. It is recommended to reinitiate the Word Program command sequence after the device has completed the hardware reset operation to insure data integrity.

The Security Sector Region (SSR) mode may also use the Word Programming command when is entered.

The Word Programming command has a modified version without unlock write cycles when it is used for programming the Lock Register and IPB MMOs. The same command is also used to change volatile bits when entered in to the IPB Lock, and DPB MMOs. See the *Instruction Definition Tables* for program command sequences.

Figure 8-1 Word Program Operation



8.6.3 Write Buffer Programming

A 512-byte address range write buffer is used to program data within an aligned 512-byte boundary Line, (example, addresses: 100h to 1FFh). Hence, a Write Buffer Programming operation must be setup on a Line boundary. If the Programming operation is less than 512-bytes, it may start on any word boundary, but may not cross a Write-Buffer-Line boundary. All bit locations in the buffer at the start of a Write Buffer programming operation are in the One's state (FFFFh/Word). Thus, any locations not loaded will retain the existing data.

The Main Memory Array and the Secure Sector Region (SSR) are the areas that are supported by the Write Buffer Programming operation. It is possible to program from 1 bit, up to 512 bytes in one Write Buffer Programming operation. The recommended write buffer method is to only write each page once in a multi-page scenario. Programming should be done in full Lines of 512 bytes setup on 512-byte boundaries, for the very best performance.

To initiate a Write Buffer Programming operation, the first 2 cycles are the unlock write commands. The 3rd write cycle contains the Write to Buffer command with the program targeted Sector Address (SA). The fourth cycle is to write the number of planned word locations minus 1. This will indicate the