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W29N04GW/Z
4G-BIT 1.8V
NAND FLASH MEMORY

winbond

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1. GENERAL DESCRIPTION

The W29N04GW/Z (4G-bit) NAND Flash memory provides a storage solution for embedded systems with limited space, pins and power. It is ideal for code shadowing to RAM, solid state applications and storing media data such as, voice, video, text and photos. The device operates on a single 1.7V to 1.95V power supply with active current consumption as low as 13mA at 1.8V and 10uA for CMOS standby current.

The memory array totals 553,648,128 bytes, and organized into 4,096 erasable blocks of 135,168 bytes (67,584 words). Each block consists of 64 programmable pages of 2,112-bytes (1056 words) each. Each page consists of 2,048-bytes (1024 words) for the main data storage area and 64-bytes (32words) for the spare data area (The spare area is typically used for error management functions).

The W29N04GW/Z supports the standard NAND flash memory interface using the multiplexed 8-bit (16-bit) bus to transfer data, addresses, and command instructions. The five control signals, CLE, ALE, #CE, #RE and #WE handle the bus interface protocol. Also, the device has two other signal pins, the #WP (Write Protect) and the RY/#BY (Ready/Busy) for monitoring the device status.

2. FEATURES

- **Basic Features**
  - Density : 4Gbit (Single chip solution)
  - Vcc : 1.7V to 1.95V
  - Bus width : x8 x16
  - Operating temperature
    - Industrial: -40°C to 85°C
- **Single-Level Cell (SLC) technology.**
- **Organization**
  - Density: 4G-bit/512M-byte
  - Page size
    - 2,112 bytes (2048 + 64 bytes)
    - 1,056 words (1024 + 32 words)
  - Block size
    - 64 pages (128K + 4K bytes)
    - 64 pages (64K + 2K words)
- **Highest Performance**
  - Read performance (Max.)
    - Random read: 25us
    - Sequential read cycle: 25ns
  - Write Erase performance
    - Page program time: 250us(typ.)
    - Block erase time: 2ms(typ.)
  - Endurance 100,000 Erase/Program Cycles(1)
  - 10-years data retention
- **Command set**
  - Standard NAND command set
  - Additional command support
    - Copy Back
    - Two-plane operation
  - Contact Winbond for OTP feature
  - Contact Winbond for Block Lock feature
- **Lowest power consumption**
  - Read: 13mA(typ.)
  - Program/Erase: 10mA(typ.)
  - CMOS standby: 10uA(typ.)
- **Space Efficient Packaging**
  - 48-pin standard TSOP1
  - 63-ball VFBGA
  - Contact Winbond for stacked packages/KGD

Note:

1. **Endurance specification is based on 1bit/528 byte ECC (Error Correcting Code).**

3. PACKAGE TYPES AND PIN CONFIGURATIONS

W29N04GW/Z is offered in a 48-pin TSOP1 package (code S), 63-ball VFBGA package (Code B) as shown in Figure 3-1 and 3-3, respectively. Package diagrams and dimensions are illustrated in Section: Package Dimensions.

3.1 Pin Assignment 48 pin TSOP1 (x8)

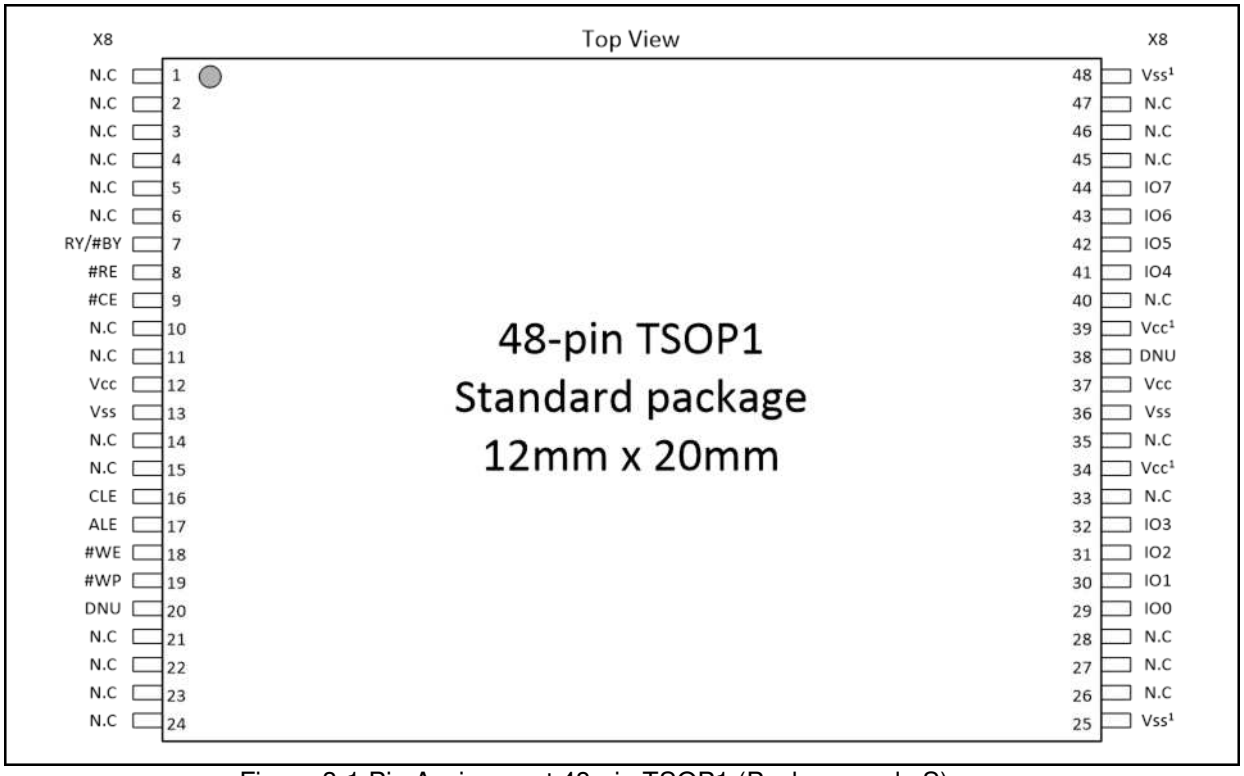

Figure 3-1 Pin Assignment 48-pin TSOP1 (Package code S)

Note:

1. **These pins might not be connected in the package. Winbond recommends connecting these pins to the designed external sources for ONFI compatibility.**

3.2 Pin Assignment 63 ball VFBGA (x8)

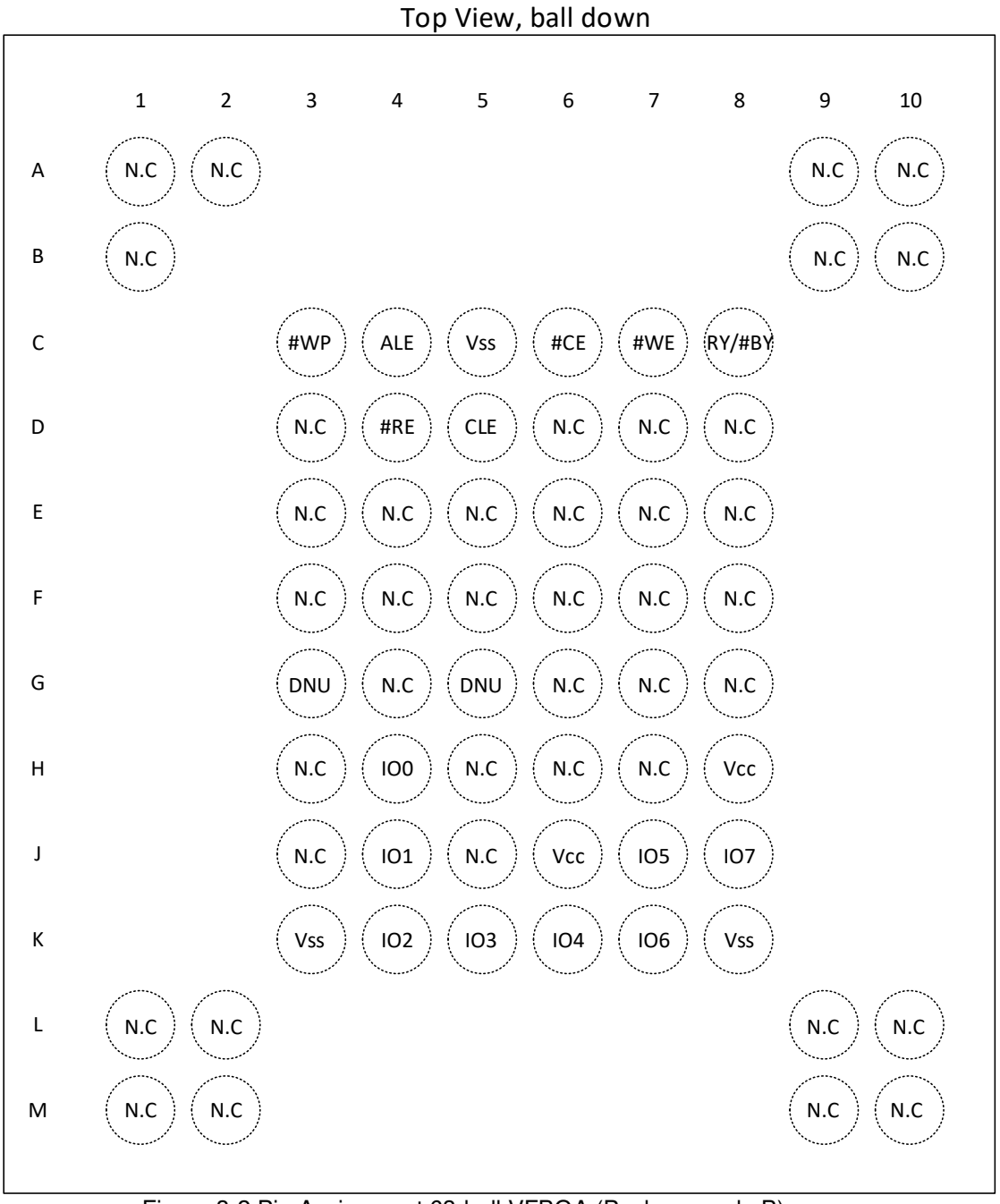

Figure 3-2 Pin Assignment 63-ball VFBGA (Package code B)

3.3 Pin Assignment 63 ball VFBGA (x16)

Top View, ball down

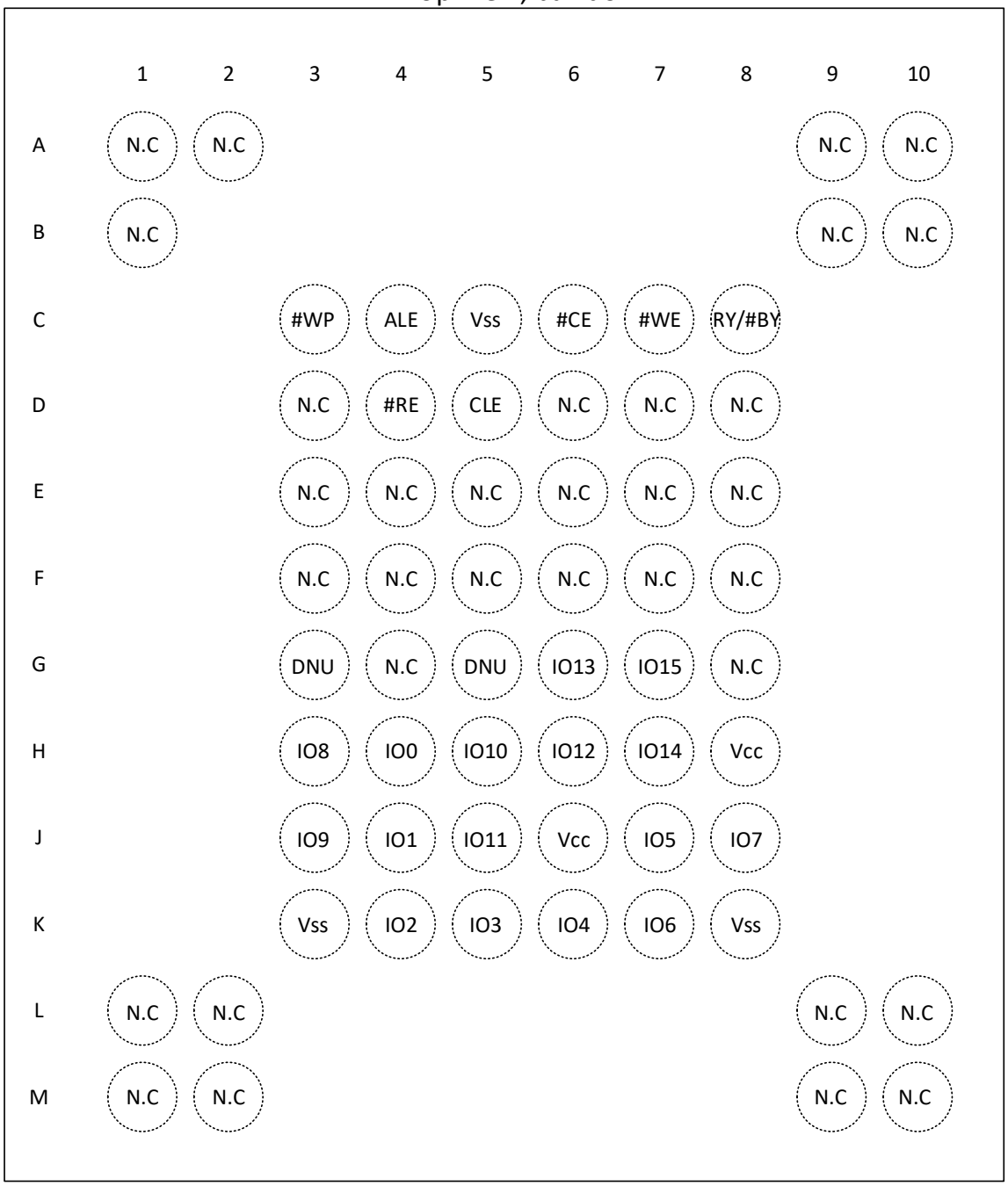

Figure 3-3 Pin Assignment 63-ball VFBGA (Package code B)

3.4 Pin Descriptions

PIN NAME	I/O	FUNCTION
#WP	I	Write Protect
ALE	I	Address Latch Enable
#CE	I	Chip Enable
#WE	I	Write Enable
RY/#BY	O	Ready/Busy
#RE	I	Read Enable
CLE	I	Command Latch Enable
I/O[0-7] I/O[0-15]	I/O	Data Input/Output (x8,x16)
Vcc	Supply	Power supply
Vss	Supply	Ground
DNU	-	Do Not Use: DNUs must be left unconnected.
N.C	-	No Connect

Table 3-1 Pin Descriptions

Note:

1. **Connect all Vcc and Vss pins to power supply or ground. Do not leave Vcc or Vss disconnected.**

4. PIN DESCRITPIONS

4.1 Chip Enable (#CE)

#CE pin enables and disables device operation. When #CE is high the device is disabled and the I/O pins are set to high impedance and enters into standby mode if not busy. When #CE is set low the device will be enabled, power consumption will increase to active levels and the device is ready for Read and Write operations.

4.2 Write Enable (#WE)

#WE pin enables the device to control write operations to input pins of the device. Such as, command instructions, addresses and data that are latched on the rising edge of #WE.

4.3 Read Enable (#RE)

#RE pin controls serial data output from the pre-loaded Data Register. Valid data is present on the I/O bus after the tREA period from the falling edge of #RE. Column addresses are incremented for each #RE pulse.

4.4 Address Latch Enable (ALE)

ALE pin controls address input to the address register of the device. When ALE is active high, addresses are latched via the I/O pins on the rising edge of #WE.

4.5 Command Latch Enable (CLE)

CLE pin controls command input to the command register of the device. When CLE is active high, commands are latched into the command register via I/O pins on the rising edge of #WE.

4.6 Write Protect (#WP)

#WP pin can be used to prevent the inadvertent program/erase to the device. When #WP pin is active low, all program/erase operations are disabled.

4.7 Ready/Busy (RY/#BY)

RY/#BY pin indicates the device status. When RY/#BY output is low, it indicates that the device is processing either a program, erase or read operations. When it returns to high, those operations have completed. RY/#BY pin is an open drain.

4.8 Input and Output (I/Ox)

I/Ox bi-directional pins are used for the following; command, address and data operations.

5. BLOCK DIAGRAM

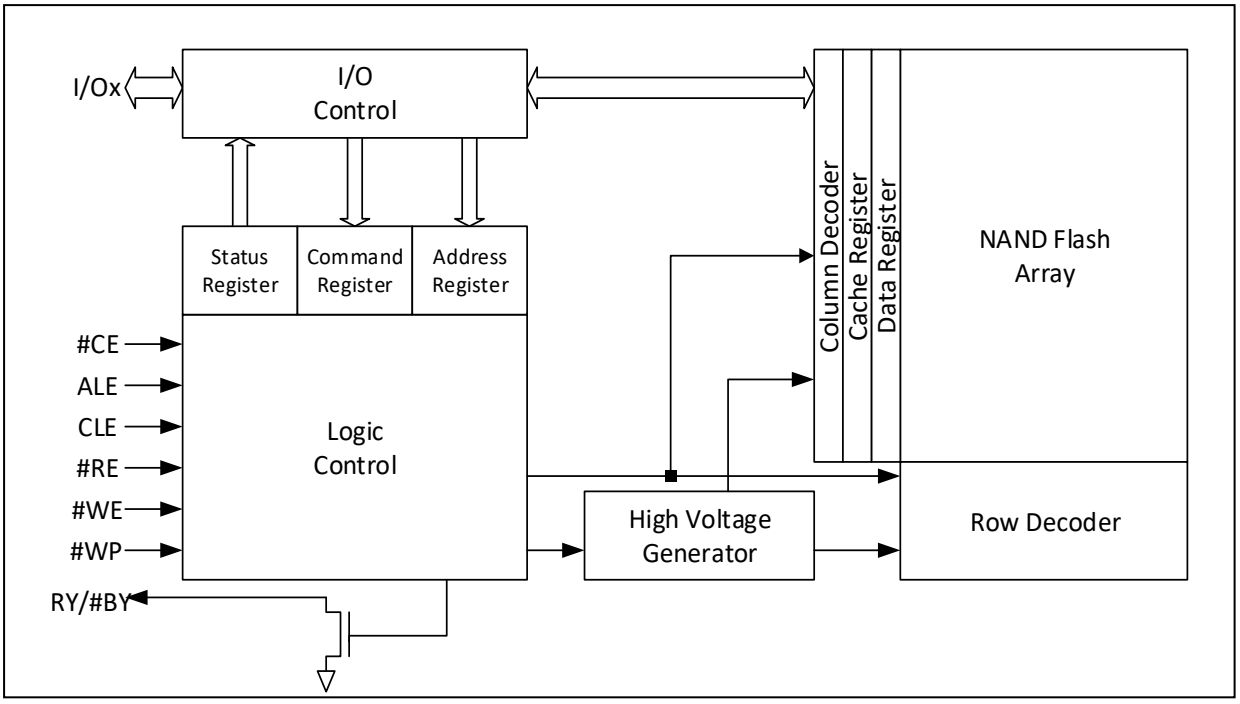

Figure 5-1 NAND Flash Memory Block Diagram

6. MEMORY ARRAY ORGANIZATION

6.1 Array Organization (x8)

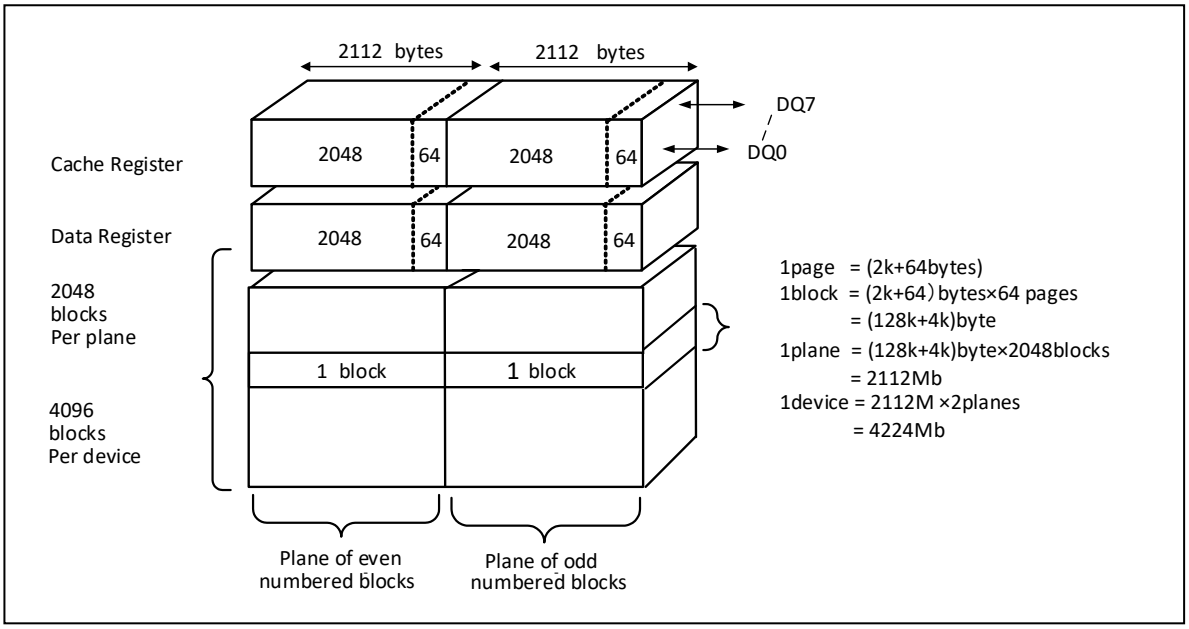

Figure 6-1 Array Organization

	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st cycle	A7	A6	A5	A4	A3	A2	A1	A0
2nd cycle	L	L	L	L	A11	A10	A9	A8
3rd cycle	A19	A18	A17	A16	A15	A14	A13	A12
4th cycle	A27	A26	A25	A24	A23	A22	A21	A20
5th cycle	L	L	L	L	L	L	A29	A28

Table 6-1 Addressing

Notes:

1. **"L" indicates a low condition, which must be held during the address cycle to insure correct processing.**
2. **A0 to A11 during the 1st and 2nd cycles are column addresses. A12 to A29 during the 3rd, 4th and 5th cycles are row addresses.**
3. **A18 is plane address**
4. **The device ignores any additional address inputs that exceed the device's requirement.**

6.2 Array Organization (x16)

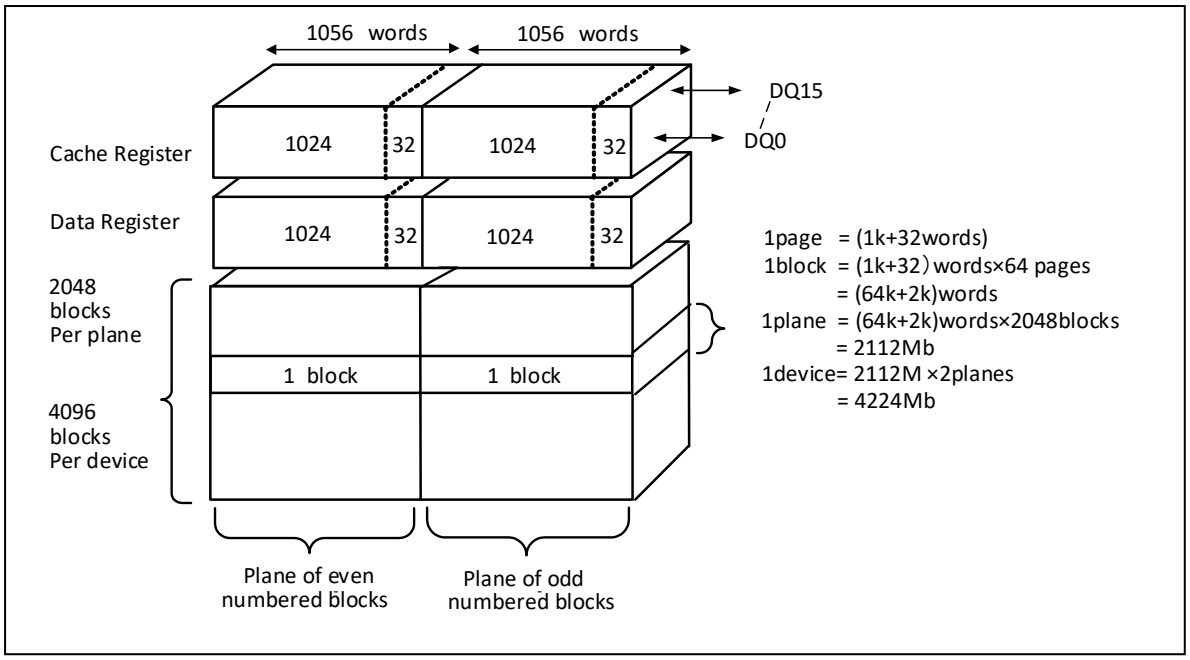

Figure 6-2 Array Organization

	I/O[15:8]	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st cycle	L	A7	A6	A5	A4	A3	A2	A1	A0
2ndcycle	L	L	L	L	L	L	A10	A9	A8
3rd cycle	L	A18	A17	A16	A15	A14	A13	A12	A11
4th cycle	L	A26	A25	A24	A23	A22	A21	A20	A19
5th cycle	L	L	L	L	L	L	L	A28	A27

Table 6-2 Addressing

Notes:

1. **"L" indicates a low condition, which must be held during the address cycle to insure correct processing.**
2. **A0 to A10 during the 1st and 2nd cycles are column addresses. A11 to A28 during the 3rd, 4th and 5th cycles are row addresses.**
3. **A17 is plane address**
4. **The device ignores any additional address inputs that exceed the device's requirement.**

7. MODE SELECTION TABLE

MODE		CLE	ALE	#CE	#WE	#RE	#WP
Read mode	Command input	H	L	L		H	X
	Address input	L	H	L		H	X
Program Erase mode	Command input	H	L	L		H	H
	Address input	L	H	L		H	H
Data input		L	L	L		H	H
Sequential Read and Data output		L	L	L	H		X
During read (busy)		X	X	X	X	H	X
During program (busy)		X	X	X	X	X	H
During erase (busy)		X	X	X	X	X	H
Write protect		X	X	X	X	X	L
Standby		X	X	H	X	X	0V/Vcc

Table 7-1 Mode Selection

Notes:

1. **"H" indicates a HIGH input level, "L" indicates a LOW input level, and "X" indicates a Don't Care Level.**
2. **#WP should be biased to CMOS HIGH or LOW for standby.**

8. COMMAND TABLE

COMMAND	1ST CYCLE	2ND CYCLE	3rd CYCLE	4th CYCLE	Acceptable during busy
PAGE READ	00h	30h			
READ for COPY BACK	00h	35h			
READ ID	90h				
READ STATUS	70h				Yes
RESET	FFh				Yes
PAGE PROGRAM	80h	10h			
PROGRAM for COPY BACK	85h	10h			
BLOCK ERASE	60h	D0h			
RANDOM DATA INPUT*1	85h				
RANDOM DATA OUTPUT*1	05h	E0h			
READ PARAMETER PAGE	ECh				
READ UNIQUE ID	EDh				
GET FEATURES	EEh				
SET FEATURES	EFh				
READ STATUS ENHANCED	78h				Yes
TWO PLANE READ PAGE	00h	00h	30h		
TWO PLANE READ FOR COPY BACK	00h	00h	35h		
TWO PLANE RANDOM DATA READ	06h	E0h			
TWO PLANE PROGRAM(TRADITIONAL)	80h	11h	81h	10h	
TWO PLANE PROGRAM(ONFI)	80h	11h	80h	10h	
TWO PLANE PROGRAM FOR COPY BACK(TRADITIONAL)	85h	11h	81h	10h	
TWO PLANE PROGRAM FOR COPY BACK(ONFI)	85h	11h	85h	10h	
TWO PLANE BLOCK ERASE(TRADITIONAL)	60h	60h	D0h		
TWO PLANE BLOCK ERASE(ONFI)	60h	D1h	60h	D0h	

Table 8-1 Command Table

Notes:

1. **RANDOM DATA INPUT and RANDOM DATA OUTPUT command is only to be used within a page.**
2. **Any commands that are not in the above table are considered as undefined and are prohibited as inputs.**
3. **Do not cross plane address boundaries when using Copy Back Read and Program for copy back.**

9. DEVICE OPERATIONS

9.1 READ operation

9.1.1 PAGE READ (00h-30h)

When the device powers on, 00h command is latched to command register. Therefore, system only issues five address cycles and 30h command for initial read from the device. This operation can also be entered by writing 00h command to the command register, and then write five address cycles, followed by writing 30h command. After writing 30h command, the data is transferred from NAND array to Data Register during tR. Data transfer progress can be done by monitoring the status of the RY/#BY signal output. RY/#BY signal will be LOW during data transfer. Also, there is an alternate method by using the READ STATUS (70h) command. If the READ STATUS command is issued during read operation, the Read (00h) command must be re-issued to read out the data from Data Register. When the data transfer is complete, RY/#BY signal goes HIGH, and the data can be read from Data Register by toggling #RE. Read is sequential from initial column address to the end of the page. (See Figure 9-1)

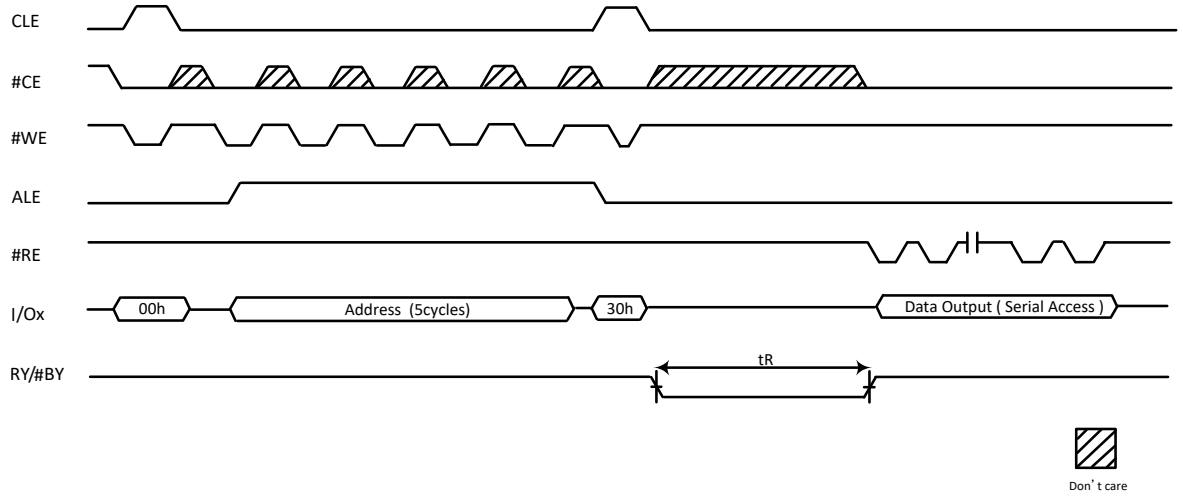

Figure 9-1 Page Read Operations

9.1.2 TWO PLANE READ (00h-00h-30h)

TWO PLANE READ (00h-00h-30h) transfers two pages data from the NAND array to the data registers. Each page address have to be indicated different plane address.

To set the TWO PLANE READ mode, write the 00h command to the command register, and then write five address cycles for plane 0. Secondly, write the 00h command to the command register, and five address cycles for plane 1. Finally, the 30h command is issued. The first-plane and second-plane addresses must be identical for all of issued address except plane address.

After the 30h command is written, page data is transferred from both planes to their respective data registers in tR. RY/#BY goes LOW While these are transfered,. When the transfers are complete, RY/#BY goes HIGH. To read out the data, at first, system writes TWO PLANE RAMDOM DATA READ (06h-E0h) command to select a plane, next, repeatedly pulse #RE to read out the data from selected plane. To change the plane address, issues TWO PLANE RANDOM DATA READ (06h-E0h)

command to select the another plane address, then repeatedly pulse #RE to read out the data from the selected plane data register.

Alternatively, data transfers can be monitored by the READ STATUS (70h). When the transfers are complete, status register bit 6 is set to 1. To read data from the first of the two planes even when READ STATUS ENHANCED (78h) command is used, the system must issue the TWO PLANE RANDOM DATA READ (06h-E0h) command at first and pulse #RE repeatedly.

Write a TWO PLANE RANDOM DATA READ (06h-E0h) command to select the other plane ,after the data cycle is complete. pulse #RE repeatedly to output the data beginning at the specified column address. During TWO PLANE READ operation,the READ STATUS ENHANCED (78h) command is prohibited .

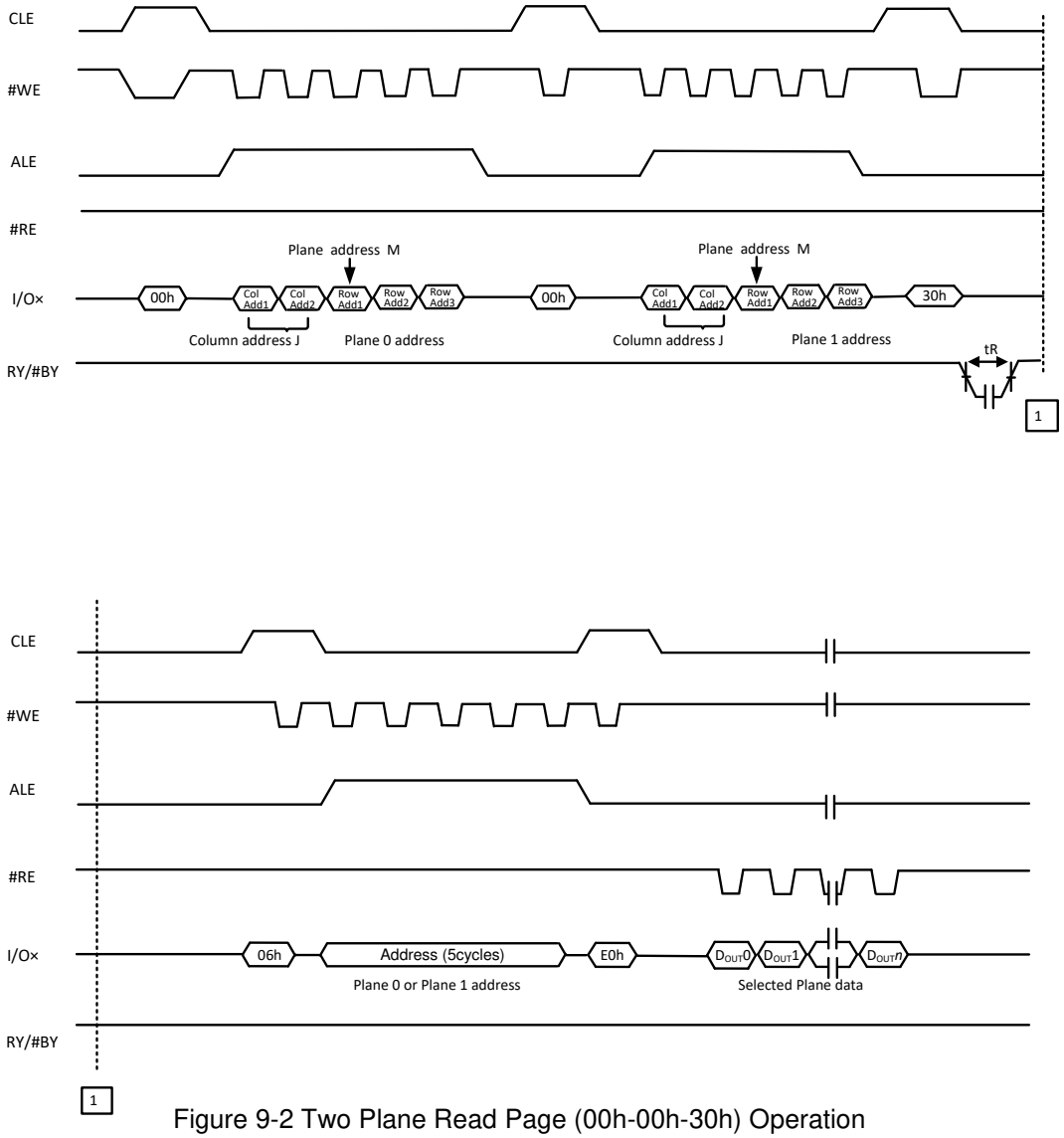

Figure 9-2 Two Plane Read Page (00h-00h-30h) Operation

9.1.3 RANDOM DATA OUTPUT (05h-E0h)

The RANDOM DATA OUTPUT allows the selection of random column addresses to read out data from a single or multiple of addresses. The use of the RANDOM DATA OUTPUT command is available after the PAGE READ (00h-30h) sequence by writing the 05h command following by the two cycle column address and then the E0h command. Toggling #RE will output data sequentially. The RANDOM DATA OUTPUT command can be issued multiple times, but limited to the current loaded page.

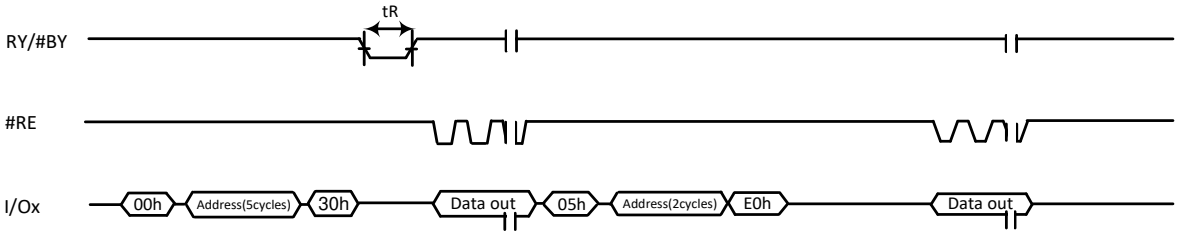

Figure 9-3 Random Data Output

9.1.3.1. TWO PLANE RANDOM DATA OUTPUT (06h-E0h)

TWO PLANE RANDOM DATA READ (06h-E0h) command can indicate to specified plane and column address on data register . This command is accepted by a device when it is ready.

Issuing 06h to the command register, two column address cycles, three row address cycles, E0h are followed, this enables data output mode on the address device's data register at the specified column address. After the E0h command , the host have to wait at least tWHR before requesting data output. The selected device is in data output mode until another valid command is issued.

The TWO PLANE RANDOM DATA READ (06h-E0h) command is used to select the data register to be enabled for data output. When the data output is complete on the selected plane, the command can be issued again to start data output on another plane.

If there is a need to update the column address without selecting a new data register, the RANDOM DATA READ (05h-E0h) command can be used instead.

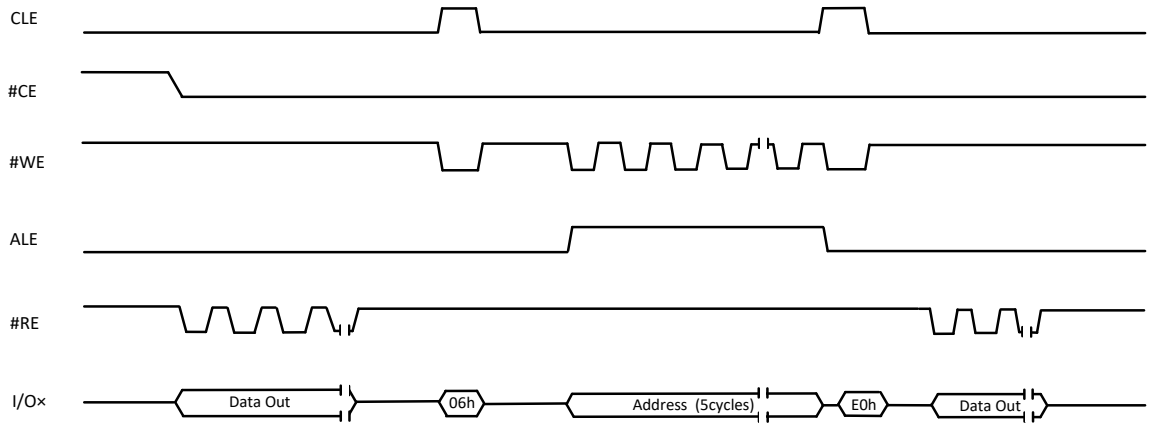

Figure 9-4 Two Plane Random Data Read (06h-E0h) Operation

9.1.4 READ ID (90h)

READ ID command is comprised of two modes determined by the input address, device (00h) or ONFI (20h) identification information. To enter the READ ID mode, write 90h to the Command Register followed by a 00h address cycle, then toggle #RE for 5 single byte cycles, W29N04GW/Z. The pre-programmed code includes the Manufacturer ID, Device ID, and Product-Specific Information (see Table 9.1). If the READ ID command is followed by 20h address, the output code includes 4 single byte cycles of ONFI identifying information (See Table 9.2). The device remains in the READ ID Mode until the next valid command is issued.

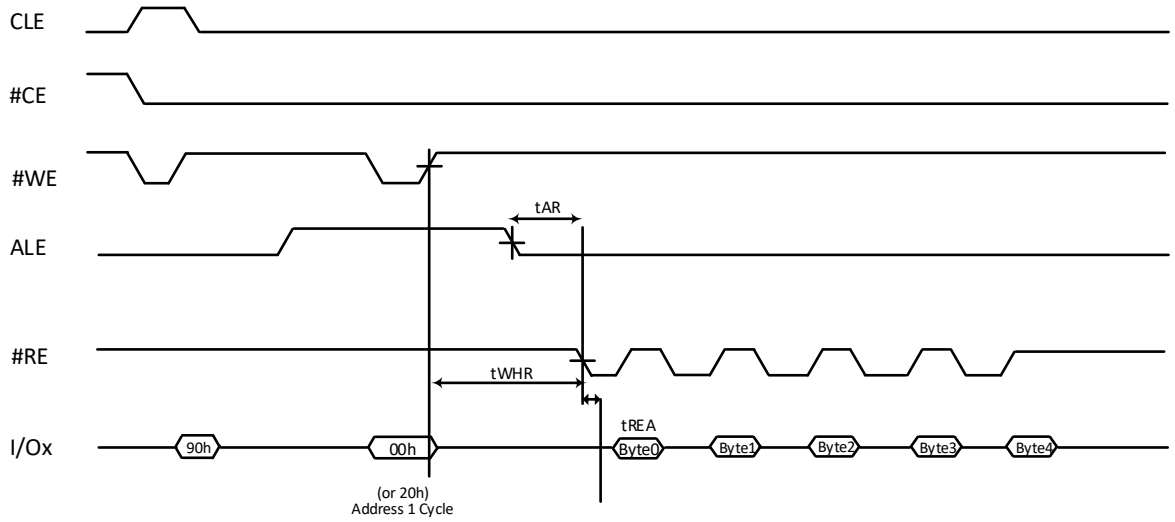

Figure 9-5 Read ID

# of Byte/Cycles	1st Byte/Cycle	2nd Byte/Cycle	3rd Byte/Cycle	4th Byte/Cycle	5th Byte/Cycle
W29N04GZ	EFh	ACh	90h	15h	54h
W29N04GW	EFh	BCh	90h	55h	54h
Description	MFR ID	Device ID	Cache Programming not Supported	Page Size:2KB Spare Area Size:64B BLK Size w/o Spare:128KB Organized:x8 or x16 Serial Access:25ns	

x16 device : the ID is outputted at word units, and defined lower-byte (IO0-7). ID table shows only lower-byte ID.

Table 9-1 Device ID and configuration codes for Address 00h

# of Byte/Cycles	1st Byte/Cycle	2nd Byte/Cycle	3rd Byte/Cycle	4th Byte/Cycle
Code	4Fh	4Eh	46h	49h

Table 9-2 ONFI Identifying Codes for Address 20h

9.1.5 READ PARAMETER PAGE (ECh)

READ PARAMETER PAGE can read out the device's parameter data structure, such as, manufacturer information, device organization, timing parameters, key features, and other pertinent device parameters. The data structure is stored with at least three copies in the device's parameter page. Figure 9-9 shows the READ PARAMETER PAGE timing. The RANDOM DATA OUTPUT (05h-E0h) command is supported during data output.

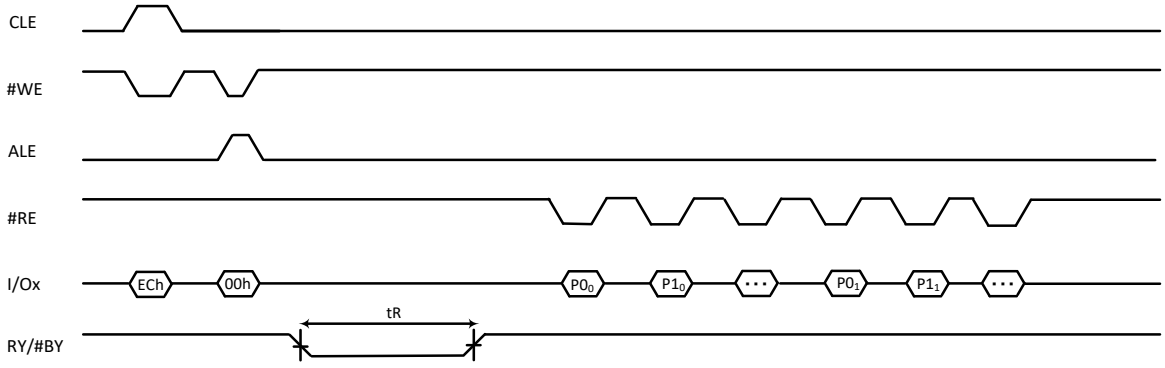

Figure 9-6 Read Parameter Page

Byte	Description		Value
0-3	Parameter page signature		4Fh, 4Eh, 46h, 49h
4-5	Revision number		02h, 00h
6-7	Features supported	W29N04GZ	18h,00h
		W29N04GW	19h,00h
8-9	Optional commands supported		3Ch,00h
10-31	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
32-43	Device manufacturer		57h, 49h, 4Eh, 42h, 4Fh, 4Eh, 44h, 20h, 20h, 20h, 20h, 20h
44-63	Device model	W29N04GZ	57h,32h,39h,4Eh,30h,34h,47h,5Ah,20h,20h,20h,20h,20h,20h,20h,20h,20h,20h,20h,20h
		W29N04GW	57h,32h,39h,4Eh,30h,34h,47h,57h,20h,20h,20h,20h,20h,20h,20h,20h,20h,20h,20h,20h
64	Manufacturer ID		EFh
65-66	Date code		00h, 00h
67-79	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
80-83	# of data bytes per page		00h, 08h, 00h, 00h

Byte	Description	Value
84-85	# of spare bytes per page	40h, 00h
86-89	# of data bytes per partial page	00h, 02h, 00h, 00h
90-91	# of spare bytes per partial page	10h, 00h
92-95	# of pages per block	40h, 00h, 00h, 00h
96-99	# of blocks per unit	00h, 10h, 00h, 00h
100	# of logical units	01h
101	# of address cycles	23h
102	# of bits per cell	01h
103-104	Bad blocks maximum per unit	50h, 00h
105-106	Block endurance	01h, 05h
107	Guaranteed valid blocks at beginning of target	01h
108-109	Block endurance for guaranteed valid blocks	00h, 00h
110	# of programs per page	04h
111	Partial programming attributes	00h
112	# of ECC bits	01h
113	# of interleaved address bits	01h
114	Interleaved operation attributes	00h
115-127	Reserved	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
128	I/O pin capacitance	0Ah
129-130	Timing mode support	1Fh, 00h
131-132	Program cache timing	00h, 00h
133-134	Maximum page program time	BCh, 02h
135-136	Maximum block erase time	10h, 27h
137-138	Maximum random read time	19h, 00h
139-140	tCCS minimum	46h, 00h
141-163	Reserved	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
164-165	Vendor specific revision #	01h,00h
166-253	Vendor specific	00h
254-255	Integrity CRC	Set at shipment
256-511	Value of bytes 0-255	

Byte	Description	Value
512-767	Value of bytes 0-255	
>767	Additional redundant parameter pages	

x16 device : the ID is outputted at word units, and defined lower-byte (IO0-7). ID table shows only lower-byte ID.

Table 9-3 Parameter Page Output Value

9.1.6 READ STATUS (70h)

The W29N04GW/Z has an 8-bit Status Register which can be read during device operation. Refer to Table 9.4 for specific Status Register definitions. After writing 70h command to the Command Register, read cycles will only read from the Status Register. The status can be read from I/O[7:0] outputs, as long as #CE and #RE are LOW. Note; #RE does not need to be toggled for Status Register read. The Command Register remains in status read mode until another command is issued. To change to normal read mode, issue the PAGE READ (00h) command. After the PAGE READ command is issued, data output starts from the initial column address.

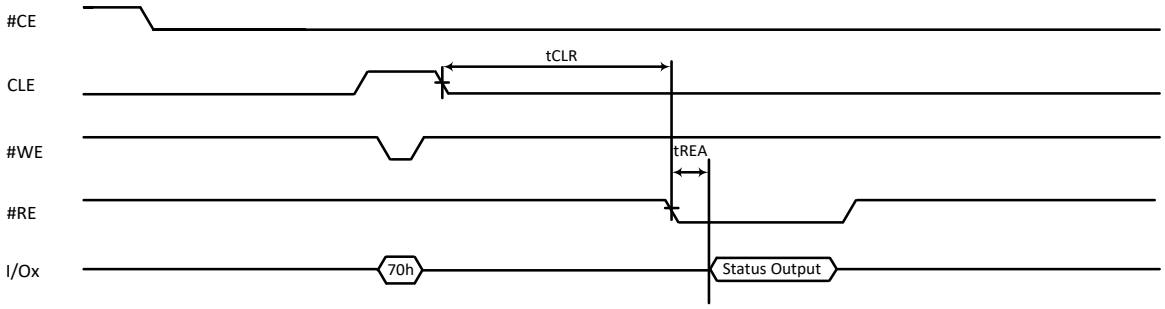

Figure 9-7 Read Status Operation

SR bit	Page Read	Page Program	Block Erase	Definition
I/O 0	Not Use	Pass/Fail	Pass/Fail	0=Successful Program/Erase 1=Error in Program/Erase
I/O 1	Not Use	Not Use	Not Use	0=Successful Program 1=Error in Program
I/O 2	Not Use	Not Use	Not Use	0
I/O 3	Not Use	Not Use	Not Use	0
I/O 4	Not Use	Not Use	Not Use	0
I/O 5	Ready/Busy	Ready/Busy	Ready/Busy	Ready = 1 Busy = 0
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Ready = 1 Busy = 0
I/O 7	Write Protect	Write Protect	Write Protect	Unprotected = 1 Protected = 0

Table 9-4 Status Register Bit Definition

9.1.7 READ STATUS ENHANCED (78h)

The READ STATUS ENHANCED (78h) command returns the status of the addressed plane on a target even when it is busy (SR BIT 6 = 0).

Writing 78h to the command register, followed by three row address cycles containing the page, plane and block addresses that is same as executed addresses, puts the device into read status mode. The device stays in this mode until another valid command is issued

The device status is returned when the host requests data output. The SR BIT 6 and SR bit 5 bits of the status register are shared for all planes on the device. The SR BIT 1 and SR BIT 0 (SR bit0) bits are specific to the plane specified in the row address.

The READ STATUS ENHANCED (78h) command also enables the device for data output. To begin data output following a READ operation after the device is ready (SR BIT 6 = 1), issue the READ MODE (00h) command, then begin data output. If the host needs to change the data register that will output data, use the TWO PLANE RANDOMDATA READ (06h-E0h) command after the device is ready