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W3150A+ Datasheet

Ver. 2.0.5

WIZnet

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Document History Information

Revision	Data	Description
Ver. 1.0.0	OCT 27, 2005	Release with W3150A Launching
Ver. 1.0.1	NOV 21, 2005	Replace, *1.8V* operation → **3.3V** operation (p.3) Change block diagram (p.4) Change figure (p.32) Replace, *g_Sn_TX_BASE* → **g_Sn_RX_BASE** (p.33) Replace, memcpy(, ,*left_size*) → in memcpy(, ,**upper_size**) (p.40, p.41, p.47, p.48, p.49) Replace, get_offset = *Sn_TX_RR* & → get_offset = **Sn_TX_WR** & (p.41, p.49) Replace, *SOCK_UDP* → **SOCK_IPRAW** (p.51)
Ver. 1.0.2	DEC 28, 2005	Add 7.3 Power Dissipation (p.56)
Ver. 2.0.0	AUG 15, 2006	New version release (W3150A -> W3150A+) Add SPI Information Added ND option in socket mode register Remove Memory test mode Add MACRAW mode
Ver. 2.0.1	JAN 8, 2007	LB bit in Mode register is not used . W3150A+ used in Big-endian ordering only.
Ver. 2.0.2	APR 5, 2007	Change Operating temperature value (p.57)
Ver. 2.0.3	May 2, 2007	Modify explanation of RECV_INT in Sn_IR register (P. 27) Replace reset value of Sn_DHAR register (0x00 to 0xFF, P. 30) Modify explanation of Sn_DIPR, Sn_DPORT register(P. 30) Replace reset value of Sn_MSS register (0xFFFF to 0x0000, P. 31) Modify figure of W3150A+ AC Characteristics(P. 58,59,60,62,63)
Ver. 2.0.4	Oct 5, 2007	Modify figure of W3150A+ AC Characteristics (Added item NO.7 SCLK high to /SS high, P. 61)
Ver. 2.0.5	Oct 5, 2015	Not support SPI mode 3

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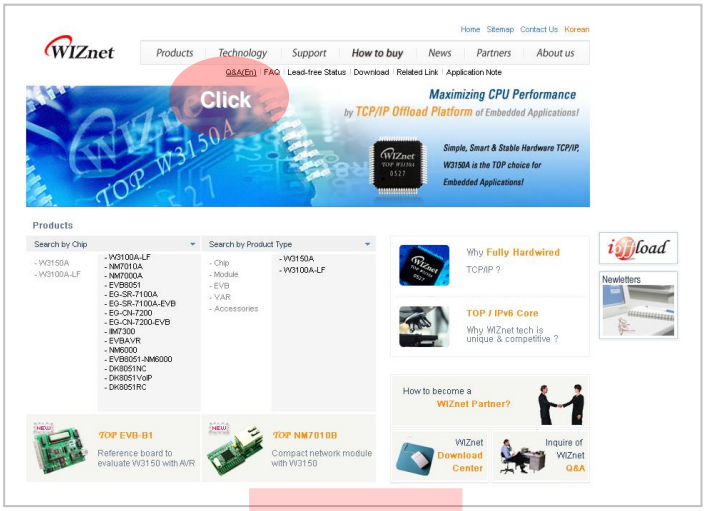
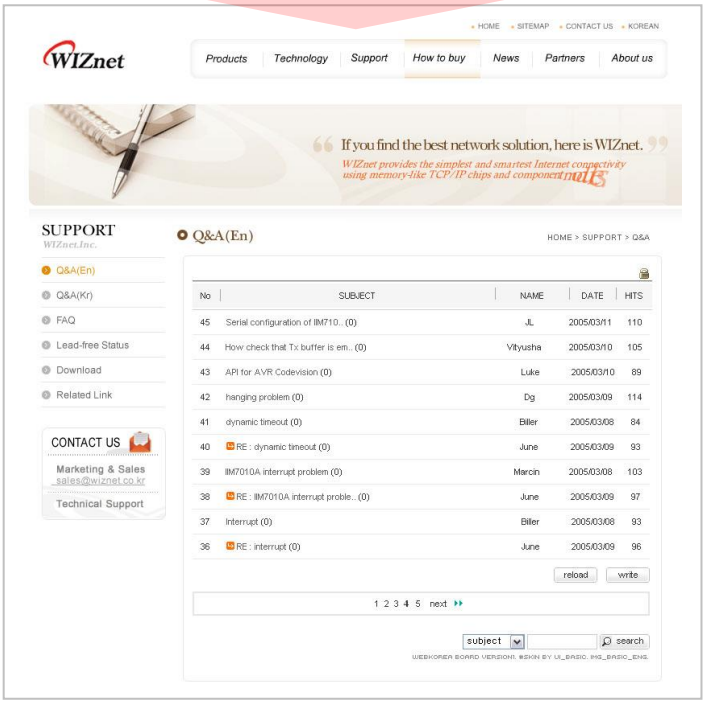




W3150A+ Datasheet

Description

The W3150A+ is an LSI of hardware protocol stack that provides an easy, low-cost solution for high-speed Internet connectivity for digital devices by allowing simple installation of TCP/IP stack in the hardware.

The W3150A+ offers a quick and easy way to add Ethernet networking functionality to any products. Implementing this LSI into a system can completely provide Internet connectivity and process standard protocols by significantly reducing the software development cost as well development time which is most important in today time-to market.

The W3150A+ contains TCP/IP Protocol Stacks such as TCP, UDP, ICMP, IPv4, ARP and PPPoE protocols, as well as Ethernet protocols such as MAC protocol. The total internal memory size is 16Kbytes, which is used as the buffer for data transmission and receipt.

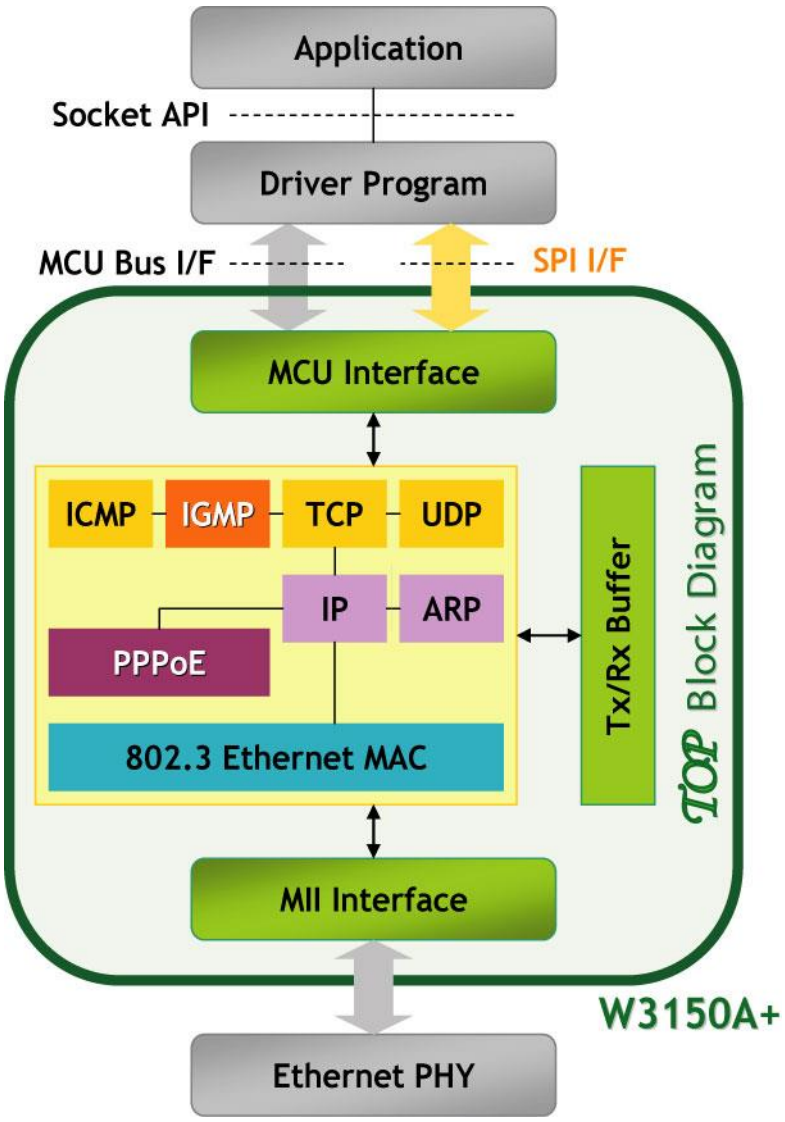
The W3150A+ provides three different interfaces like direct, indirect bus interfaces and SPI(Serial Peripheral Interface) to connect with MCUs and standard MII(Media Independent Interface) composed of nibble data bus to connect with Ethernet PHY devices.

The W3150A+ is a best-fitted device for embedded application including IP-Settop Box, Internet-DVR, Internet phones, VoIP SOC chips, Internet MP3 players, handheld medical devices, various industrial system for monitoring and metering, and any other non-portable electronic devices such as large consumer electronic products.

Features

- Support Hardwired TCP/IP Protocols : TCP, UDP, ICMP, IGMP, IPv4, ARP, PPPoE, Ethernet
- Support ADSL connection (with support PPPoE Protocol with PAP/CHAP Authentication mode)
- Supports 4 independent sockets simultaneously
- Not support IP Fragmentation
- Standard MII Interface for Ethernet-PHY chip
- Supports 10BaseT/100BaseTX
- Supports full-duplex mode
- Internal 16Kbytes Memory for Tx/Rx Buffers
- 0.18 μm CMOS technology
- 3.3V operation with 5V I/O signal tolerance
- Small 64 Pin LQFP Package
- Lead-Free Package
- Support Serial Peripheral Interface(SPI MODE 0)

Block Diagram



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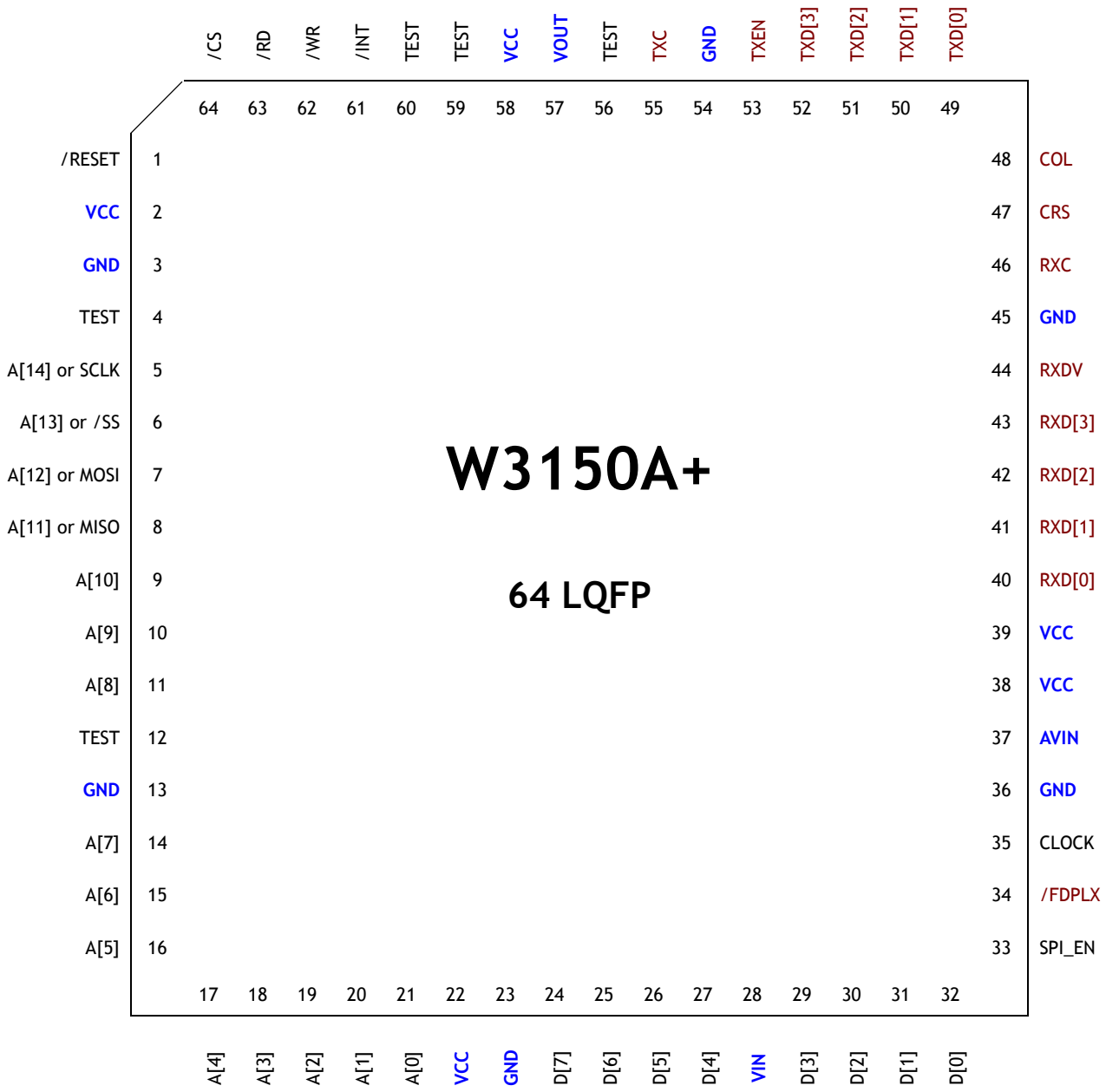
1. Pin Assignment



1.1. MII Signal Description

Pin#	Signal	I/O	Description
55	TXC	I	**Transmit Clock** This input pin needs a continuous clock as timing reference for TXD[3:0] and TXEN. TXC is supplied by the PHY. TXC is 2.5 MHz in 10 BASE-T nibble mode, and 25MHz in 100BASE-TX nibble mode.
53	TXEN	O	**Transmit Enable** This output signal indicates the presence of a valid nibble data on TXD[3:0]. It becomes active when the first nibble data of the packet is valid on TXD[3:0] and goes low after the last nibble data of the packet is clocked out of TXD[3:0]. This signal connects directly to the PHY device. This signal is active high.
52 51 50 49	TXD[3] TXD[2] TXD[1] TXD[0]	O	**Transmit Data** These pins transmit Nibble NRZ data to the PHY synchronously with TXC when TXEN is asserted.
46	RXC	I	**Receive Clock** This input pin needs a continuous clock as timing reference for RXDV and RXD[3:0] signals. RXC is supplied by the PHY. RXC is 2.5MHz in 10BASE-T nibble mode, and 25MHz in 100BASE-TX nibble mode.
48	COL	I	**Collision Detect** The active high signal at this input pin indicates that a collision has been detected in Half-Duplex modes. This signal is asynchronous and is ignored during full-duplex operation.
47	CRS	I	**Carrier Sense** The active high signal at this input pin detects that carrier is present.
44	RXDV	I	**Receive Data Valid** If signal is detected high on this input pin, valid data is present on the RXD[3:0]. If signal is detected low at the end of the valid packet, the signal is valid on the rising of the RXC.
43 42 41 40	RXD[3] RXD[2] RXD[1] RXD[0]	I	**Receive Data** These pins receive Nibble NRZ data from the PHY device synchronously with RXC when RXDV is asserted.

1.2. MCU Interface Signal Description

Pin#	Signal	I/O	Description
1	/RESET	I	**RESET** This pin is active Low input to initialize or re-initialize W3150A+. Asserting this pin low for at least 2us will force a reset process to occur which will result in all internal registers re-initializing to their default states.
35	CLOCK	I	**CLOCK** This pin is the Primary clock required for internal operation of W3150A+. 25MHz is required. In general, PHY driving clock can be shared for saving cost. *Note) Sharing crystal source clock with multiple devices may cause some troubles. In our reference design, we used one crystal for both PHY and W3150A+ with verification.* *But for other kind of PHY, please confirm safety prior to decision.*
5	A[14]/ SCLK	I	**ADDRESS PIN or SCLK (Serial Clock) *** This pin is used to select a register or memory. When asserting SPI_EN pin high, this pin is used to SPI Clock signal Pin.
6	A[13]/ /SS	I	**ADDRESS PIN or /SS (Slave Select) *** This pin is used to select a register or memory. When asserting SPI_EN pin high, this pin is used to SPI Slave Select signal Pin. In only SPI Mode, this pin is active low
7	A[12]/ MOSI	I	**ADDRESS PIN or MOSI (Master Out Slave In) *** This pin is used to select a register or memory. When asserting SPI_EN pin high, this pin is used to SPI MOSI signal pin.
8	A[11]/ MISO	I/O	**ADDRESS PIN or MISO (Master In Slave Out) *** This pin is used to select a register or memory. When asserting SPI_EN pin high, this pin is used to SPI MISO signal pin.
9:11 14:21	A[10:8] A[7:0]	I	**ADDRESS PINS** These pins are used to select a register or memory.
24:27, 29:32	D[7:4] D[3:0]	I/O	**DATA PINS** These pins are used to read and write register or memory data.

* Difference from W3150A

61	/INT	O	**INTERRUPT** This pin Indicates that W3150A+ requires MCU attention after socket connecting, disconnecting, receiving data or timeout. The interrupt is cleared by writing IR(Interrupt Register) or S*n*_IR (Socket *n*th Interrupt Register). All interrupts are maskable. This signal is active low.
64	/CS	I	**CHIP SELECT** Chip Select is for MCU access to internal registers/memory. /WR and /RD select direction of data transfer. This signal is active low.
62	/WR	I	**WRITE ENABLE** Strobe from MCU to write an internal register/memory selected by A[14:0]. Data is latched into the W3150A+ on the rising edge of this input. This signal is active low.
63	/RD	I	**READ ENABLE** Strobe from MCU to read an internal register/memory selected by A[14:0]. This signal is active low.

1.3. Miscellaneous Signal Description

Pin#	Signal	I/O	Description
34	/FDPLX	I	**FULL/HALF DUPLEX SELECT** This pin selects Half/Full Duplex operation mode. This pin must be externally pulled low (typically x kΩ) in order to configure the W3150A+ for Full Duplex operation. Low = Full Duplex High = Half Duplex
33	SPI_EN	I	**SPI Enable*** This pin selects Enable/disable of the SPI Mode. This pin is internally pulled down for previous W3150A users. Even if there is no signal connection to this pin, it asserts low internally. Thereby, in case of change to W3150A+, there is no effort to change previous board design. Low = SPI Mode Disable High = SPI Mode Enable
4,12,56, 59,60	TEST	I	**FACTORY TEST INPUT** Used to check the chip's internal functions. This should be tied low (pull-down) during normal operation.

* * Difference from W3150A

1.4. Power Supply Signal Description

Pin#	Signal	I/O	Description
2, 22, 38, 39, 58	VCC		**POSITIVE 3.3V SUPPLY PINS**
28	VIN		**1.8V power input** 1.8V power supply
37	AVIN		**1.8V Analog power input** 1.8V power supply for analog circuit ; should be well decoupled. Refer Figure 1-1. Reference Schematic for Power input.
57	VOUT		**1.8V power out** Be sure to connect 10uF tantalum capacitor and a 0.1uF capacitor for noise de-coupling. Then connect this pin through a ferrite bead to VIN and AVIN.
3, 13, 23, 36, 45, 54	GND		**NEGATIVE (GROUND) SUPPLY PINS**

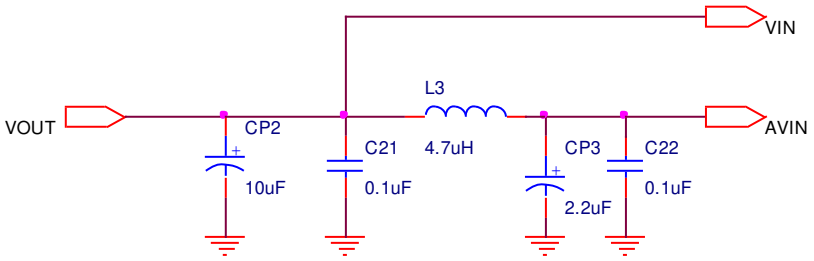
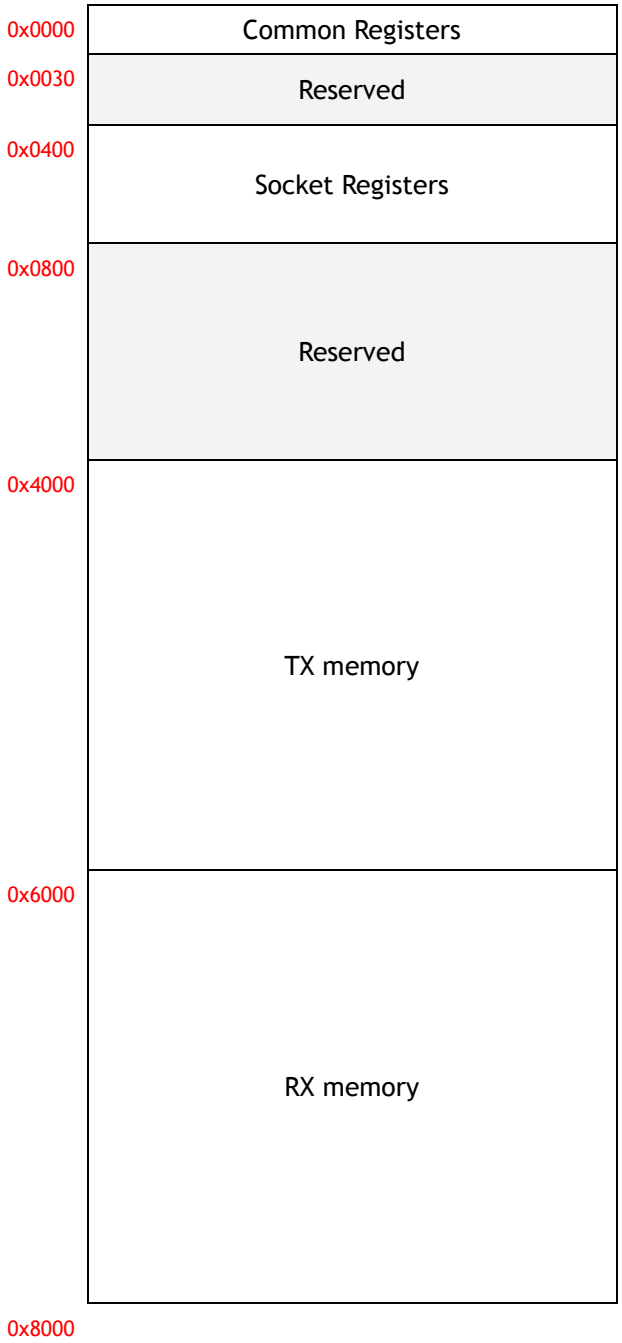


Figure 1-1. Reference Schematic for Power input

2. Memory map

W3150A+ is composed of Common Register, Socket Register, TX Memory, and RX Memory. Each fields are shown as below.



3. W3150A+ Registers

3.1. Common Registers

Address	Register
0x0000	Mode (MR)
0x0001	Gateway Address (GAR0)
0x0002	(GAR1)
0x0003	(GAR2)
0x0004	(GAR3)
0x0005	Subnet mask Address (SUBR0)
0x0006	(SUBR1)
0x0007	(SUBR2)
0x0008	(SUBR3)
0x0009	Source Hardware Address (SHAR0)
0x000A	(SHAR1)
0x000B	(SHAR2)
0x000C	(SHAR3)
0x000D	(SHAR4)
0x000E	(SHAR5)
0x000F	Source IP Address (SIPR0)
0x0010	(SIPR1)
0x0011	(SIPR2)
0x0012	(SIPR3)
0x0013	Reserved
0x0014	
0x0015	Interrupt (IR)
0x0016	Interrupt Mask (IMR)
0x0017	Retry Time (RTR0)
0x0018	(RTR1)
0x0019	Retry Count (RCR)

Address	Register
0x001A	RX Memory Size (RMSR)
0x001B	TX Memory Size (TMSR)
0x001C	Authentication Type in PPPoE (PATR0)
0x001D	(PATR1)
0x001E ~ 0x0027	Reserved
0x0028	PPP LCP Request Timer (PTIMER)
0x0029	PPP LCP Magic number (PMAGIC)
0x002A	Unreachable IP Address (UIPR0)
0x002B	(UIPR1)
0x002C	(UIPR2)
0x002D	(UIPR3)
0x002E	Unreachable Port (UPORT0)
0x002F	(UPORT1)
0x0030 ~ 0x03FF	Reserved

3.2. Socket Registers

Address	Register
0x0400	Socket 0 Mode (S0_MR)
0x0401	Socket 0 Command (S0_CR)
0x0402	Socket 0 Interrupt (S0_IR)
0x0403	Socket 0 Status (S0_SR)
0x0404 0x0405	Socket 0 Source Port (S0_PORT0) (S0_PORT1)
0x0406 0x0407 0x0408 0x0409 0x040A 0x040B	Socket 0 Destination Hardware Address (S0_DHAR0) (S0_DHAR1) (S0_DHAR2) (S0_DHAR3) (S0_DHAR4) (S0_DHAR5)
0x040C 0x040D 0x040E 0x040F	Socket 0 Destination IP Address (S0_DIPR0) (S0_DIPR1) (S0_DIPR2) (S0_DIPR3)
0x0410 0x0411	Socket 0 Destination Port (S0_DPORT0) (S0_DPORT1)
0x0412 0x0413	Socket 0 Maximum Segment Size (S0_MSSR0) (S0_MSSR1)
0x0414	Socket 0 Protocol in IP Raw mode (S0_PROTO)

Address	Register
0x0415	Socket 0 IP TOS (S0_TOS)
0x0416	Socket 0 IP TTL (S0_TTL)
0x0417 ~ 0x041F	Reserved
0x0420 0x0421	Socket 0 TX Free Size (S0_TX_FSR0) (S0_TX_FSR1)
0x0422 0x0423	Socket 0 TX Read Pointer (S0_TX_RD0) (S0_TX_RD1)
0x0424 0x0425	Socket 0 TX Write Pointer (S0_TX_WR0) (S0_TX_WR1)
0x0426 0x0427	Socket 0 RX Received Size (S0_RX_RSR0) (S0_RX_RSR1)
0x0428 0x0429	Socket 0 RX Read Pointer (S0_RX_RD0) (S0_RX_RD1)
0x042A 0x042B	Reserved
0x042C ~ 0x04FF	Reserved

Address	Register
0x0500	Socket 1 Mode (S1_MR)
0x0501	Socket 1 Command (S1_CR)
0x0502	Socket 1 Interrupt (S1_IR)
0x0503	Socket 1 Status (S1_SR)
0x0504	Socket 1 Source Port (S1_PORT0)
0x0505	(S1_PORT1)
0x0506	Socket 1 Destination Hardware Address (S1_DHAR0)
0x0507	(S1_DHAR1)
0x0508	(S1_DHAR2)
0x0509	(S1_DHAR3)
0x050A	(S1_DHAR4)
0x050B	(S1_DHAR5)
0x050C	Socket 1 Destination IP Address (S1_DIPR0)
0x050D	(S1_DIPR1)
0x050E	(S1_DIPR2)
0x050F	(S1_DIPR3)
0x0510	Socket 1 Destination Port (S1_DPORT0)
0x0511	(S1_DPORT1)
0x0512	Socket 1 Maximum Segment Size (S1_MSSR0)
0x0513	(S1_MSSR1)
0x0514	Socket 1 Protocol in IP Raw mode (S1_PROTO)

Address	Register
0x0515	Socket 1 IP TOS (S1_TOS)
0x0516	Socket 1 IP TTL (S1_TTL)
0x0517 ~ 0x051F	Reserved
0x0520	Socket 1 TX Free Size (S1_TX_FSR0)
0x0521	(S1_TX_FSR1)
0x0522	Socket 1 TX Read Pointer (S1_TX_RD0)
0x0523	(S1_TX_RD1)
0x0524	Socket 1 TX Write Pointer (S1_TX_WR0)
0x0525	(S1_TX_WR1)
0x0526	Socket 1 RX Received Size (S1_RX_RSR0)
0x0527	(S1_RX_RSR1)
0x0528	Socket 1 RX Read Pointer (S1_RX_RD0)
0x0529	(S1_RX_RD1)
0x052A 0x052B	Reserved
0x052C ~ 0x05FF	Reserved

Address	Register
0x0600	Socket 2 Mode (S2_MR)
0x0601	Socket 2 Command (S2_CR)
0x0602	Socket 2 Interrupt (S2_IR)
0x0603	Socket 2 Status (S2_SR)
0x0604 0x0605	Socket 2 Source Port (S2_PORT0) (S2_PORT1)
0x0606 0x0607 0x0608 0x0609 0x060A 0x060B	Socket 2 Destination Hardware Address (S2_DHAR0) (S2_DHAR1) (S2_DHAR2) (S2_DHAR3) (S2_DHAR4) (S2_DHAR5)
0x060C 0x060D 0x060E 0x060F	Socket 2 Destination IP Address (S2_DIPR0) (S2_DIPR1) (S2_DIPR2) (S2_DIPR3)
0x0610 0x0611	Socket 2 Destination Port (S2_DPORT0) (S2_DPORT1)
0x0612 0x0613	Socket 2 Maximum Segment Size (S2_MSSR0) (S2_MSSR1)
0x0614	Socket 2 Protocol in IP Raw mode (S2_PROTO)

Address	Register
0x0615	Socket 2 IP TOS (S2_TOS)
0x0616	Socket 2 IP TTL (S2_TTL)
0x0617 ~ 0x061F	Reserved
0x0620 0x0621	Socket 2 TX Free Size (S2_TX_FSR0) (S2_TX_FSR1)
0x0622 0x0623	Socket 2 TX Read Pointer (S2_TX_RD0) (S2_TX_RD1)
0x0624 0x0625	Socket 2 TX Write Pointer (S2_TX_WR0) (S2_TX_WR1)
0x0626 0x0627	Socket 2 RX Received Size (S2_RX_RSR0) (S2_RX_RSR1)
0x0628 0x0629	Socket 2 RX Read Pointer (S2_RX_RD0) (S2_RX_RD1)
0x062A 0x062B	Reserved
0x062C ~ 0x06FF	Reserved

Address	Register
0x0700	Socket 3 Mode (S3_MR)
0x0701	Socket 3 Command (S3_CR)
0x0702	Socket 3 Interrupt (S3_IR)
0x0703	Socket 3 Status (S3_SR)
0x0704 0x0705	Socket 3 Source Port (S3_PORT0) (S3_PORT1)
0x0706 0x0707 0x0708 0x0709 0x070A 0x070B	Socket 3 Destination Hardware Address (S3_DHAR0) (S3_DHAR1) (S3_DHAR2) (S3_DHAR3) (S3_DHAR4) (S3_DHAR5)
0x070C 0x070D 0x070E 0x070F	Socket 3 Destination IP Address (S3_DIPR0) (S3_DIPR1) (S3_DIPR2) (S3_DIPR3)
0x0710 0x0711	Socket 3 Destination Port (S3_DPORT0) (S3_DPORT1)
0x0712 0x0713	Socket 3 Maximum Segment Size (S3_MSSR0) (S3_MSSR1)
0x0714	Socket 3 Protocol in IP Raw mode (S3_PROTO)

Address	Register
0x0715	Socket 3 IP TOS (S3_TOS)
0x0716	Socket 3 IP TTL (S3_TTL)
0x0717 ~ 0x071F	Reserved
0x0720 0x0721	Socket 3 TX Free Size (S3_TX_FSR0) (S3_TX_FSR1)
0x0722 0x0723	Socket 3 TX Read Pointer (S3_TX_RD0) (S3_TX_RD1)
0x0724 0x0725	Socket 3 TX Write Pointer (S3_TX_WR0) (S3_TX_WR1)
0x0726 0x0727	Socket 3 RX Received Size (S3_RX_RSR0) (S3_RX_RSR1)
0x0728 0x0729	Socket 3 RX Read Pointer (S3_RX_RD0) (S3_RX_RD1)
0x072A 0x072B	Reserved
0x072C ~ 0x07FF	Reserved

4. Register Descriptions

4.1. Common Registers

MR (Mode Register) [R/W] [0x0000] [0x00][1]

This register is used for S/W Reset, memory test mode, ping block mode, PPPoE mode and Indirect bus I/F.

7	6	5	4	3	2	1	0
RST			PB	PPPoE		AI	IND

Bit	Symbol	Description
7	RST	**S/W Reset** If this bit is '1', internal register will be initialized. It will be automatically cleared after reset.
6	Reserved	Reserved
5	Reserved	Reserved
4	PB	**Ping Block Mode** 0 : Disable Ping block 1 : Enable Ping block If the bit is set as '1', there is no response to the ping request.
3	PPPoE	**PPPoE Mode** 0 : Disable PPPoE mode 1 : Enable PPPoE mode If you use ADSL without router or etc, you should set the bit as '1', and connect to ADSL Server. For more detail, refer to the application note, "How to connect ADSL".
2	Not used	Not used.
1	AI	**Address Auto-Increment in Indirect Bus I/F** 0 : Disable auto-increment 1 : Enable auto-increment At the Indirect Bus I/F mode, if this bit is set as '1', the address will be automatically increased by 1 whenever Read and Write are performed. For more detail, refer to 6.1.2 Indirect Bus IF Mode.
0	IND	**Indirect Bus I/F mode** 0 : Disable Indirect bus I/F mode

[*] [Read/Write] [Address] [Reset value]

		1 : Enable Indirect bus I/F mode If this bit is set as '1', Indirect BUS I/F mode is set. For more detail, refer to 6. Application Information, 6.1.2. Indirect Bus IF Mode.

GWR (Gateway IP Address Register) [R/W] [0x0001 – 0x0004] [0x00]

This Register sets up the default gateway address.

Ex) in case of "192.168.0.1"

0x0001	0x0002	0x0003	0x0004
192 (0xC0)	168 (0xA8)	0 (0x00)	1 (0x01)

SUBR (Subnet Mask Register) [R/W] [0x0005 – 0x0008] [0x00]

This register sets up the subnet mask address.

Ex) in case of "255.255.255.0"

0x0005	0x0006	0x0007	0x0008
255 (0xFF)	255 (0xFF)	255 (0xFF)	0 (0x00)

SHAR (Source Hardware Address Register) [R/W] [0x0009 – 0x000E] [0x00]

This register sets up the Source Hardware address.

Ex) In case of "00.08.DC.01.02.03"

0x0009	0x000A	0x000B	0x000C	0x000D	0x000E
0x00	0x08	0xDC	0x01	0x02	0x03

SIPR (Source IP Address Register) [R/W] [0x000F – 0x0012] [0x00]

This register sets up the Source IP address.

Ex) in case of "192.168.0.3"

0x000F	0x0010	0x0011	0x0012
192 (0xC0)	168 (0xA8)	0 (0x00)	3 (0x03)

IR (Interrupt Register) [R] [0x0015] [0x00]

This register is accessed by the host processor to know the cause of an interrupt.

Any interrupt can be masked in the Interrupt Mask Register (IMR). The /INT signal retain low as long as any masked signal is set, and will not go high until all masked bits in this Register have been cleared.

7	6	5	4	3	2	1	0
CONFLICT	UNREACH	PPPoE	Reserved	S3_INT	S2_INT	S1_INT	S0_INT

Bit	Symbol	Description
7	CONFLICT	**IP Conflict** It is set as '1', when there is ARP request with same IP address as Source IP address. This bit is cleared to '0' by **writing '1' to this bit.***
6	UNREACH	**Destination unreachable** W3150A+ will receive ICMP(Destination Unreachable) packet if not-existing destination IP address is transmitted during UDP data transmission. (Refer to 5.2.2. UDP). In this case, the IP address and the port number will be saved in Unreachable IP Address (UIPR) and Unreachable Port Register (UPORT), and the bit will be set as '1'. This bit will be cleared to '0' by **writing '1' to this bit.***
5	PPPoE	**PPPoE Close** In the PPPoE Mode, if the PPPoE connection is closed, '1' is set. This bit will be cleared to '0' by **writing '1' to this bit.***
4	Reserved	Reserved
3	S3_INT	**Occurrence of Socket 3 Socket Interrupt** It is set in case that interrupt occurs at the socket 3. For more detailed information of socket interrupt, refer to "Socket 3 Interrupt Register (S3_IR). This bit will be automatically cleared when S3_IR is cleared to 0x00.
2	S2_INT	**Occurrence of Socket 2 Socket Interrupt** It is set in case that interrupt occurs at the socket 2. For more detailed information of socket interrupt, refer to "Socket 2 Interrupt Register(S2_IR). This bit will be automatically cleared when S2_IR is cleared to 0x00.
1	S1_INT	**Occurrence of Socket 1 Socket Interrupt** It is set in case that interrupt occurs at the socket 1. For more detailed information of socket interrupt, refer to "Socket 1 Interrupt Register (S1_IR). This bit will be automatically cleared when S1_IR is cleared to 0x00.

* Difference from W3150A

0	S0_INT	**Occurrence of Socket 0 Socket Interrupt** It is set in case that interrupt occurs at the socket 0. For more detailed information of socket interrupt, refer to "Socket 0 Interrupt Register (S0_IR). This bit will be automatically cleared when S0_IR is cleared to 0x00.

IMR (Interrupt Mask Register) [R/W] [0x0016] [0x00]

The Interrupt Mask Register is used to mask interrupts. Each interrupt mask bit corresponds to a bit in the Interrupt Register (IR). If an interrupt mask bit is set, an interrupt will be issued whenever the corresponding bit in the IR is set. If any bit in the IMR is set as '0', an interrupt will not occur though the bit in the IR is set.

7	6	5	4	3	2	1	0
IM_IR7	IM_IR6	IM_IR5	Reserved	IM_IR3	IM_IR2	IM_IR1	IM_IR0

Bit	Symbol	Description
7	IM_IR7	**IP Conflict Enable**
6	IM_IR6	**Destination unreachable Enable**
5	IM_IR5	**PPPoE Close Enable**
4	Reserved	**It should be set as '0'**
3	IM_IR3	**Occurrence of Socket 3 Socket Interrupt Enable**
2	IM_IR2	**Occurrence of Socket 2 Socket Interrupt Enable**
1	IM_IR1	**Occurrence of Socket 1 Socket Interrupt Enable**
0	IM_IR0	**Occurrence of Socket 0 Socket Interrupt Enable**

RTR (Retry Time-value Register) [R/W] [0x0017 - 0x0018] [0x07D0]

This register sets the period of timeout. Value 1 means 100us. The initial value is 2000(0x07D0). That will be set as 200ms.

Ex) For 400ms configuration, set as 4000(0x0FA0)

0x0017	0x0018
0x0F	0xA0

Re-transmission will occur if there is no response from the remote peer to the commands of CONNECT, DISCON, CLOSE, SEND, SEND_MAC and SEND_KEEP, or the response is delayed.

RCR (Retry Count Register) [R/W] [0x0019] [0x08]

This register sets the number of re-transmission. If retransmission occurs more than the number recorded in RCR, Timeout Interrupt (TIMEOUT bit of Socket *n* Interrupt Register (Sn_IR) is set as '1') will occur.

RMSR(RX Memory Size Register) [R/W] [0x001A] [0x55]

This register assigns total 8K RX Memory to each socket.

7	6	5	4	3	2	1	0
Socket 3		Socket 2		Socket 1		Socket 0	
S1	S0	S1	S0	S1	S0	S1	S0

The memory size according to the configuration of S1, S0, is as below.

S1	S0	Memory size
0	0	1KB
0	1	2KB
1	0	4KB
1	1	8KB

According to the value of S1 and S0, the memory is assigned to the sockets from socket 0 within the range of 8KB. If there is not enough memory to be assigned, the socket should not be used. The initial value is 0x55 and the 2K memory is assigned to each 4 sockets respectively.

Ex) When setting as 0xAA, the 4KB memory should be assigned to each socket.
However, the total memory size is 8KB. The memory is normally assigned to the socket 0 and 1, but not to the socket 2 and 3. Therefore, socket 2 and 3 are not absolutely used.

Socket 3	Socket 2	Socket 1	Socket 0
0KB	0KB	4KB	4KB

TMSR(TX Memory Size Register) [R/W] [0x001B] [0x55]

This register is used in assigning total 8K TX Memory to sockets. Configuration can be done in the same way of RX Memory Size Register (RMSR). The initial value is 0x55 and it is to assign 2K memory to 4 sockets respectively.

PATR (Authentication Type in PPPoE mode) [R] [0x001C-0x001D] [0x0000]

This register notifies authentication method that has been agreed at the connection with PPPoE Server. W3150A+ supports two types of Authentication method - PAP and CHAP.

Value	Authentication Type
0xC023	PAP
0xC223	CHAP

PTIMER (PPP Link Control Protocol Request Timer Register) [R/W] [0x0028] [0x28]

This register indicates the duration for sending LCP Echo Request. Vaule 1 is about 25ms.

Ex) in case that PTIMER is 200,

200 * 25(ms) = 5000(ms) = 5 seconds

PMAGIC (PPP Link Control Protocol Magic number Register) [R/W] [0x0029] [0x00]

This register is used in Magic number option during LCP negotiation. Refer to the application note, “How to connect ADSL”.

UIPR (Unreachable IP Address Register) [R] [0x002A – 0x002D] [0x00]

In case of data transmission by using UDP (refer to 5.2.2. UDP), if transmitting to non-existing IP address, ICMP (Destination Unreachable) packet will be received. In this case, that IP address and port number will be respectively saved in the Unreachable IP Address Register(UIPR) and Unreachable Port Register(UPORT).

Ex) in case of “192.168.0.11”,

0x002A	0x002B	0x002C	0x002D
192 (0xC0)	168 (0xA8)	0 (0x00)	11 (0x0B)

UPORT (Unreachable Port Register) [R] [0x002E – 0x002F] [0x0000]

Refer to Unreachable IP Address Register (UIPR)

Ex) In case of 5000(0x1388),

0x002E	0x002F
0x13	0x88