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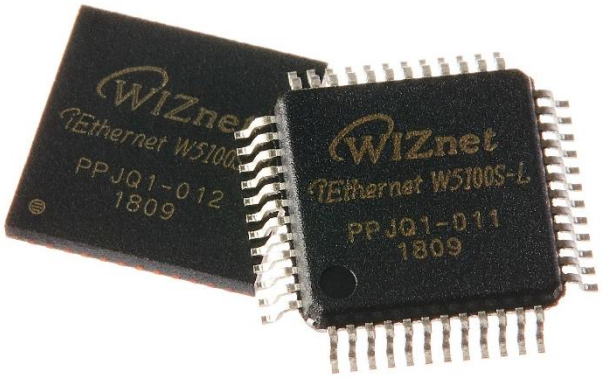
W5100S

(W5100S-L & W5100S-Q)

Version 1.0.0



http://www.wiznet.io/

W5100S

W5100S designed with Hardwired TCP/IP, WIZnet technology, is an embedded Internet Controller Chip. W5100S supporting Full Hardwired, Ethernet MAC (Media Access Control), and 10Base-T/100Base-TX Ethernet PHY is Internet Connectivity One-chip Solution for Internet Protocol (TCP/IP).

With W5100S, Host (User MCU) simply handles variety Internet Protocol such as IPv4, TCP, UDP, ICMP, IGMP, ARP, PPPoE and etc. And W5100S supports each 8KB Memory for Transmit and Receive to minimize using memory on Low-end level Host. Host also independently uses 4 Hardwired SOCKETs to develop vary Internet Applications in each Hardwired SOCKETs.

W5100S supports SPI and Parallel System BUS Interface for Host Interface. It also provides Low Power / Low Heat design, WOL (Wake On LAN), Ethernet PHY Power Down Mode and etc.

W5100S is Low-cost chip that improves on W5100. Any Firmware using on W5100 can be used on W5100S without any modification. Also, W5100S has 48 Pin LQFP & QFN Lead-Free Package, smaller than W5100 for product miniaturization.

Features

- Support Hardwired Internet protocols
  : TCP, UDP, WOL over UDP, ICMP, IGMPv1/v2, IPv4, ARP, PPPoE
- Support 4 independent SOCKETs simultaneously
- Support SOCKET-less command
  : ARP-Request, PING-Request
- Support Ethernet Power down mode & Main Clock gating for power save
- Support Wake on LAN over UDP
- Support Serial & Parallel Host Interface
  : High Speed SPI (MODE 0/3), System Bus with 2 Address signal & 8bit Data
- Internal 16Kbytes Memory for TX/ RX Buffers
- 10BaseT/100BaseTX Ethernet PHY Integrated
- Support Auto Negotiation (Full and half duplex, 10 and 100-based)
- Support Auto-MDIX only when Auto-Negotiation mode
- Not support IP Fragmentation
- 3.3V operation with 5V I/O signal tolerance
- Network Indicator LEDs (Full/Half duplex, Link, 10/100 Speed, Active)
- 48 Pin LQFP & QFN Lead-Free Package (7x7mm, 0.5mm pitch)

Target Applications

W5100S is well-suited for many embedded applications, including:

- User product based on W5100 : No modify firmware
- Home Network Devices: Set-Top Boxes, PVRs, Digital Media Adapters
- Serial-to-Ethernet: Access Controls, LED displays, Wireless AP relays, etc.
- Parallel-to-Ethernet: POS / Mini Printers, Copiers
- USB-to-Ethernet: Storage Devices, Network Printers
- GPIO-to-Ethernet: Home Network Sensors
- Security Systems: DVRs, Network Cameras, Kiosks
- Factory, Building, Home Automations
- Medical Monitoring Equipment
- Embedded Servers
- Internet of Thing (IoT) Devices
- IoT Cloud Devices

Block Diagram

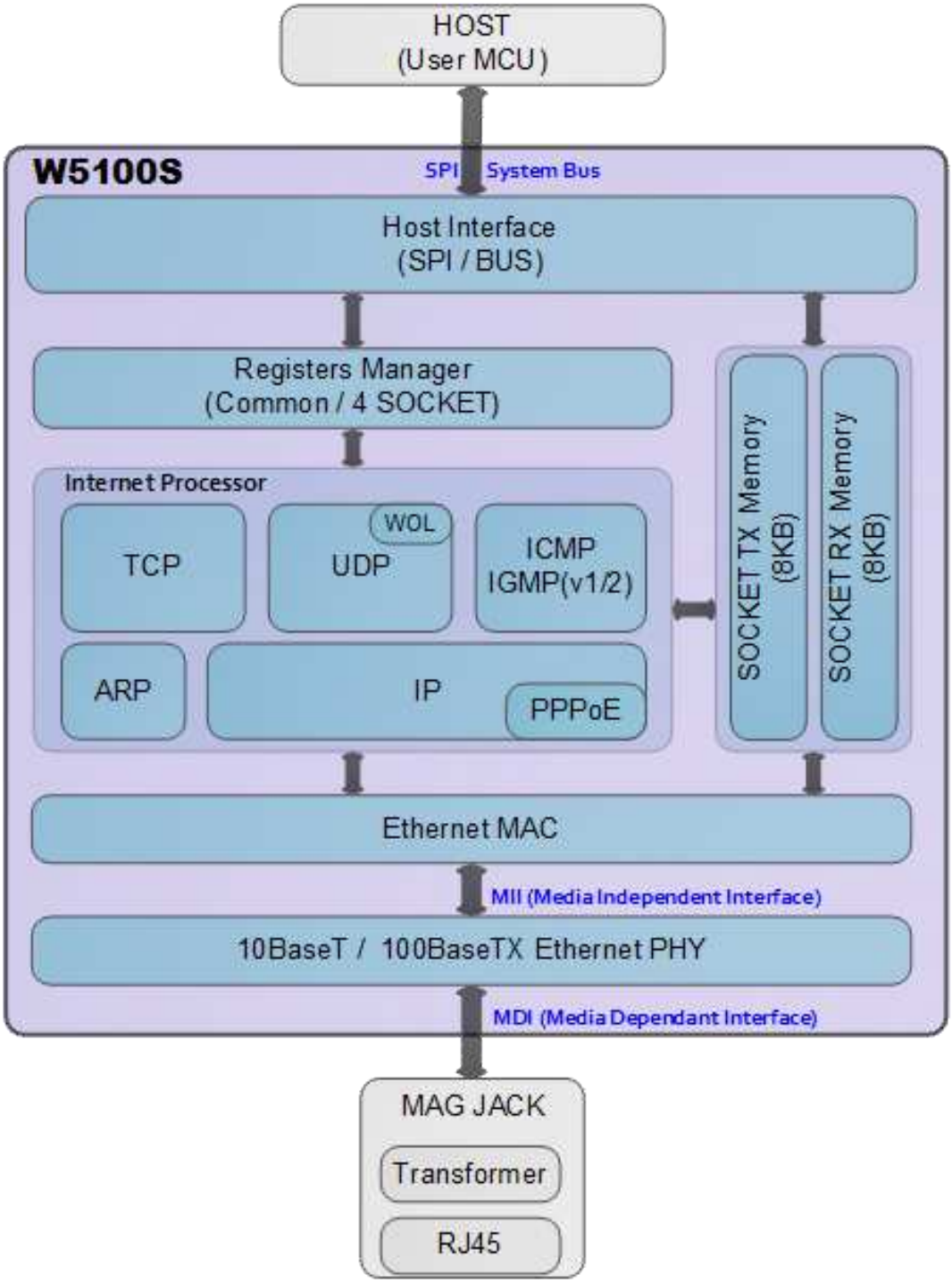


Figure 1 Block Diagram

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1 PIN Description

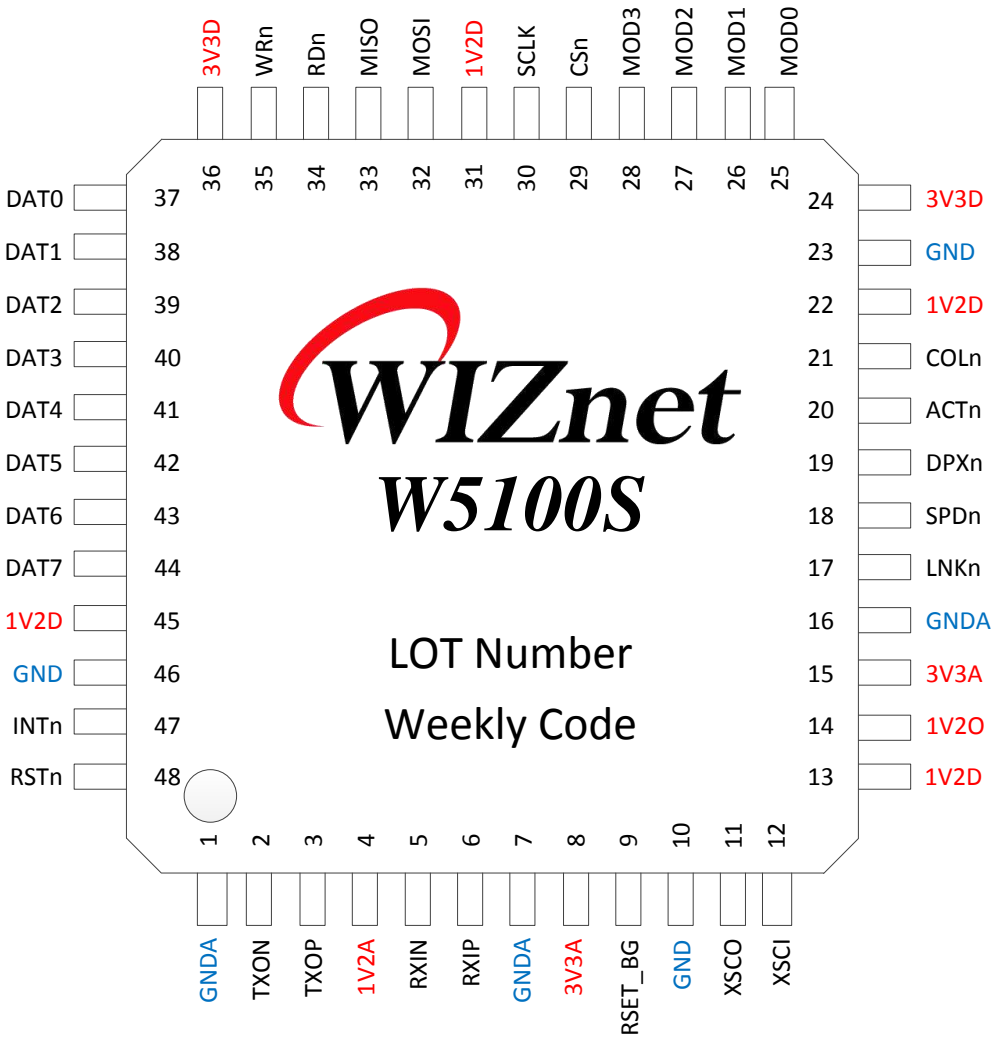

Figure 2 W5100S Pin Layout

Table 1 Pin Type Notation

Type	Description
I	Input
O	Output
M	Alternate (Multi-function) Signal
U	Internal pulled-up 75KΩ resistor
D	Internal pulled-down 75KΩ resistor
A	Analog
P	Power & Ground

1.1 PIN Description

Table 2 PIN Description

PIN #	Symbol	Type	Description
1	GNDA	AP	**Analog Ground**
2	TXON	AO	**Differential Transmitted Signal Pair** Differential Data is transmitted to Media via TXOP/TXON signal pair on MDI Mode.
3	TXOP	AO	
4	1V2A	AP	**Analog 1.2V Power** Supplied from 1V20 voltage source
5	RXIN	AI	**Differential Received Signal Pair** Differential Data is received from Media via RXIP/RXIN signal pair on MDI Mode.
6	RXIP	AI	
7	GNDA	AP	**Analog Ground**
8	3V3A	AP	**Analog 3.3V Power**
9	RSET_BG	AO	**Off-chip Bias Resistor** Must be connected to analog Ground through external 12.3KΩ, error 1% Resistance.
10	GND	AP	**Digital Ground**
11	XSCO	AO	**25MHz Clock** 25MHz Crystal Oscillator (TXAL) or Oscillator (OSC) are used for Internal oscillator stabilization. W5100S uses 25MHz (Low Frequency Mode) or 100MHz (Normal Mode) as Internal Clock from External 25MHz Clock Source. If OSC is used, 25MHz@1.2V must be used and only XSCI must be connected and XSCO must be floated. For more information, refer to *Clock Selection Guide*.
12	XSCI	AI	
13	1V2D	P	**Digital 1.2V Power** Supplied from 1V20 voltage source
14	1V2O	PO	**Internal Regulator 1.2V Power Output** Internal Regulator for W5100S needs Max 150mA for 1.2V Power Output. Make sure to supply 1V2D and 1V2A for External Capacitor 3.3uF stabilization. 1V2O must use Ferrite Bead. 1V2D and 1V2A must be separated and be supplied. This power is only for W5100S. It must not be used for other device.

15	3V3A	AP	**Analog 3.3V Power**
16	GNDA	AP	**Analog Ground**
17	LNKn	OU	**Link Status LED -** It is valid on SPI and Parallel Bus Mode. Low : Link up High : Link down
18	SPDn	OU	**Link Speed LED-** It is valid on SPI and Parallel Bus Mode. Low : 100Mbps High : 10Mbps
19	DPXn	OU	**Link Duplex LED** It is valid on SPI and Parallel Bus Mode. Low : Full-Duplex High : Half-Duplex
20	ACTn	OU	**Link Activity LED** It is valid on SPI and Parallel Bus Mode. No Flash : Link up state without TX/RX Flash : Link up state with TX/RX data High : Link-down state
21	COLn	OU	**Link Collision Detect LED** It is valid on SPI and Parallel Bus Mode. It indicates a collision during Data transmission. Low : Collision Detected High : No Collision
22	1V2D	P	**Digital 1.2V Power** Supplied from 1V20 voltage source.
23	GND	P	**Digital Ground**
24	3V3D	P	**Digital 3.3V power**
25	MOD[0]	ID	**W5100S Interface Mode Selection** Interface Mode is selected by MOD [3:0]. “0000” : SPI Mode “010X” : Parallel Bus Mode
26	MOD[1]	ID	
27	MOD[2]	ID	
28	MOD[3]	ID	
29	CSn	IU	**W5100S Chip Select**

			Low : Select High : No Select
30	SCLK	ID	**SPI Clock** On SPI Mode, it is used to SPI Clock. But on Parallel Bus Mode, it must be connected to GND or be floated.
31	1V2D	P	**Digital 1.2V Power** Supplied from 1V20 voltage source.
32	MOSI /ADDR0	IDM	**SPI Master Output Slave Input / Address 0** MOSI : On SPI Mode, SPI Data is received from HOST. ADDR0 : On Parallel Bus Mode, it is used to Address 0.
33	MISO /ADDR1	IOPM	**SPI Master Input Slave Output / Address 1** MISO : On SPI Mode, SPI Data is transmitted to HOST. ADDR1 : On Parallel Bus Mode, It is used to Address 1.
34	RDn	IU	**Read Strobe** On Parallel Bus Mode, it indicates Read Operation. On SPI Mode, it must be connected to 3V3D or be floated.
35	WRn	IU	**Write Strobe** On Parallel Bus Mode, it indicates Write Operation.
36	3V3D	P	**Digital 3.3V Power**
37	DAT0	IOU	**8 Bits Data Bus** On Parallel Bus Mode, DAT [7:0] receives Data from HOST or W5100S. On SPI Mode, DAT [7:0] must be floated.
38	DAT1	IOU	
39	DAT2	IOU	
40	DAT3	IOU	
41	DAT4	IOU	
42	DAT5	IOU	
43	DAT6	IOU	
44	DAT7	IOU	
45	1V2D	P	**Digital 1.2V Power**
46	GND	P	**Digital Ground**
47	INTn	OP	**Interrupt** When the event occurs during W5100S Ethernet Communication, INTn notices to HOST. Low : Interrupt Occurred High : No Interrupt Refer to IEN (Interrupt pin Enable) in MR2 (Mode Register 2), INTPTMR (Interrupt Pending Time Register), IMR

			(Interrupt Mask Register), IMR2 (Interrupt Mask Register 2), SLIMR (SOCKET-less Interrupt Mask Register)
48	RSTn	IP	**Reset** RSTn initializes W5100S. RSTn must be asserted to Low longer than 500ns. After asserted RSTn, W5100S spends 60.3ms for initialization. (Ref *7.4.1 Reset Timing*) Low : W5100S initialized. High : Normal Operation.

2 Memory Map

W5100S has the same Memory Map as W5100 for compatibility and additional Common Register for improved functionality. The below Figure 3 shows W5100S Memory Map.

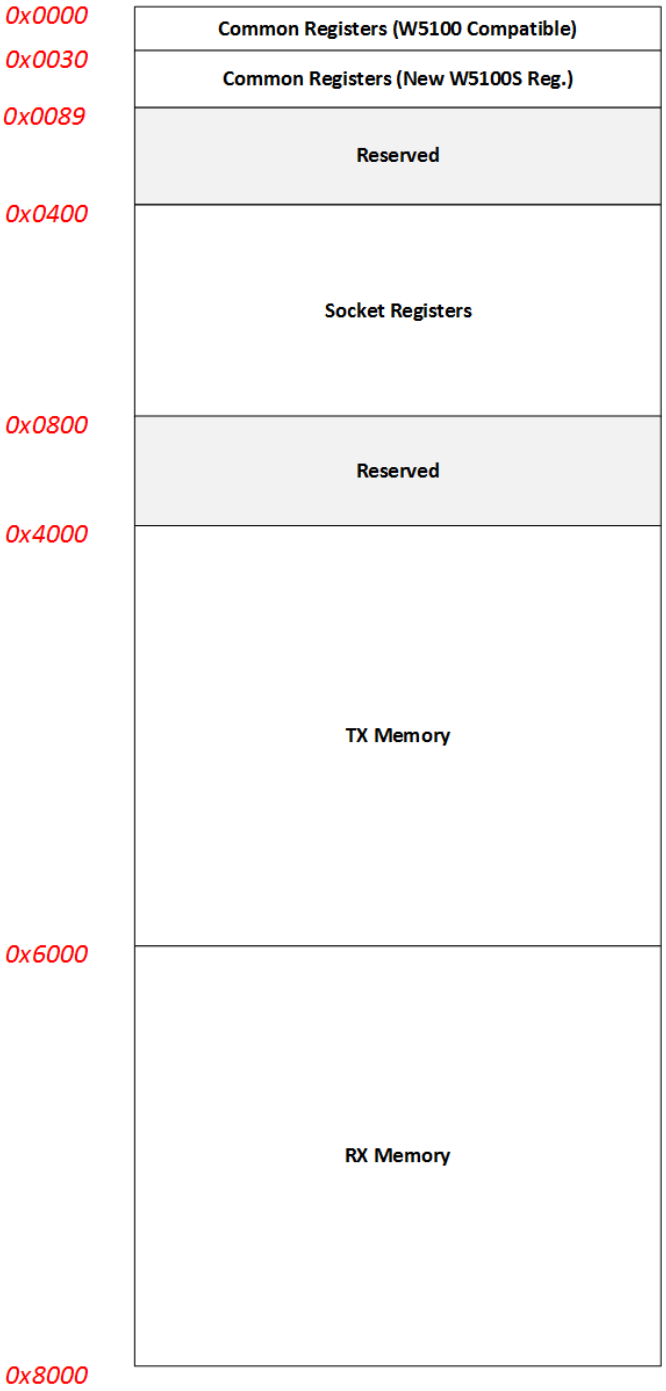

Figure 3 Memory Map

Figure 3 shows the Address Offset of Common & SOCKET Register Block and TX/RX Memory Block. At W5100S Reset, each SOCKET n TX/RX Buffer are assigned with 2KB/2KB from TX/RX Memory Block.

After W5100S Reset, each SOCKET n TX/RX Buffer Size are set by TMSR (TX Memory Size Register) and RMSR (RX Memory Size Register) or by SOCKET n TX/RX Buffer Size Register (Sn_TXBUF_SIZE / Sn_RXBUF_SIZE). The total Buffer Size of SOCKET n TX/RX must not be exceeded by 8 Kbytes.

2.1 W5100S Registers

2.1.1 Common registers

Table 3 Common Registers

Address	Register
0x0000	Mode (MR)
0x0001 0x0002 0x0003 0x0004	Gateway Address (GAR0) (GAR1) (GAR2) (GAR3)
0x0005 0x0006 0x0007 0x0008	Subnet Mask Address (SUBR0) (SUBR1) (SUBR2) (SUBR3)
0x0009 0x000A 0x000B 0x000C 0x000D 0x000E	Source Hardware Address (SHAR0) (SHAR1) (SHAR2) (SHAR3) (SHAR4) (SHAR5)
0x000F 0x0010 0x0011 0x0012	Source IP Address (SIPR0) (SIPR1) (SIPR2) (SIPR3)
0x0013 0x0014	Interrupt Pending Time (INTPTMR0) (INTPTMR1)
0x0015	Interrupt (IR)
0x0016	Interrupt Mask (IMR)
0x0017 0x0018	Retransmission Time (RTR0) (RTR0)
0x0019	Retransmission Time (RCR)
0x001A	RX Memory Size (RMSR)
0x001B	TX Memory Size (TMSR)

Address	Register
0x001C ~ 0x001F	Reserved
0x0020	Interrupt2 (IR2)
0x0021	Interrupt2 Mask (IMR2)
0x0022 ~ 0x0027	Reserved
0x0028	PPP LCP Request Timer (PTIMER)
0x0029	PPP LCP Magic Number (PMAGIC)
0x002A 0x002B 0x002C 0x002D	Unreachable IP Address (UIPR0) (UIPR1) (UIPR2) (UIPR3)
0x002E 0x002F	Unreachable Port (UPORTR0) (UPORTR1)
0x0030	Mode2 (MR2)
0x0031	Reserved
0x0032 0x0033 0x0034 0x0035 0x0036 0x0037	Destination Hardware Address on PPPoE (PHAR0) (PHAR1) (PHAR2) (PHAR3) (PHAR4) (PHAR5)
0x0038 0x0039	Session ID on PPPoE (PSIDR0) (PSIDR1)
0x003A 0x003B	Maximum Receive Unit on PPPoE (PMRUR0) (PMRUR1)
0x003C	PHY Status (PHYSR0)

Address	Register
0x003E	PHY Address Value (PHYAR)
0x003F	PHY Register Address (PHYRAR)
0x0040 0x0041	PHY Data Input (PHYDIR0) (PHYDIR1)
0x0042 0x0043	PHY Data Output (PHYDOR0) (PHYDOR1)
0x0044	PHY Access (PHYACR)
0x0045	PHY Division (PHYDIVR)
0x0046 0x0047	PHY Control (PHYCR0) (PHYCR1)
0x0048 ~ 0x004B	Reserved
0x004C	SOCKET-less Command (SLCR)
0x004D 0x004E	SOCKET-less Retransmission Time (SLRTR0) (SLRTR1)
0x004F	SOCKET-less Retransmission Count (SLRCR)
0x0050 0x0051 0x0052 0x0053	SOCKET-less Peer IP Address (SLPIPR0) (SLPIPR1) (SLPIPR2) (SLPIPR3)
0x0054 0x0055 0x0056 0x0057 0x0058 0x0059	SOCKET-less Peer Hardware Address (SLPHAR0) (SLPHAR1) (SLPHAR2) (SLPHAR3) (SLPHAR4) (SLPHAR5)
0x005A 0x005B	PING Sequence Number (PINGSEQR0) (PINGSEQR1)
0x005C 0x005D	PING ID (PINGIDR0) (PINGIDR1)

Address	Register
0x005E	SOCKET-less Interrupt Mask (SLIMR)
0x005F	SOCKET-less Interrupt (SLIR)
0x0060 ~ 0x006A	Reserved
0x0070	Clock Lock (CLKLCKR)
0x0071	Network Lock (NETLCKR)
0x0072	PHY Lock (PHYLCKR)
0x0073 ~ 0x007F	Reserved
0x0080	Chip Version (VERR)
0x0081	Reserved
0x0082 0x0083	100us Tick Counter (TCNTR0) (TCNTR1)
0x0084 ~ 0x0087	Reserved
0x0088	TCNTCLR

2.1.2 SOCKET Registers

Table 4 Socket Registers

Symbol	Description	Address				
		Sn_	S0_	S1_	S2_	S3_
Sn_MR	SOCKET n Mode	0x0400+(0x0100 x n)	0x0400	0x0500	0x0600	0x0700
Sn_CR	SOCKET n Command	0x0401+(0x0100 x n)	0x0401	0x0501	0x0601	0x0701
Sn_IR	SOCKET n Interrupt	0x0402+(0x0100 x n)	0x0402	0x0502	0x0602	0x0702
Sn_SR	SOCKET n Status	0x0403+(0x0100 x n)	0x0403	0x0503	0x0603	0x0703
Sn_PORTR0	SOCKET n Source Port	0x0404+(0x0100 x n)	0x0404	0x0504	0x0604	0x0704
Sn_PORTR1		0x0405+(0x0100 x n)	0x0405	0x0505	0x0605	0x0705
Sn_DHAR0	SOCKET n Destination Hardware Address	0x0406+(0x0100 x n)	0x0406	0x0506	0x0606	0x0706
Sn_DHAR1		0x0407+(0x0100 x n)	0x0407	0x0507	0x0607	0x0707
Sn_DHAR2		0x0408+(0x0100 x n)	0x0408	0x0508	0x0608	0x0708
Sn_DHAR3		0x0409+(0x0100 x n)	0x0409	0x0509	0x0609	0x0709
Sn_DHAR4		0x040A+(0x0100 x n)	0x040A	0x050A	0x060A	0x070A
Sn_DHAR5		0x040B+(0x0100 x n)	0x040B	0x050B	0x060B	0x070B
Sn_DIPR0	SOCKET n Destination IP Address	0x040C+(0x0100 x n)	0x040C	0x050C	0x060C	0x070C
Sn_DIPR1		0x040D+(0x0100 x n)	0x040D	0x050D	0x060D	0x070D
Sn_DIPR2		0x040E+(0x0100 x n)	0x040E	0x050E	0x060E	0x070E
Sn_DIPR3		0x040F+(0x0100 x n)	0x040F	0x050F	0x060F	0x070F
Sn_DPORTR0	SOCKET n Destination Port	0x0410+(0x0100 x n)	0x0410	0x0510	0x0610	0x0710
Sn_DPORTR0		0x0411+(0x0100 x n)	0x0411	0x0511	0x0611	0x0711
Sn_MSS0	SOCKET n Maximum Segment Size	0x0412+(0x0100 x n)	0x0412	0x0512	0x0612	0x0712
Sn_MSS1		0x0413+(0x0100 x n)	0x0413	0x0513	0x0613	0x0713
Sn_PROTOR	SOCKET n IP Protocol	0x0414+(0x0100 x n)	0x0414	0x0514	0x0614	0x0714
Sn_TOS	SOCKET n IP Type Of Service	0x0415+(0x0100 x n)	0x0415	0x0515	0x0615	0x0715
Sn_TTL	SOCKET n IP Time To Live	0x0416+(0x0100 x n)	0x0416	0x0516	0x0616	0x0716
Reserved	Reserved	0x0417+(0x0100 x n)	0x0417	0x0517	0x0617	0x0717
Reserved	Reserved	0x041D+(0x0100 x n)	0x041D	0x051D	0x061D	0x071D
Sn_RXBUF_SIZE	SOCKET n RX Buffer Size	0x041E+(0x0100 x n)	0x041E	0x051E	0x061E	0x071E
Sn_TXBUF_SIZE	SOCKET n TX Buffer Size	0x041F+(0x0100 x n)	0x041F	0x051F	0x061F	0x071F
Sn_TX_FSR0	SOCKET n	0x0420+(0x0100 x n)	0x0420	0x0520	0x0620	0x0720

Sn_TX_FSR1	TX Free Size	0x0421+(0x0100 x n)	0x0421	0x0521	0x0621	0x0721
Sn_TX_RD0	SOCKET n TX Read Pointer	0x0422+(0x0100 x n)	0x0422	0x0522	0x0622	0x0722
Sn_TX_RD1		0x0423+(0x0100 x n)	0x0423	0x0523	0x0623	0x0723
Sn_TX_WR0	SOCKET n TX Write Pointer	0x0424+(0x0100 x n)	0x0424	0x0524	0x0624	0x0724
Sn_TX_WR1		0x0425+(0x0100 x n)	0x0425	0x0525	0x0625	0x0725
Sn_RX_RSR0	SOCKET n RX Received Size	0x0426+(0x0100 x n)	0x0426	0x0526	0x0626	0x0726
Sn_RX_RSR1		0x0427+(0x0100 x n)	0x0427	0x0527	0x0627	0x0727
Sn_RX_RD0	SOCKET n RX Read Pointer	0x0428+(0x0100 x n)	0x0428	0x0528	0x0628	0x0728
Sn_RX_RD1		0x0429+(0x0100 x n)	0x0429	0x0529	0x0629	0x0729
Sn_RX_WR0	SOCKET n RX Write Pointer	0x042A+(0x0100 x n)	0x042A	0x052A	0x062A	0x072A
Sn_RX_WR1		0x042B+(0x0100 x n)	0x042B	0x052B	0x062B	0x072B
Sn_IMR	SOCKET n Interrupt Mask	0x042C+(0x0100 x n)	0x042C	0x052C	0x062C	0x072C
Sn_FRAGR0	SOCKET n Fragment Offset in IP Header	0x042D+(0x0100 x n)	0x042D	0x052D	0x062D	0x072D
Sn_FRAGR1		0x042E+(0x0100 x n)	0x042E	0x052E	0x062E	0x072E
Sn_MR2	SOCKET n Mode 2	0x042F+(0x0100 x n)	0x042F	0x052F	0x062F	0x072F
Sn_KPALVTR	SOCKET n Keep-alive Timer	0x0430+(0x0100 x n)	0x0430	0x0530	0x0630	0x0730
Sn_RTR0	SOCKET n Retransmission Time	0x0432+(0x0100 x n)	0x0432	0x0532	0x0632	0x0732
Sn_RTR1		0x0433+(0x0100 x n)	0x0433	0x0533	0x0633	0x0733
Sn_RCR	SOCKET n Retransmission Count	0x0434+(0x0100 x n)	0x0434	0x0534	0x0634	0x0734

3 Register Descriptions

Register Notation

* Register Symbol (Register full Name)

- [Register Type][Address Offset][Reset Value]

Register Description….

7	6	5	4	3	2	1	0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Bit Type	Bit Type	Bit Type	Bit Type	Bit Type	Bit Type	Bit Type	Bit Type

Sn_IR [3: 0] indicates a Register Symbol [Upper Bit: Lower Bit].

Sn_IR [3: 0] = '0001' indicates Sn_IR [3] = '0', Sn_IR [2] = '0', Sn_IR [1] = '0', Sn_IR [0] = '1'.

[Register/Bit Type]: Type of Register and Bit.

- [RW] : Both reading and writing are possible.
- [R=W] : The value read and written are the same.
- [RO] : Read Only
- [WO] : Write Only
- [W] : Write Only
- [WC] : Cleared by written ‘1’.
- [W0] : Must be written only ‘0’.
- [W1] : Must be written only ‘1’.
- [AC] : Auto Clear
- [1] : Always read ‘1’
- [0] : Always read ‘0’
- [-] : Not available

[Address Offset]: Register Address Offset

[Reset Value]: Default Value.

Ex1)

3.1.1 MR (Mode Register)

[RW][0x0000][0x03]

MR is abbreviation for Mode Register. This Register is possible to be read and written.

The Register Address Offset is ‘0x0000’ and it is set to ‘0x03’ after Reset.

7	6	5	4	3	2	1	0
RST	-	-	PB	PPPoE	-	AI	IND
AC	W0	W0	R=W	R=W	-	1	1

Ex2) MR [RST]

MR [RST] means RST Bit in MR.

Ex3) MR [7:0]

MR [7:0] means the Bits from 7th to 0th bit in MR.

3.1 Common Registers

3.1.1 MR (Mode Register)

[RW][0x0000] [0x03]

MR is used for Reset, PING Block and PPPoE Enable

7	6	5	4	3	2	1	0
RST	-	-	PB	PPPoE	-	-	-

Bit	Symbol	Description
7	RST	**Reset** If this Bit is '1', All W5100S Registers will be initialized. It will be automatically cleared as '0' after 3 SYS_CLK
[6:5]	-	Reserved
4	PB	**PING Response Block** If this Bit is '1', it blocks the Response to a ping request. 1 : Disable PING Response 0 : Enable PING Response
3	PPPoE	**PPPoE Enable** 1 : Enable PPPoE 0 : Disable PPPoE
[2:0]	-	Reserved

3.1.2 GWR (Gateway IP Address Register)

[R=W] [0x0001-0x0004] [0x00]

GWR configures the Gateway Address when NETLCKR (Network Lock Register) is on Unlock Mode.

Ex) GWR = "192.168.0.1"

GWR0(0x0001)	GWR1(0x0002)	GWR2(0x0003)	GWR3(0x0004)
192 (0xC0)	168 (0xA8)	0 (0x00)	1 (0x01)

3.1.3 SUBR (Subnet Mask Register)

[R=W] [0x0005-0x0008] [0x00]

SUBR configures the Subnet Mask Address when NETLCKR (Network Lock Register) is on Unlock Mode.

Ex) SUBR = "255.255.255.255"

SUBR0(0x0005)	SUBR0(0x0006)	SUBR0(0x0007)	SUBR0(0x0008)
255 (0xFF)	255 (0xFF)	255 (0xFF)	255 (0xFF)

3.1.4 SHAR (Source Hardware Address Register)

[R=W] [0x0009-0x000E] [0x00]

SHAR configures the Source MAC Address when NETLCKR (Network Lock Register) is on Unlock Mode.

Ex) SHAR = "11:22:33:AA:BB:CC"

SHAR0(0x0009)	SHAR1(0x000A)	SHAR2(0x000B)
0x11	0x22	0x33
SHAR3(0x000C)	SHAR4(0x000D)	SHAR5(0x000E)
0xAA	0xBB	0xCC

3.1.5 SIPR (Source IP Address Register)

[R=W] [0x000F-0x0012] [0x00]

SIPR configures the Source IP Address when NETLCKR (Network Lock Register) is on Unlock Mode.

Ex) SIPR = "192.168.0.100"

SIPR0(x000F)	SIPR1(0x0010)	SIPR2(0x0011)	SIPR3(0x0012)
192 (0xC0)	168 (0xA8)	0 (0x00)	100(0x64)

3.1.6 INTPTMR (Interrupt Pending Time Register)

[RW][0x0013-0x0014][0x0000]

INTPTMR sets internal Interrupt Pending Timer Count. When INTn is de-asserted to High, Timer Count is initialized to INTPTMR and decreased by 1 from initial value to '0' every SYS_CLK x 4. When Interrupt occurs and the corresponding Interrupt Mask is set and INTPTMR is '0', INTn is asserted to Low.

Ex) INTPTMR = 1000(0x03EB)

INTPTMR0(0x0013)	INTPTMR1(0x0014)
0x03	0xEB

3.1.7 IR (Interrupt Register)

[RW] [0x0015] [0x00]

When W5100S or SOCKET n Event occurs, the corresponding Bit in IR is set to '1'. If the Event occurs and the corresponded Interrupt Mask Bit in IMR is set to '1' and internal Interrupt