Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

iEthernet W5200
Datasheet

Version 1.3.0

http://www.wiznet.co.kr

W5200

The W5200 chip is a Hardwired TCP/IP embedded Ethernet controller that enables easier internet connection for embedded systems using SPI (Serial Peripheral Interface). W5200 suits best for users who need Internet connectivity for application that uses a single chip to implement TCP/IP Stack, 10/100 Ethernet MAC and PHY.

The W5200 is composed of a fully hardwired market-proven TCP/IP stack and an integrated Ethernet MAC & PHY. Hardwired TCP/IP stack supports TCP, UDP, IPv4, ICMP, ARP, IGMP, and PPPoE, which has been proven in various applications for many years. W5200 uses a 32Kbytes internal buffer as its data communication memory. By using W5200, users can implement the Ethernet application they need by using a simple socket program instead of handling a complex Ethernet Controller.

SPI (Serial Peripheral Interface) is provided for easy integration with the external MCU. Using the only 4 pins of SPI to connect with MCU, it is possible to design for small form factor system with the MCU's I/O pin limit.

In order to reduce power consumption of the system, W5200 provides WOL (Wake on LAN) and power down mode. To wake up during WOL, W5200 should be received magic packet, which is the Raw Ethernet packet.

Features

- Support Hardwired TCP/IP Protocols : TCP, UDP, ICMP, IPv4 ARP, IGMP, PPPoE, Ethernet
- Supports 8 independent sockets simultaneously
- Very small 48 Pin QFN Package
- Support Power down mode
- Support Wake on LAN
- Support High Speed Serial Peripheral Interface(SPI MODE 0, 3)
- Internal 32Kbytes Memory for Tx/Rx Buffers
- 10BaseT/100BaseTX Ethernet PHY embedded
- Support Auto Negotiation (Full and half duplex, 10 and 100-based)
- Support Auto MDI/MDIX
- Support ADSL connection (with support PPPoE Protocol with PAP/CHAP Authentication mode)
- Not support IP Fragmentation
- 3.3V operation with 5V I/O signal tolerance
- Lead-Free Package
- Multi-function LED outputs (Full/Half duplex, Link, Speed)

Target Applications

The W5200 is well suited for many embedded applications, including:

- Home Network Devices: Set-Top Boxes, PVRs, Digital Media Adapters
- Serial-to-Ethernet: Access Controls, LED displays, Wireless AP relays, etc.
- Parallel-to-Ethernet: POS / Mini Printers, Copiers
- USB-to-Ethernet: Storage Devices, Network Printers
- GPIO-to-Ethernet: Home Network Sensors
- Security Systems: DVRs, Network Cameras, Kiosks
- Factory and Building Automations
- Medical Monitoring Equipments
- Embedded Servers

Block Diagram

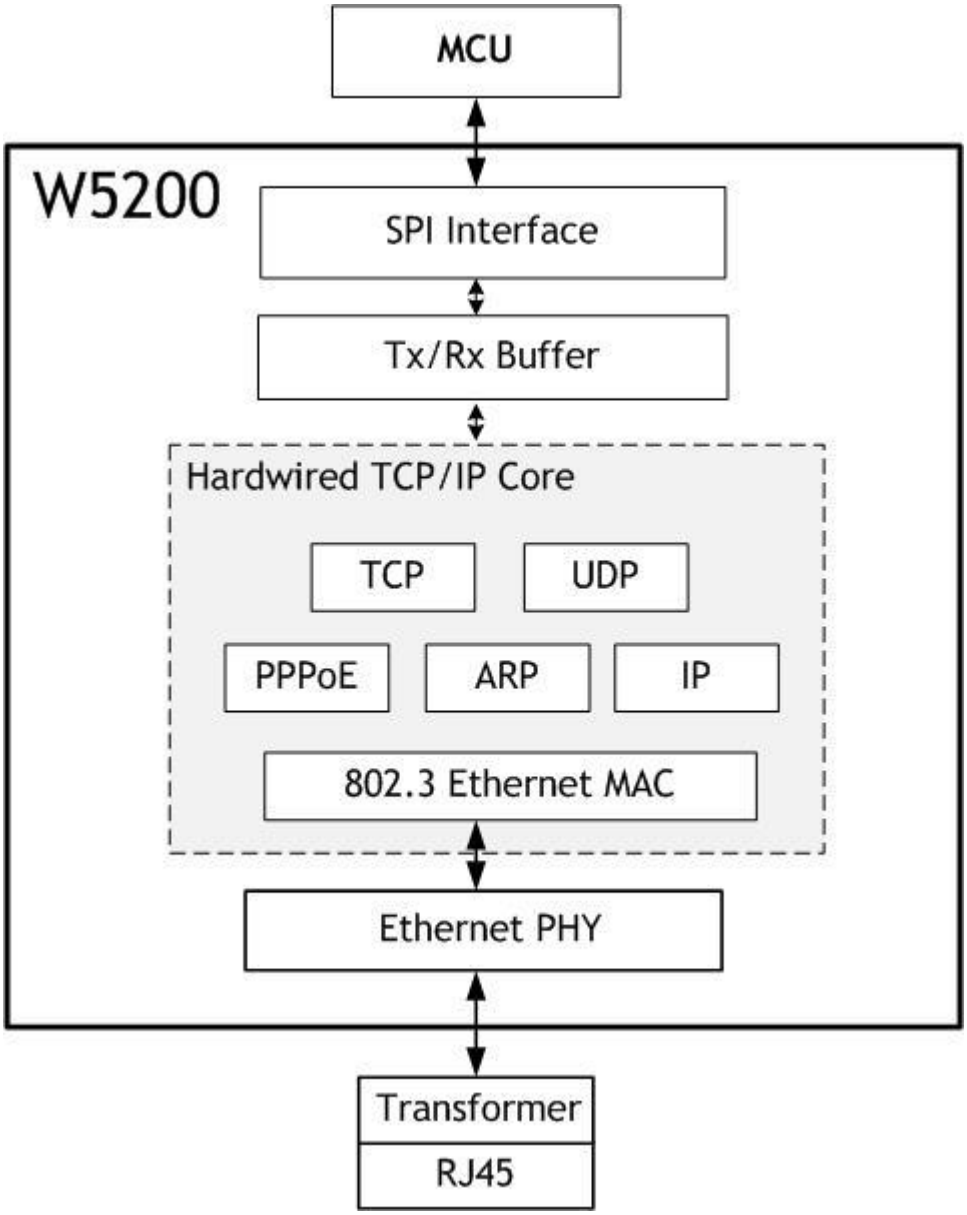


Table of Contents

Table of Figure

1 Pin Assignment

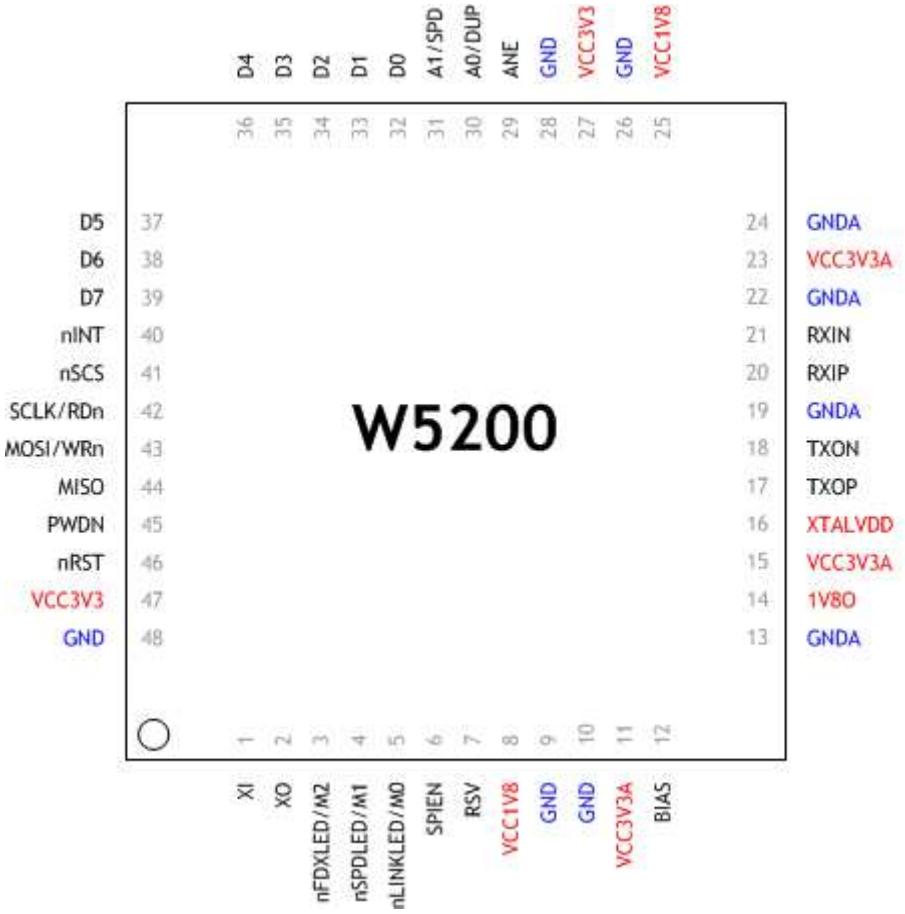


Figure 1 Pin Description W5200

1.1 MCU Interface Signals

Symbol	Type	Pin No	Description
A0/DUP	I	30	**(*)ADDRESS[0]** This pin is used to select a register or memory when using indirect interface.
A1/SPD	I	31	**(*)ADDRESS[1]** This pin is used to select a register or memory when using indirect interface.
D7-0	I/O	32, 33, 34, 35, 36, 37, 38, 39	**(*)DATA** These pins are used to read and write register or memory data.
RSTn	I	46	**RESET (Active LOW)** This pin is active Low input to initialize or re-initialize W5200. RESET should be held at least 2us after low assert, and

			wait for at least 150ms after high de-assert in order for PLL logic to be stable. Refer to RESET timing of "7 Electrical Specification"
CSn	I	41	**SPI SLAVE SELECT (Active LOW)** This pin is used to SPI Slave Select signal Pin when using SPI interface. **(*)CHIP SELECT (Active LOW)** Chip Select is for MCU to access to internal registers or memory when using indirect interface.
INTn	O	40	**INTERRUPT (Active LOW)** This pin indicates that W5200 requires MCU attention after socket connecting, disconnecting, data receiving timeout, and WOL (Wake on LAN). The interrupt is cleared by writing IR(Interrupt Register) or Sn_IR (Socket n Interrupt Register). All interrupts are maskable. This pin is active low.
SCLK/RDn	I	42	**SPI CLOCK** This pin is used to SPI Clock signal Pin when using SPI interface. **(*)READ ENABLE (Active LOW)** Strobe from MCU to read an internal register/memory selected by A[1:0] when using indirect interface.
MOSI/WRn	I	43	**SPI MASTER OUT SLAVE IN** This pin is used to SPI MOSI signal pin when using SPI interface. **(*)WRITE ENABLE (Active LOW)** Strobe from MCU to write an internal register/memory selected by A[1:0] when using indirect interface. Data is latched into the W5200 on the rising edge of this input.
MISO	O	44	**SPI MASTER IN SLAVE OUT** This pin is used to SPI MISO signal pin.
PWDN	I	45	**POWER DOWN (Active HIGH)** This pin is used to power down pin. Low : Normal Mode Enable High : Power Down Mode Enable
SPIEN	I	6	**(*)SPI ENABLE (Active HIGH)** This pin selects Enable/disable of the SPI Mode. Low = SPI Mode Disable High = SPI Mode Enable

			If you don't use SPI mode, in other words, if you want to use indirect mode, then you tied this signal to '0'. This function activate only when reset period.

(*) These pins are related with indirect interface mode. If you need details, Please refer to the W5200_AN_Indirect.pdf file.

1.2 PHY Signals

Symbol	Type	Pin No	Description
RXIP	I	20	**RXIP/RXIN Signal Pair** The differential data from the media is received on the RXIP/RXIN signal pair.
RXIN	I	21	
TXOP	O	17	**TXOP/TXON Signal Pair** The differential data is transmitted to the media on the TXOP/TXIN signal pair.
TXON	O	18	
BIAS	O	12	**BIAS Register** Connect a resistor of 28.7kΩ±1% to the ground. Refer to the "Reference schematic".
ANE	I	29	**Auto Negotiation Mode Enable** This pin selects Enable/Disable of Auto Negotiation Mode. Low :Auto Negotiation Mode Disable High : Auto Negotiation Mode Enable
A0/DUP	I	30	**Full Duplex Mode Enable** This pin selects Enable/Disable of Full Duplex Mode. Low = Half Duplex Mode Enable High = Full Duplex Mode Enable This function activates only during reset period.
A1/SPD	I	31	**Speed Mode** This pin selects 100M/10M Speed Mode. Low = 10M Speed Mode High = 100M Speed Mode This function activates only during reset period.

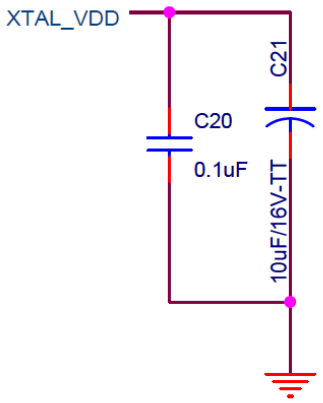
1.3 Miscellaneous Signals

Symbol	Type	Pin No	Description
FDXLEDn/M2	I	3,	**W5200 MODE SELECT**
SPDLEDn/M1		4,	Normal mode : 111
LINKLEDn/M0		5	Other test modes are internal test mode.

			This function activates only during reset period
RSV	I	7	Reserved Pin

- Notes: Pull-Up/Down resistor = Typical value are 10KΩ.

1.4 Power Supply Signals

Symbol	Type	Pin No	Description
VCC3V3A	Power	11, 15, 23	**3.3V power supply for Analog part**
VCC3V3	Power	27, 47	**3.3V power supply for Digital part**
VCC1V8	Power	8, 25	**1.8V power supply for Digital part**
GNDA	Ground	13, 19, 22, 24	**Analog ground**
GND	Ground	9, 10, 26, 28, 48	**Digital ground**
1V8O	O	14	**1.8V regulator output voltage** 1.8V/200mA power created by internal power regulator, is used for core operation power (VCC1V8). Be sure to connect tantalum capacitor between 1V8O and GND for output frequency compensation, and selectively connect 0.1uF capacitor for high frequency noise decoupling. **Notice: 1V8O is the power for W5200 core operation. It should not be connected to the power of other devices.**
XTALVDD	I	16	 Figure 2 XTAL_VDD Reference Schematic Connect a capacitor of 10.1uF to the ground. ※ Refer to the 'W5200E01-M3 Reference schematic

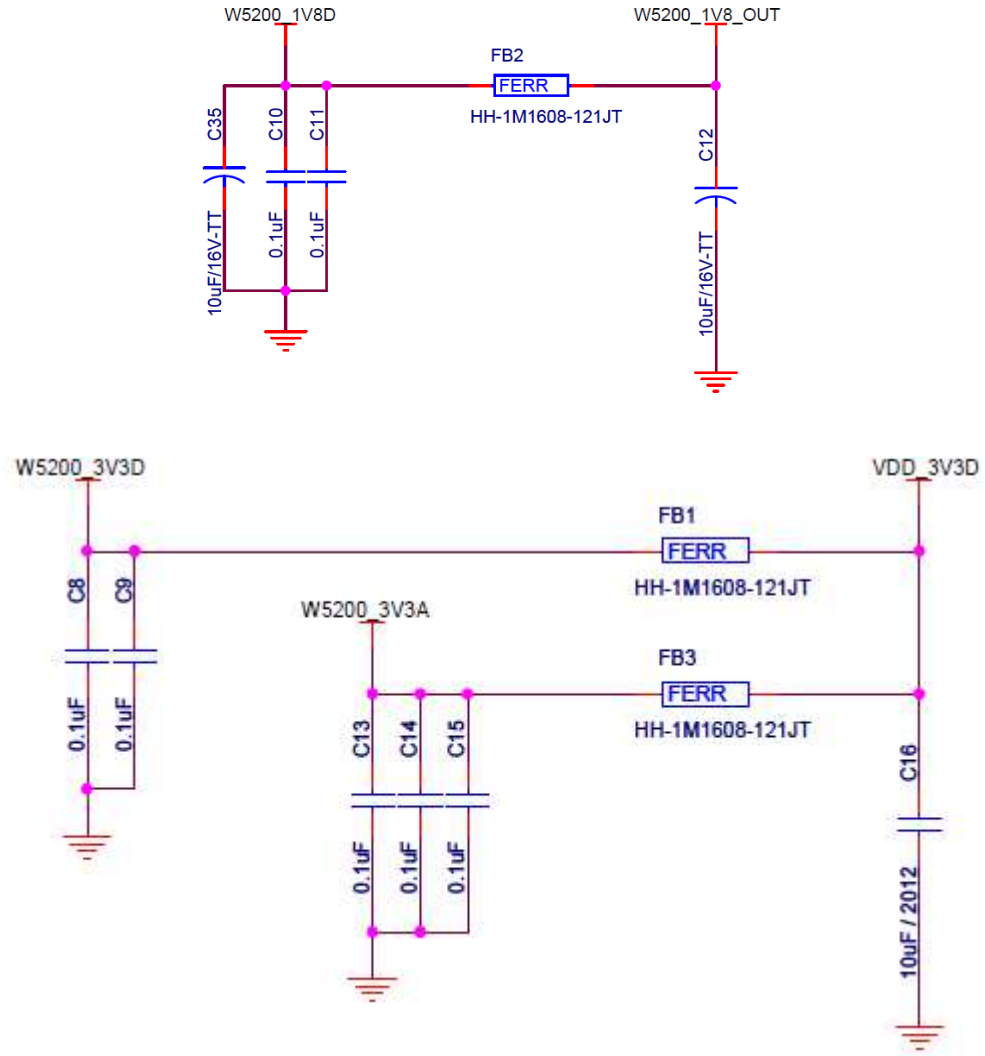


Figure 3 Power Design

Recommend for power design.

1. **Locate decoupling capacitor as close as possible to W5200.**
2. **Use ground plane as wide as possible.**
3. **If ground plane width is adequate, having a separate analog ground plane and digital ground plane is good practice.**
4. **If ground plane is not wide, design analog and digital ground planes as a single ground plane, rather than separate them.**

1.5 Clock Signals

Symbol	Type	Pin No	Description
XI	I	1	25MHz crystal input/output. A 25MHz crystal and Oscillator is used to connect these pins.
XO	O	2	

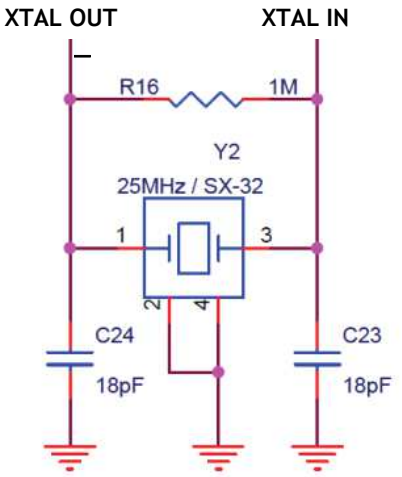


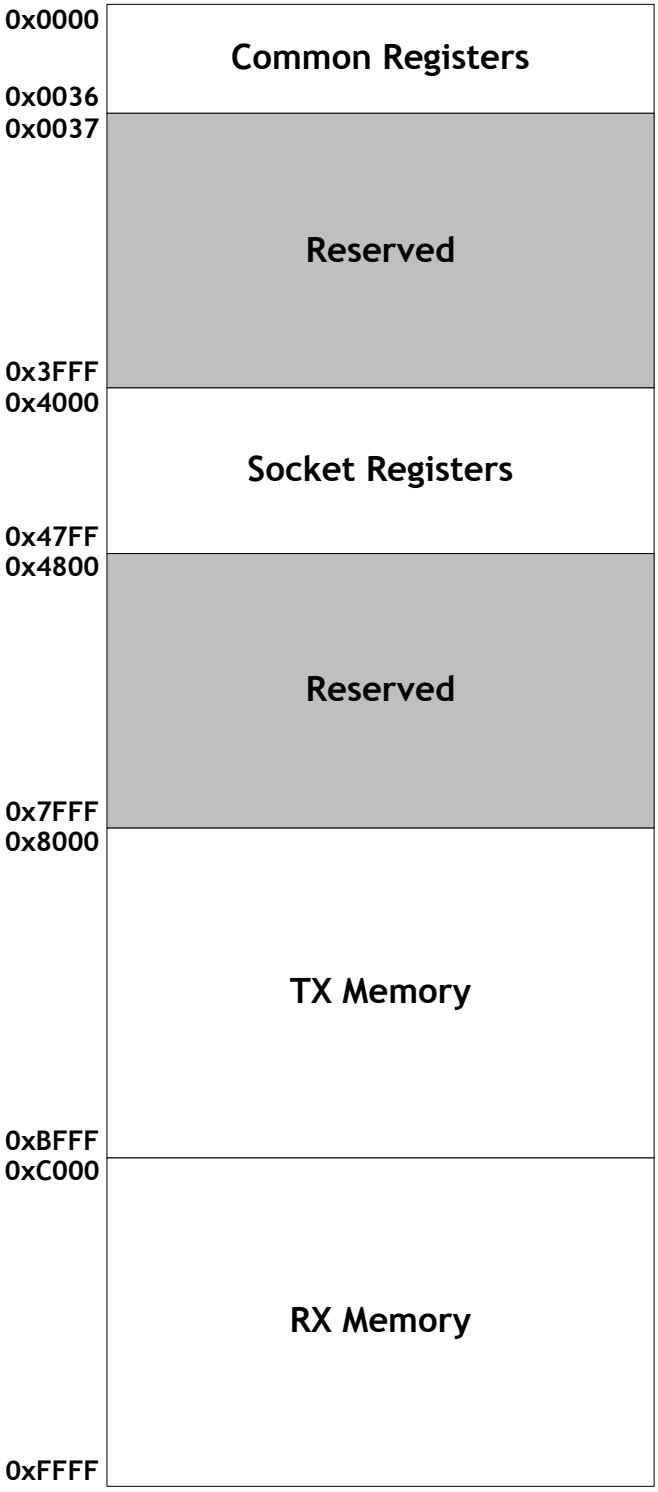
Figure 4 Crystal Reference Schematic

1.6 LED Signals

Symbol	Type	Pin No	Description
FDXLEDn/M2	O	3	**Full Duplex/Collision LED** Low: Full-duplex High: Half-duplex.
SPDLEDn/M1	O	4	**Link speed LED** Low: 100Mbps High: 10Mbps
LINKLEDn/M0	O	5	**Link LED** Low: Link (10/100M) High: Un-Link blink: TX or RX state on Link

2 Memory Map

W5200 is composed of Common Register, Socket Register, TX Memory, and RX Memory as shown below.



W5200 Memory Map

3 W5200 Registers

3.1 common registers

Address	Register
0x0000	Mode (MR)
0x0001 0x0002 0x0003 0x0004	Gateway Address (GAR0) (GAR1) (GAR2) (GAR3)
0x0005 0x0006 0x0007 0x0008	Subnet mask Address (SUBR0) (SUBR1) (SUBR2) (SUBR3)
0x0009 0x000A 0x000B 0x000C 0x000D 0x000E	Source Hardware Address (SHAR0) (SHAR1) (SHAR2) (SHAR3) (SHAR4) (SHAR5)
0x000F 0x0010 0x0011 0x0012	Source IP Address (SIPR0) (SIPR1) (SIPR2) (SIPR3)
0x0013 0x0014	Reserved
0x0015	Interrupt (IR)
0x0016	Interrupt Mask (IMR)
0x0017 0x0018	Retry Time (RTR0) (RTR1)
0x0019	Retry Count (RCR)
0x001A 0x001B	Reserved

Address	Register
0x001C 0x001D	Authentication Type in PPPoE (PATR0) (PATR1)
0x001E	Authentication Algorithm in PPPoE (PPPALGO)
0x001F	Chip version(VERSIONR)
0x0020 ~ 0x0027	Reserved
0x0028	PPP LCP RequestTimer (PTIMER)
0x0029	PPP LCP Magic number (PMAGIC)
0x002A ~ 0x002F	Reserved
0x0030 0x0031	Interrupt Low Level Timer (INTLEVEL0) (INTLEVEL1)
0x0032 ~ 0x0033	Reserved
0x0034	Socket Interrupt (IR2)
0x0035	PHY Status(PSTATUS)
0x0036	Socket Interrupt Mask (IMR2)

3.2 Socket registers

Note : n is socket number (0, 1, 2, 3, 4, 5, 6, 7)

Address	Register
0x4n00	Socket n Mode (Sn_MR)
0x4n01	Socket n Command (Sn_CR)
0x4n02	Socket n Interrupt (Sn_IR)
0x4n03	Socket n Status (Sn_SR)
0x4n04	Socket n Source Port (Sn_PORT0)
0x4n05	(Sn_PORT1)
0x4n06	Socket n Destination Hardware Address (Sn_DHAR0)
0x4n07	(Sn_DHAR1)
0x4n08	(Sn_DHAR2)
0x4n09	(Sn_DHAR3)
0x4n0A	(Sn_DHAR4)
0x4n0B	(Sn_DHAR5)
0x4n0C	Socket n Destination IP Address (Sn_DIPR0)
0x4n0D	(Sn_DIPR1)
0x4n0E	(Sn_DIPR2)
0x4n0F	(Sn_DIPR3)
0x4n10	Socket n Destination Port (Sn_DPORT0)
0x4n11	(Sn_DPORT1)
0x4n12	Socket n Maximum Segment Size (Sn_MSSR0)
0x4n13	(Sn_MSSR1)
0x4n14	Socket n Protocol in IP Raw mode (Sn_PROTO)
0x4n15	Socket n IP TOS (Sn_TOS)
0x4n16	Socket n IP TTL (Sn_TTL)
0x4n17 ~ 0x4n1D	Reserved

Address	Register
0x4n1E	Receive Memory Size (Sn_RXMEM_SIZE)
0x4n1F	Transmit Memory Size (Sn_TXMEM_SIZE)
0x4n20	Socket n TX Free Size (Sn_TX_FSR0)
0x4n21	(Sn_TX_FSR1)
0x4n22	Socket n TX Read Pointer (Sn_TX_RD0)
0x4n23	(Sn_TX_RD1)
0x4n24	Socket n TX Write Pointer (Sn_TX_WR0)
0x4n25	(Sn_TX_WR1)
0x4n26	Socket n RX Received Size (Sn_RX_RSR0)
0x4n27	(Sn_RX_RSR1)
0x4n28	Socket n RX Read Pointer (Sn_RX_RD0)
0x4n29	(Sn_RX_RD1)
0x4n2A	Socket n RX Write Pointer (Sn_RX_WR0)
0x4n2B	(Sn_RX_WR1)
0x4n2C	Socket n Interrupt Mask (Sn_IMR)
0x4n2D	Socket n Fragment Offset in IP header (Sn_FRAG0)
0x4n2E	(Sn_FRAG1)
0x4n30 ~ 0x4nFF	Reserved

4 Register Descriptions

4.1 Common Registers

MR (Mode Register) [R/W] [0x0000] [0x00]

This register is used for S/W reset, ping block mode and PPPoE mode.

7	6	5	4	3	2	1	0
RST		WOL	PB	PPPoE			

Bit	Symbol	Description
7	RST	**S/W Reset** If this bit is '1', internal register will be initialized. It will be automatically cleared after reset.
6	Reserved	Reserved
5	WOL	**Wake on LAN** 0:Normal Mode 1:WOL mode If the bit is set as '1', there is waiting for the Magic Packet.
4	PB	**Ping Block Mode** 0 : Disable Ping block 1 : Enable Ping block If the bit is set as '1', there is no response to the ping request.
3	PPPoE	**PPPoE Mode** 0 : DisablePPPoE mode 1 : EnablePPPoE mode If you use ADSL without router or etc, you should set the bit as '1' to connect to ADSL Server. For more detail, refer to the application note, *"How to connect ADSL"*.
2	Reserved	Reserved
1	Reserved	Reserved
0	Reserved	Reserved

GAR (Gateway IP Address Register) [R/W] [0x0001 – 0x0004] [0x00]

This Register sets up the default gateway address.

Ex) In case of "192.168.0.1"

0x0001	0x0002	0x0003	0x0004
192 (0xC0)	168 (0xA8)	0 (0x00)	1 (0x01)

SUBR (Subnet Mask Register) [R/W] [0x0005 – 0x0008] [0x00]

This register sets up the subnet mask address.

Ex) In case of "255.255.255.0"

0x0005	0x0006	0x0007	0x0008
255 (0xFF)	255 (0xFF)	255 (0xFF)	0 (0x00)

SHAR (Source Hardware Address Register) [R/W] [0x0009 – 0x000E] [0x00]

This register sets up the Source Hardware address.

Ex) In case of "00.08.DC.01.02.03"

0x0009	0x000A	0x000B	0x000C	0x000D	0x000E
0x00	0x08	0xDC	0x01	0x02	0x03

SIPR (Source IP Address Register) [R/W] [0x000F – 0x0012] [0x00]

This register sets up the Source IP address.

Ex) In case of "192.168.0.2"

0x000F	0x0010	0x0011	0x0012
192 (0xC0)	168 (0xA8)	0 (0x00)	2 (0x02)

IR (Interrupt Register) [R] [0x0015] [0x00]

This register is accessed by the host processor to know the cause of interrupt. Any interruption can be masked in the Interrupt Mask Register (IMR2). The INTn signal retain low as long as any masked signal is set, and will not go high until all masked bits in this Register have been cleared.

7	6	5	4	3	2	1	0
CONFLICT	Reserved	PPPoE	Reserved	Reserved	Reserved	Reserved	Reserved

Bit	Symbol	Description
7	CONFLICT	**IP Conflict** It is set as '1' when there is ARP request with same IP address as Source IP address. This bit is cleared to '0' by writing '1' to this bit.
6	Reserved	Reserved
5	PPPoE	**PPPoE Connection Close** In the Point-to-Point Protocol over Ethernet (PPPoE) Mode, if the PPPoE connection is closed, '1' is set. This bit will be cleared to '0' by writing '1' to this bit.
4	Reserved	Reserved
3	Reserved	Reserved
2	Reserved	Reserved
1	Reserved	Reserved
0	Reserved	Reserved

IMR(Interrupt Mask Register)[R/W][0x0016][0x00]

The Interrupt Mask Register is used to mask interrupts. Each interrupt mask bit corresponds to a bit in the Interrupt Register2 (IR2). If an interrupt mask bit is set, an interruption will be issued whenever the corresponding bit in the IR2 is set. If any bit in the IMR is set as '0' an interrupt will not occur though the bit.

7	6	5	4	3	2	1	0
S7_IMR	S6_IMR	S5_IMR	S4_IMR	S3_IMR	S2_IMR	S1_IMR	S0_IMR

Bit	Symbol	Description
7	S7_IMR	IR2(S7_INT) Interrupt Mask
6	S6_IMR	IR2(S6_INT) Interrupt Mask
5	S5_IMR	IR2(S5_INT) Interrupt Mask
4	S4_IMR	IR2(S4_INT) Interrupt Mask
3	S3_IMR	IR2(S3_INT) Interrupt Mask
2	S2_IMR	IR2(S2_INT) Interrupt Mask
1	S1_IMR	IR2(S1_INT) Interrupt Mask
0	S0_IMR	IR2(S0_INT) Interrupt Mask

RTR (Retry Time-value Register) [R/W] [0x0017 – 0x0018] [0x07D0]

It configures the retransmission timeout-period. The standard unit of RTR is 100us. RTR is initialized with 2000(0x07D0) and has 200ms timeout-period.

Ex) When timeout-period is set as 400ms, RTR = (400ms / 1ms) X 10 = 4000(0x0FA0)

0x0017	0x0018
0x0F	0xA0

Re-transmission will occur if there is no response from the remote peer to the commands of CONNECT, DISCON, CLOSE, SEND, SEND_MAC and SEND_KEEP, or the response is delayed.

RCR (Retry Count Register) [R/W] [0x0019] [0x08]

It configures the number of retransmission times. When retransmission occurs as many as 'RCR+1' times, Timeout interrupt is set ('TIMEOUT' bit of Sn_IR is set as '1').

In case of using TCP communication, the value of Sn_SR (Socket n Status Register) is changed to 'SOCK_CLOSED' and Sn_IR(Socket n Status Register) (TIMEOUT) turns into '1'.

In case of not using TCP communication, only Sn_IR(TIMEOUT) turns into '1'.

Ex) RCR = 0x0007

0x0019
0x07

The timeout of W5200 can be configurable with RTR and RCR. W5200's timeout has Address Resolution Protocol (ARP) and TCP retransmission timeout.

At the ARP (Refer to RFC 826, http://www.ietf.org/rfc.html) retransmission timeout, W5200 automatically sends ARP-request to the peer's IP address in order to acquire MAC address information (used for communication of IP, UDP, or TCP). As waiting for ARP-response from the peer, if there is no response during the time set in RTR, Timeout occurs and ARP-request is re-transmitted. It is repeated as many as 'RCR + 1' times.

Even after ARP-request retransmissions are repeated 'RCR + 1' times, if there is no ARP-response, the final timeout occurs and Sn_IR(TIMEOUT) becomes '1'.

The value of final timeout (ARP_{TO}) of ARP-request is as below.

$$ARP_{TO} = (RTR \times 0.1ms) \times (RCR + 1)$$

At the TCP packet retransmission timeout, W5200 transmits TCP packets (SYN, FIN, RST, DATA packets) and waits for the acknowledgement (ACK) during the time set in RTR and RCR. If there is no ACK from the peer, Timeout occurs and TCP packets (sent earlier) are retransmitted. The retransmissions are repeated as many as 'RCR + 1' times. Even after TCP packet retransmissions are repeated 'RCR +1' times, if there is no ACK from the peer, final timeout occurs and Sn_SR is changed to 'SOCK_CLOSED" at the same time with Sn_IR(TIMEOUT) = '1'

$$TCP_{TO} = \left(\sum_{N=0}^{M} (RTR \times 2^N) + ((RCR-M) \times RTR_{MAX}) \right) \times 0.1ms$$

N : Retransmission count, $0 <= N <= M$
M : Minimum value when $RTR \times 2^{(M+1)} > 65535$ and $0 <= M <= RCR$
RTR_{MAX} : $RTR \times 2^M$

Ex) When RTR = 2000(0x07D0), RCR = 8(0x0008),

ARP_{TO} = 2000 X 0.1ms X 9 = 1800ms = 1.8s

TCP_{TO} = (0x07D0 + 0x0FA0 + 0x1F40 + 0x3E80 + 0x7D00 + 0xFA00 + 0xFA00 + 0xFA00 + 0xFA00) X 0.1ms
= (2000 + 4000 + 8000 + 16000 + 32000 + ((8 - 4) X 64000)) X 0.1ms
= 318000 X 0.1ms = 31.8s

The value of final timeout (TCP_{TO}) of TCP packet retransmission can be calculated as below,

PATR (Authentication Type in PPPoE mode) [R] [0x001C-0x001D] [0x0000]

This register notifies authentication method that has been agreed at the connection with PPPoE Server. W5200 supports two types of Authentication method - PAP and CHAP.

Value	Authentication Type
0xC023	PAP
0xC223	CHAP

PPPALGO(Authentication Algorithm in PPPoE mode)[R][0x001E][0x00]

This register notifies authentication algorithm in PPPoE mode. For detailed information, please refer to PPPoE application note.

VERSIONR (W5200 Chip Version Register)[R][0x001F][0x03]

This register is the W5200 chip version register.

PTIMER (PPP Link Control Protocol Request Timer Register) [R/W] [0x0028]

This register indicates the duration for sending LCP Echo Request. Value 1 is about 25ms.

Ex) in case that PTIMER is 200,

200 * 25(ms) = 5000(ms) = 5 seconds

PMAGIC (PPP Link Control Protocol Magic number Register) [R/W] [0x0029][0x00]

This register is used in Magic number option during LCP negotiation. Refer to the application note, *"How to connect ADSL"*.

INTLEVEL (Interrupt Low Level Timer Register)[R/W][0x0030 - 0x0031][0x0000]

It sets Interrupt Assert wait time (I_{AWT}). It configures INTn Low Assert waiting time until the next interrupt.

$$I_{AWT} = (INTLEVEL + 1) * PLL\_CLK^{1} \text{ (when INTLEVEL > 0)}$$

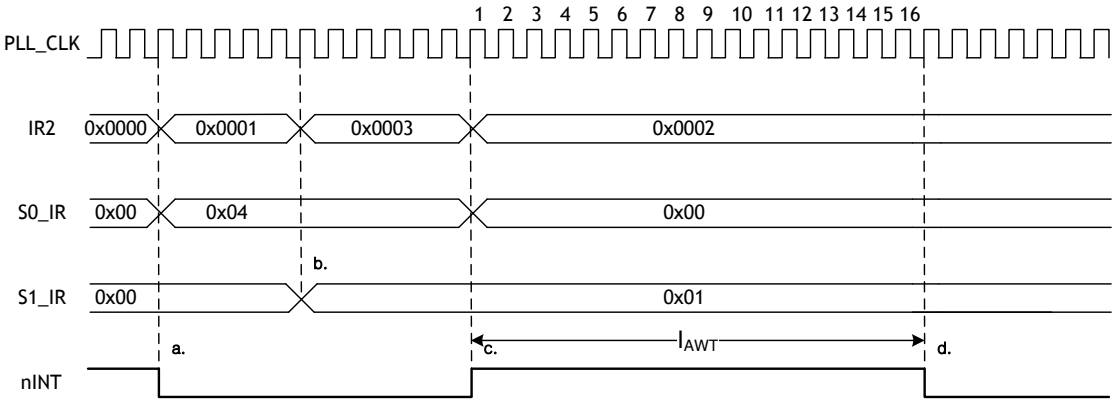


Figure 5 INTLEVEL Timing

a. At SOCKET 0, Receive Timeout Interrupt occurs (S0_IR(3) = '1') and corresponding IR2 bit is set as '1' (IR(S0_IR) = '1'). INTn signal is asserted low.

b. At SOCKET 1, Connected Interrupt occurs (S1_IR(0) = '1') and corresponding IR2 bit set as '1' (IR2(S1_IR) = '1').

c. The Host clears S0_IR(S0_IR = 0x00) and corresponding IR2 bit is automatically cleared

[1] PLL_CLK is 125MHz

(IR2(S0_IR) = '0'). INTn signal becomes High.

d. S0_IR is cleared. As IR2 is not 0x00, INTn should be asserted low right after 1PLL_CLK. However, as INTLEVEL is 0x000F, the interrupt about IR is processed after I_{AWT}(16 PLL_CLK).

IR2(W5200 SOCKET Interrupt Register)[R/W][0x0034][0x00]

IR2 is the Register to notify W5200 SOCKET interrupt to the Host. If any interrupt occurs, the related bit of IR2 is set as '1'. When related Mask Bit is '1', INTn signal is asserted low. INTn keeps low until all bits of Sn_IR becomes '0'. If all bits of Sn_IR become '0', it becomes high automatically.

7	6	5	4	3	2	1	0
S7_INT	S6_INT	S5_INT	S4_INT	S3_INT	S2_INT	S1_INT	S0_INT

Bit	Symbol	Description
7	S7_INT	When an interrupt occurs at SOCKET 7 , it becomes '1'. This interrupt information is applied to S7_IR. This bit is automatically cleared when S7_IR is cleared to 0x00 by host.
6	S6_INT	When an interrupt occurs at SOCKET 6 , it becomes '1'. This interrupt information is applied to S6_IR. This bit is automatically cleared when S6_IR is cleared to 0x00 by host.
5	S5_INT	When an interrupt occurs at SOCKET 5 , it becomes '1'. This interrupt information is applied to S5_IR. This bit is automatically cleared when S5_IR is cleared to 0x00 by host.
4	S4_INT	When an interrupt occurs at SOCKET 4 , it becomes '1'. This interrupt information is applied to S4_IR. This bit is automatically cleared when S4_IR is cleared to 0x00 by host.
3	S3_INT	When an interrupt occurs at SOCKET 3 , it becomes '1'. This interrupt information is applied to S3_IR. This bit is automatically cleared when S3_IR is cleared to 0x00 by host.
2	S2_INT	When an interrupt occurs at SOCKET 2 , it becomes '1'. This interrupt information is applied to S2_IR. This bit is automatically cleared when S2_IR is cleared to 0x00 by host.
1	S1_INT	When an interrupt occurs at SOCKET 1 , it becomes '1'. This interrupt information is applied to S1_IR. This bit is automatically cleared when S1_IR is cleared to 0x00 by host.
0	S0_INT	When an interrupt occurs at SOCKET 0 , it becomes '0'. This interrupt information is applied to S0_IR. This bit is automatically cleared when S0_IR is cleared to 0x00 by host.

PHYSTATUS(W5200 PHY status Register)[R/W][0x0035][0x00]

PHYSTATUS is the Register to indicate W5200 status of PHY.

Bit	Symbol	Description
7	Reserved	Reserved
6	Reserved	Reserved
5	LINK	**Link Status Register[Read Only]** This register indicates Link status. 0 : Link down 1 : Link Up
4	Reserved	Reserved
3	POWERDOWN	**Power down mode of PHY[Read/Write]** This register indicates status of Power down mode 0 : Disable Power down mode(operates normal mode) 1 : Enable Power down mode
2	Reserved	Reserved
1	Reserved	Reserved
0	Reserved	Reserved

IMR2 (Socket Interrupt Mask Register2) [R/W] [0x0036] [0x00]

The IMR2(Socket Interrupt Mask Register) is used to mask interrupts. Each interrupt mask bit corresponds to a bit in the Interrupt Register (IR). If an interrupt mask bit is set, an interrupt will be issued whenever the corresponding bit in the IR is set. If any bit in the IMR2 is set as '0', an interrupt will not occur though the bit in the IR is set.

7	6	5	4	3	2	1	0
IM_IR7	Reserved	IM_IR5	Reserved	Reserved	Reserved	Reserved	Reserved

Bit	Symbol	Description
7	IM_IR7	**IP Conflict Enable**
6	Reserved	Reserved
5	IM_IR5	**PPPoE Close Enable**
4	Reserved	Reserved
3	Reserved	Reserved
2	Reserved	Reserved
1	Reserved	Reserved
0	Reserved	Reserved

4.2 Socket Registers

S*n*[2]_MR (Socket n Mode Register) [R/W] [0x4000+0x0n00] [0x00][3]

This register sets up socket option or protocol type for each socket.

7	6	5	4	3	2	1	0
MULTI	MF	ND / MC		P3	P2	P1	P0

Bit	Symbol	Description
7	MULTI	Multicasting 0 : disable Multicasting 1 : enable Multicasting It is applied only in case of UDP. For using multicasting, write multicast group address to Socket n Destination IP and multicast group port number to Socket n Destination Port Register, before OPEN command.
6	MF	MAC Filter 0 : Disable MAC filter 1 : Enable MAC filter It is used in MACRAW (P3~P0: “0100”). When this bit is set as ‘1’, W5200 can receive packet that is belong in itself or broadcasting. When this bit is set as ‘0’, W5200 can receive all packets on Ethernet. When using the hybrid TCP/IP stack, it is recommended to be set as ‘1’ for reducing the receiving overhead of host.
5	ND/MC	Use No Delayed ACK 0 : Disable No Delayed ACK option 1 : Enable No Delayed ACK option, This only applies to TCP case (P3-P0 : “0001”) If this bit is set as ‘1’, ACK packet is immediately transmitted after receiving data packet from a peer. If this bit is cleared, ACK packet is transmitted according to internal timeout mechanism. Multicast 0 : using IGMP version 2 1 : using IGMP version 1 This bit is valid when MULTI bit is enabled and UDP mode is used (P3-P0 : “0010”). In addition, multicast can be used to send out the version number in IGMP messages such as Join/Leave/Report to multicast-group

[2] *n* is Socket n-thumber (0, 1, 2, 3, 4, 5, 6, 7).
[3] [Read/Write] [address of socket 0, address of socket 1, address of socket 2, address of socket 3,address of socket 4, address of socket 5, address of socket 6, address of socket 7] [Reset value]

<table>
<tr><td>4</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>3</td><td>P3</td><td rowspan="4">Protocol
Sets up corresponding socket as TCP, UDP, or IP RAW mode
<table><tr><th>P3</th><th>P2</th><th>P1</th><th>P0</th><th>Meaning</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Closed</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>TCP</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>UDP</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>IPRAW</td></tr></table>
* In case of socket 0, MACRAW and PPPoE mode exist.
<table><tr><th>P3</th><th>P2</th><th>P1</th><th>P0</th><th>Meaning</th></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>MACRAW</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>PPPoE</td></tr></table>
S0_MR_MACRAW and S0_MR_PPPoE are valid only in SOCKET 0.
S0_MR_PPPoE is temporarily used for PPPoE server connection/Termination. After connection is established, it can be utilized as another protocol.</td></tr>
<tr><td>2</td><td>P2</td></tr>
<tr><td>1</td><td>P1</td></tr>
<tr><td>0</td><td>P0</td></tr>
</table>