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High-Performance Internet Connectivity Solution

W5300

Version 1.2.5

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Document History Information

Version	Date	Descriptions
Ver. 1.0.0	Mar. 11, 2008	Release with W5300 launching
Ver. 1.1.0	May. 15, 2008	◦ Correct a number of typing errors ◦ 4.4 SOCKET Register >> Sn_DPORTR R/W → WO, Modify the description, Refer to P.77 ◦ 4.4 SOCKET Register >> Sn_MSSR In the MSS Table, Modified the PPPoE MSS value of MACRAW(1502 → 1514), Refer to P.79 ◦ 5.2.1.1 TCP SERVER >> ▪ ESTABLISHED : Receiving process At the <Notice> phase, Modified the example code Replace 'SEND' with 'SEND_KEEP'. Refer to P.93~94 ◦ 5.2.4 MACRAW >> ▪ Receiving process At the <NOTICE> phase, Modified the free size and CRC Free size 1526 → 1528, CRC(2) → CRC(4), Refer to P.111
Ver. 1.1.1	July 4, 2008	◦ Correct a number of typing errors ◦ Add PIN "BRDYn" description to "1.3 Host Interface signal" ◦ 5.2.1.1 TCP SERVER >> ▪ ESTABLISHED : Receiving process At the <Notice> phase, Modified the example code Replace 'SEND_KEEP' with 'SEND'. Refer to P.93~94
Ver 1.2	Dec. 30, 2008	◦ 1. PIN Description Add to '8' Symbol ◦ 1.2 Configuration Signals Modify ADDR type (ID → I), No Internal Pulled-down Modify DATA[15:0] type (IO → IO8) ◦ 6.2. Indirect Address Mode ADDR[9:0] has no internal pulled-down resister. So, ADDR[9:3] should be connected to ground for using indirect address mode.

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		Modify the description & figures.
Ver 1.2.1	Jan. 22, 2009	◦ Modify the Figure 2. Ferrite Bead 0.1uF → 1uH
Ver 1.2.2	Feb. 16, 2009	◦ 1.7 Clock Signals. Delete XTLP/XTLN Pin Type ◦ 7. Electrical Specifications - DC Characteristics : Modify the Test Condition of $V_{OH,}$ V_{OL} : V_{OH} - Min (2.0(2.4), Delete Typical and Max value : V_{OL} – Delete Min and Typical value
V1.2.3	Feb.11, 2010	◦ Change Figure 2 - Change W5300 Power Supply Signal schemati
V1.2.4	Aug. 19, 2010	- Change Temperature condition (p.119)
V1.2.5	Sep. 29, 2010	- Modify Table 1.8 Power Supply Signal (p.19) --1V8O: **1.8V regulator output voltage** Capacitor value: 0.1uF -> 10Uf - Modified Fig.2 Power Design (p.21)

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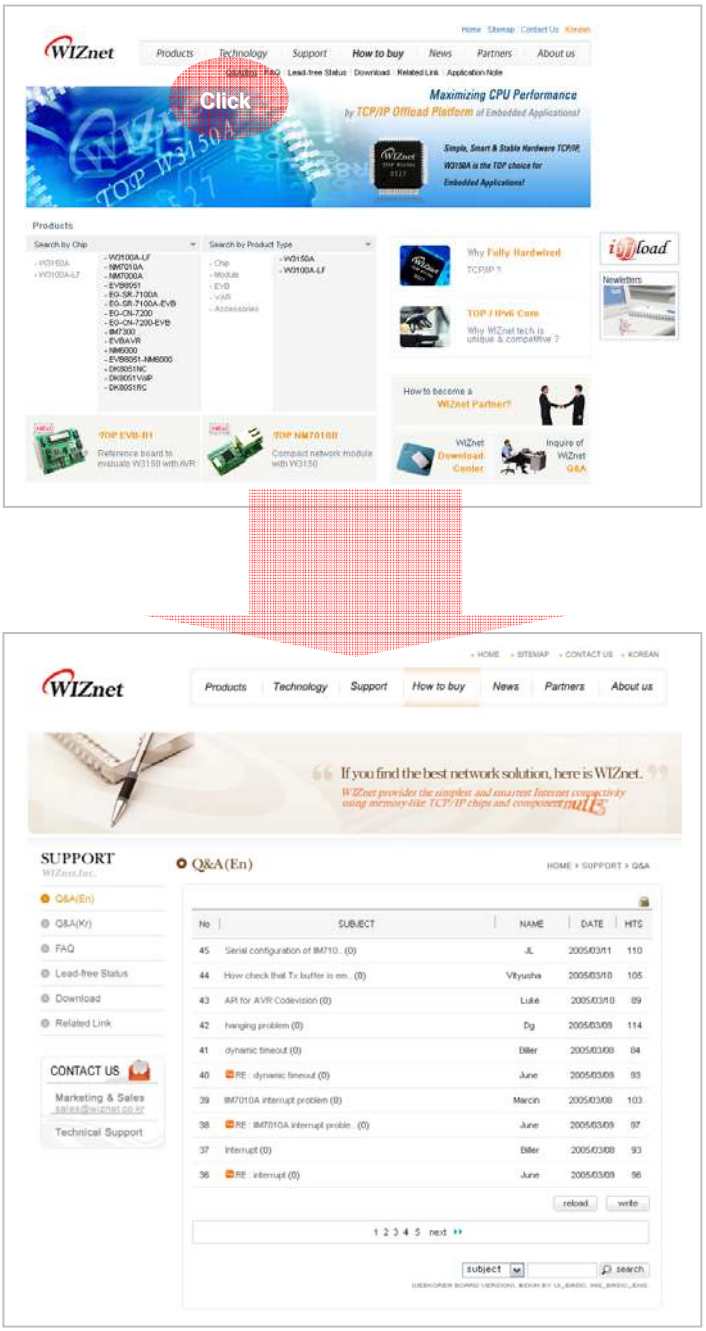

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W5300

W5300 is a 0.18 μm CMOS technology single chip into which 10/100 Ethernet controller, MAC, and TCP/IP are integrated. W5300 is designed for Internet embedded applications where easy implementation, stability, high performance, and effective cost are required.

W5300's target application is the embedded internet solution requiring high performance such as multi-media streaming service. Comparing to existing WIZnet chip solution, W5300 has been improved in memory and data process. W5300 is the most appropriate to the products of IPTV, IP-STB and DTV transferring multi-media data with high-capacity.

The Internet connectivity can be implemented easily and quickly only with single chip having TCP/IP protocol and 10/100 Ethernet MAC & PHY.

High-Performance Hardware TCP/IP single chip solutions

WIZnet retains the technology of full hardware logic of communication protocols such as TCP, UDP, IPv4, ICMP, IGMP, ARP and PPPoE. In order to provide high-performing data communication, the data communication memory is extended to 128Kbyte and 16bit bus interface is supported in W5300. Users can utilize independent 8 hardware SOCKETs for high-speed data communication.

More flexible memory allocation for various applications

The memory for data communication can be allocated to each SOCKET in the range of 0~64Kbytes. It is more flexible for users to utilize the memory according to their application. Users can develop more efficient system by concentrating on the application of high performance.

Easy to implements for beginners

W5300 supports BUS interface as the host interface. By using direct and indirect access methods, W5300 can easily interfaced to the host as like SRAM memory. The data communication memory of W5300 can be accessed through TX/RX FIFO registers that exist in each SOCKET. With these features, even beginners can implement Internet connectivity by using W5300.

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Target Applications

The W5300 is well-suited for many embedded applications, including:

- Home Network Devices: Set-Top Boxes, PVRs, Digital Media Adapters
- Serial-to-Ethernet: Access Controls, LED displays, etc.
- Parallel-to-Ethernet: POS / Mini Printers, Copiers
- USB-to-Ethernet: Storage Devices, Network Printers
- GPIO-to-Ethernet: Home Network Sensors
- Security Systems: DVRs, Network Cameras, Kiosks
- Factory and Building Automation
- Medical Monitoring Equipment
- Embedded Servers

Features

- Supports hardwired TCP/IP protocols : TCP,UDP,ICMP,IPv4,ARP,IGMPv2,PPPoE,Ethernet
- Supports 8 independent SOCKETs simultaneously
- High network performance : Up to 50Mbps
- Supports hybrid TCP/IP stack(software and hardware TCP/IP stack)
- Supports PPPoE connection (with PAP/CHAP Authentication mode)
- IP Fragmentation is not supported
- Internal 128Kbytes memory for data communication(Internal TX/RX memory)
- More flexible allocation internal TX/RX memory according to application throughput
- Supports memory-to-memory DMA (only 16bit Data bus width & slave mode)
- Embedded 10BaseT/100BaseTX Ethernet PHY
- Supports auto negotiation (Full-duplex and half duplex)
- Supports auto MDI/MDIX(Crossover)
- Supports network Indicator LEDs (TX, RX, Full/Half duplex, Collision, Link, Speed)
- Supports a external PHY instead of the internal PHY
- Supports 16/8 bit data bus width
- Supports 2 host interface mode(Direct address mode & Indirect address mode)
- External 25MHz operation frequency (For internal PLL logic, period=40ns)
- Internal 150MHz core operation frequency (PLL_CLK, period=about 6.67ns)
- Network operation frequency (NIC_CLK : 25MHz(100BaseTX) or 2.5MHz(10BaseT))
- 3.3V operation with 5V I/O signal tolerance
- Embedded power regulator for 1.8V core operation
- 0.18 μm CMOS technology
- 100LQFP 14X14 Lead-Free Package

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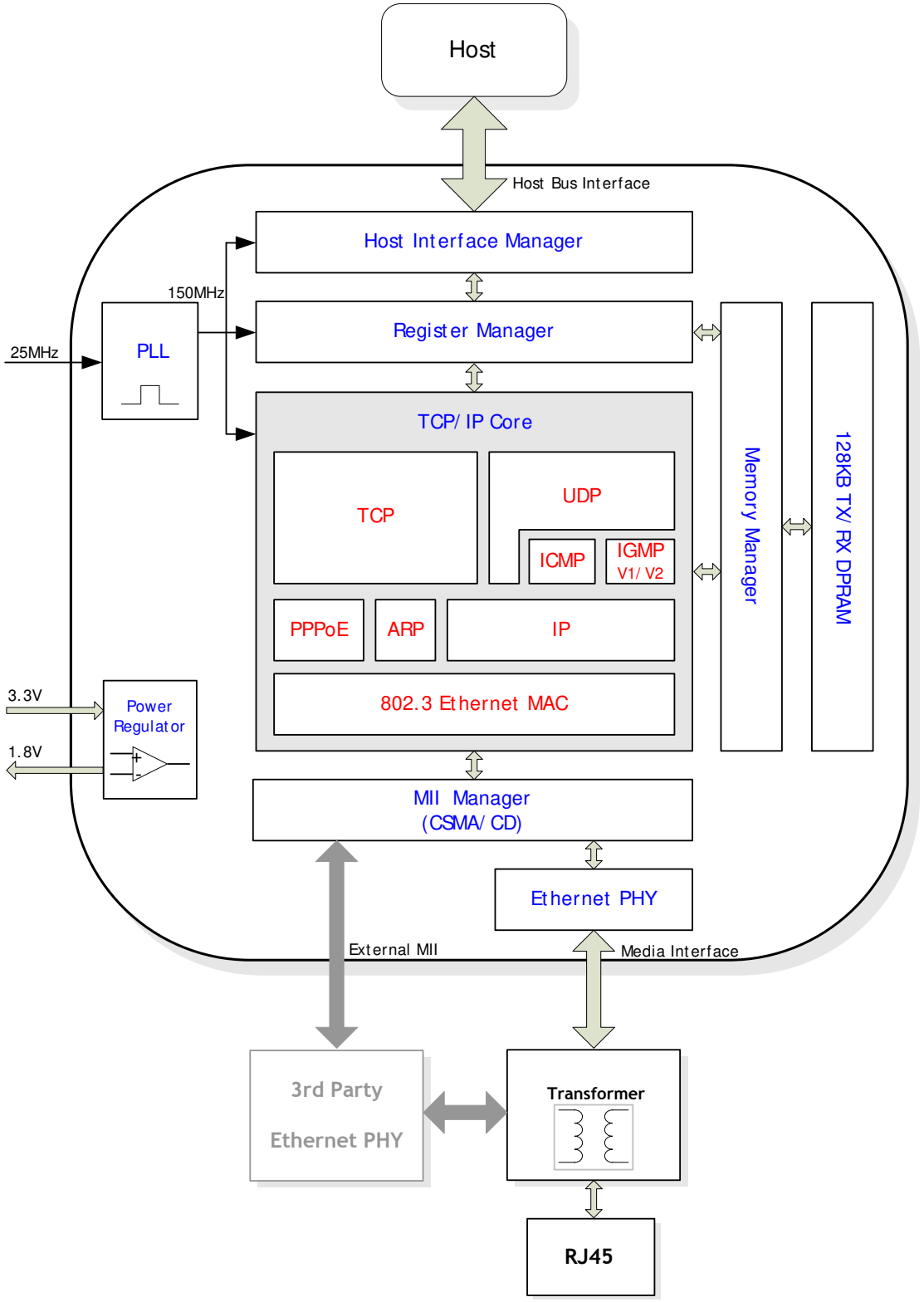
Block Diagram



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PLL(Phase-Locked Loop)

It creates a 150MHz clock signal by multiplying 25MHz clock source by six. The 150MHz clock is used for operating internal blocks such as TCP/IP core block, 'Host Interface Manager' and 'Register Manager'. PLL is locked-in after reset and it supplies a stable clock.

Power Regulator

With 3.3V power input, the power regulator creates 1.8V/150mA power. This power regulator supplies the power for core operation of W5300. It is not required to add other power regulators, but recommended to add a capacitor for more stable 1.8V power supplying.

Host Interface Manager

It detects host bus signal, and manages read/write operations of the host according to data bus width or host interface mode.

Register Manager

It manages Mode register, COMMON Register, and SOCKET Register.

Memory Manager

It manages internal data memory of 128KBytes – TX/RX memory allocated in each SOCKET by the host. The host can access the memory only through TX/RX FIFO Register of each SOCKET.

128KB TX/RX DPRAM

It is the 128KByte memory for data communication and composed of 16 DPRAM(Dual-Port RAM) of 8KBytes. It is allocated flexibly to each SOCKET by the host.

MII(Media Independent Interface) Manager

It manages MII interface. MII interface can be switched to internal PHY or external PHY(3rd party PHY) according to the configuration of TEST_MODE[3:0].

Internal Ethernet PHY

W5300 includes 10BaseT/100BaseTX Ethernet PHY. Internal PHY supports half-duplex/full duplex, auto-negotiation and auto MDI/MDIX. It also supports 6 network indicator LED output such as Link status, speed and duplex.

TCP/IP Core

TCP/IP Core is the fully hardwired logic based on network protocol processing technology of WIZnet.

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- **802.3 Ethernet MAC(Media Access Control)**

  It controls Ethernet access of CSMA/CD(Carrier Sense Multiple Access with Collision Detect). It is the protocol technology based on a 48-bit source/destination MAC address. It also allows the host to control MAC layer through its 0th SOCKET. So, it is possible to implement software TCP/IP stack together with hardware TCP/IP stack.

- **PPPoE(Point-To-Point Protocol over Ethernet)**

  It is the protocol technology to use PPP service at the Ethernet. It encapsulates the payload(data) part of Ethernet frame as the PPP frame and transmits it. When receiving, it de-capsulates the PPP frame. PPPoE supports PPP communication with PPPoE server and PAP/CHAP authentication methods.

- **ARP(Address Resolution Protocol)**

  ARP is the MAC address resolution protocol by using IP address. It transmits the ARP-reply to the ARP-request from the peer. It also sends ARP-request to find the MAC address of the peer and processes the ARP-reply to the request.

- **IP(Internet Protocol)**

  IP is the protocol technology to support data communication at the IP layer. IP fragmentation is not supported. It is not possible to receive the fragmented packets. Except for TCP or UDP, all protocol number is supported. In case of TCP or UDP, use the hardwired stack.

- **ICMP(Internet Control Message Protocol)**

  It receives the ICMP packets such as the fragment MTU, unreachable destination, and notifies the host. After receiving Ping-request ICMP packet, it transmits Ping-reply ICMP packet. It supports maximum 119 Byte as Ping-request size. If the size is over 119Bytes, it is not supported.

- **IGMPv1/v2(Internet Group Management Protocol version 1/2)**

  It processes IGMP such as IGMP Join/Leave, Report at the UDP multicasting mode. Only version 1 and 2 of IGMP logic is supported. When using upper version of IGMP, it should be manually implemented by using IP layer.

- **UDP(User Datagram Protocol)**

  It is the protocol technology to support data communication at the UDP layer. It supports user datagram such as unicast, multicast, and broadcast.

- **TCP(Transmission Control Protocol)**

  It is the protocol technology to support data communication at the TCP layer. It supports “TCP SERVER” and “TCP CLIENT” communication.

W5300 internally processes all protocol communication without intervention of the host. W5300 is based on TOE(TCP/IP Offload Engine) that can maximize the host performance by reducing the host overhead in processing TCP/IP stack.

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1. PIN Description

Type	Description	Type	Description
I	Input	D	Internal pulled-down with 75KΩ resistor
O	Output with driving current 2mA	M	Multi-function
IO	Input/Output (Bidirectional)	H	Active high
U	Internal pulled-up with 75KΩ resistor	L	Active low
O8	Output with driving current 8mA		

<Notation> IUL : Input PIN with 75KΩ pull-up resistor. Active low

OM : Multi-functional Output PIN

1.1 PIN Layout

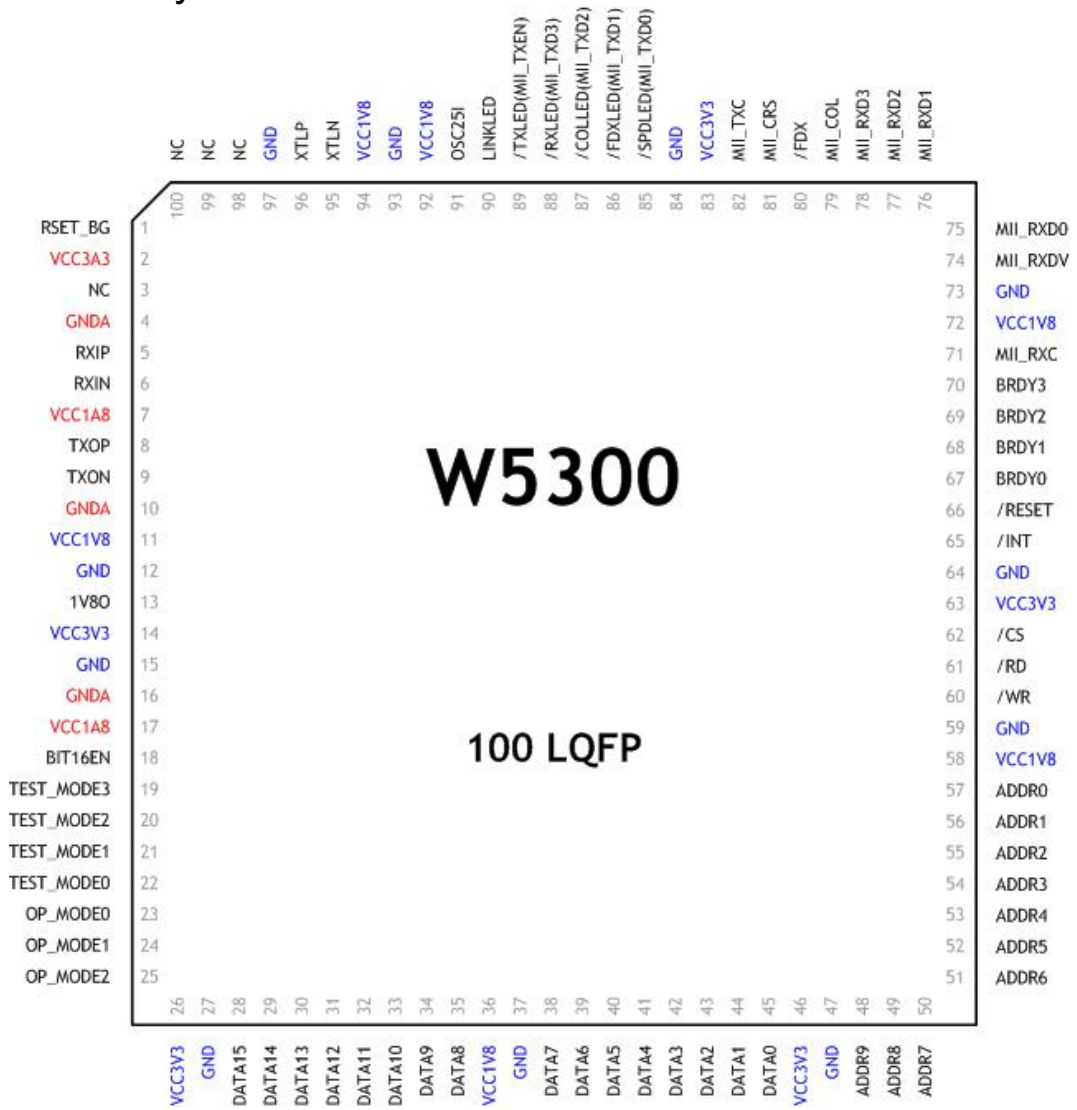

Fig 1. PIN Layout

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1.2 Configuration Signals

<table>
<tr><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>TEST_MODE[3:0]</td><td>ID</td><td>W5300 mode select

It configures PHY mode and factory test mode of W5300.

<table>
<tr><th colspan="4">TEST_MODE</th><th rowspan="2">Description</th></tr>
<tr><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Internal PHY Mode (Normal Operation)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>External PHY Mode with Crystal clock</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>External PHY Mode with Oscillator clock</td></tr>
<tr><td colspan="4">Others</td><td>Reserved (Factory Test Mode)</td></tr>
</table>

At the external PHY mode, Clock input pin is changed by clock source. Refer to “1.7 Clock Signals”.</td></tr>
<tr><td>OP_MODE[2:0]</td><td>ID</td><td>Internal PHY operation control mode

It configures the operation mode of internal PHY.
<table>
<tr><th colspan="3">OP_MODE</th><th rowspan="2">Description</th></tr>
<tr><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Normal Operation Mode, Recommended
Auto-negotiation enable with all capabilities</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Auto-negotiation with 100 BASE-TX FDX/HDX ability</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Auto-negotiation with 10 BASE-T FDX/HDX ability</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Manual selection of 100 BASE-TX FDX</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Manual selection of 100 BASE-TX HDX</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Manual selection of 10 BASE-T FDX</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Manual selection of 10 BASE-T HDX</td></tr>
</table>
cf> FDX : Full-duplex, HDX : Half-duplex

The setting value is latched after hardware reset.</td></tr>
</table>

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1.3 Host Interface Signals

Symbol	Type	Description
/RESET	IL	**RESET** Hardware Reset Signal. It initializes W5300. RESET should be held at least 2us after low assert, and wait for at least 10ms after high de-assert in order for PLL logic to be stable. Refer to RESET timing of “7 Electrical Specification” W5300 does not support Power-On-Reset. Therefore, it should be manually designed in the target system.
BIT16EN	IU	**16/8 BIT DATA BUS SELECT** High : 16 bit data bus Low : 8 bit data bus It determinates data bus width of W5300. At reset time, it is latched in 15th Bit(‘BW’)of Mode register(MR). After reset, its change is ignored. It means data bus width can’t be changed after reset. When using 8 bit data bus, it should be connected to ground.
ADDR9-0	I	**ADDRESS** System address bus. These are selected by host interface mode and data bus width of W5300. When using 16 bit data bus, ADDR0 is internally ignored. Refer to “6.External Interface”.
DATA[15:8]	IO	**DATA** System high data bus. These are used for read/write operation of W5300 register. In case of using 8 bit data bus, These are driven as High-Z.
DATA[7:0]	IO8	**DATA** System low data bus. These are used for read/write operation of W5300 register.
/CS	IL	**CHIP SELECT** Chip select signal.

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		Host selects W5300 at the W5300 read/write operation. When /CS is de-asserted high, DATA[15:0] are driven as High-Z.
/WR	IL	**WRITE ENABLE** Write enable signal. Host writes W5300 register addressed by ADDR[9:0] to DATA[15:0]. DATA[15:0] are latched in the W5300 register according to the configuration of the Write-data-fetch-timing. Refer to 13-11th bit(WDF[2:0] of MR).
/RD	IL	**READ ENABLE** Read enable signal. Host reads W5300 register addressed by ADDR[9:0] through DATA[15:0].
/INT	OL	**INTERRUPT** Interrupt Request Signal. It is asserted low when interrupt(connected, disconnected, data received, data sent or timeout) occurs on operating. When interrupt service is completed by host and Interrupt register(IR) is cleared by host, it is de-asserted high. Refer to IR, Interrupt Mask Register(IMR), SOCKETn Interrupt Register(Sn_IR), SOCKETn Interrupt Mask Register(Sn_IMR).
BRDY[3:0]	O	**Buffer Ready Indicator** These PIN are configured with SOCKET number, memory Type, and buffer depth by user. When TX free or RX received size of the specified SOCKET is same or greater than the configured buffer depth, these PIN signals asserts high or low. Refer to Pn_BRDYR & Pn_DPTHR in “4.3 COMMON Registers”.

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1.4 Media Interface Signals

Media(10Mbps/100Mbps) interface signals are used in internal PHY mode (TEST_Mode[3:0] = "0000"). Refer to "1.2 Configuration Signals".

Symbol	Type	Description
RXIP	I	**RXIP/RXIN Signal Pair** Differential receive Input signal pair. Receive data from the media. This signal pair needs 2 termination resistors 50Ω(±1%) and 1 capacitor 0.1uF for better impedance matching, and this resistor/capacitor pair is located near magnetic(transformer). If not used, connect to ground.
RXIN	I	
TXOP	O	**TXOP/TXON Signal Pair** Differential transmit output signal pair. Transmits data to the media. This signal pair needs 2 termination resistors 50Ω(±1%) and 1 capacitor 0.1uF for better impedance matching, and this resistor/capacitor pair should be located near W5300. If not used, just let them float.
TXON	O	
RSET_BG	O	**Off-chip Resistor** This pin should be pulled-down with 12.3 kΩ±1% resistor.

For the better performance,

1. Make the length of RXIP/RXIN signal pair (RX) same if possible.
2. Make the length of TXOP/TXON signal pail (TX) same if possible.
3. Locate the RXIP and RXIN signal as near as possible.
4. Locate the TXOP and TXON signal as near as possible.
5. Locate the RX and TX signal pairs far from noisy signals such as bias resistor or crystal.

For the detailed information refer to "W5100 Layout Guide.pdf"

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1.5 MII interface signal for external PHY

MII interface signals are for interfacing to external PHY instead of the internal PHY of W5300. These signals can be used at the external PHY mode (TEST_Mode[3:0] = “0001” or “0010”). Refer to “1.2 Configuration Signals”.

At the internal PHY mode, just let them float because the pins except for multi-function pins are internal pulled-down.

Symbol	Type	Description
/TXLED(**MII_TXEN**)	OMH	Transmit Act LED / **Transmit Enable** This signal indicates the presence of transmit packet on the MII_TXD[3:0]. It is asserted high when the first nibble data of transmit packet is valid on MII_TXD[3:0] and is de-asserted low after the last nibble data of transmit packet is clocked out on MII_TXD[3:0].
/RXLED(**MII_TXD3**) /COLLED(**MII_TXD2**) /FDXLED(**MII_TXD1**) /SPDLED(**MII_TXD0**)	OM	/RXLED,/COLLED,/LEDFDX,/SPDLED / **Transmit data output** The transmit packet is synchronized with MII_TXC clock and output to external PHY in nibble unit. MII_TXD3 is the Most Significant Bit (MSB).
MII_TXC	ID	**Transmit Clock Input** It is a continuous transmit clock from the external PHY. It is 25MHz at the 100BaseTX and 2.5MHz at the 10 BaseT. Transmit clock is used as timing reference of MII_TXD[3:0] and used for network operation clock (NIC_CLK). Rising Edge Sensitive.
MII_CRS	IDH	**Carrier Sense** It is signal to notify the link traffic of the media. If carrier of media is not idle (carrier present), it is asserted high.
MII_COL	IDH	**Collision Detect** When collision is detected on the media, it is asserted high. It is valid at the half-duplex and ignored at the full-duplex. Asynchronous signal.

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MII_RXD3 MII_RXD2 MII_RXD1 MII_RXD0	ID	**Receive Data Input** When MII_RXDV is high, the received packet is synchronized with MII_RXC and inputs in nibble unit. MII_RXD3 is MSB.
MII_RXDV	ID	**Receive Data Valid** This signal indicates the presence of received packet from MII_RXD[3:0]. It is asserted high when the first nibble data of the received packet is valid on MII_RXD[3:0] and is de-asserted low after the last nibble data of receive packet clocked in on MII_RXD[3:0]. It is valid when MII_RXC is at rising edge.
MII_RXC	ID	**Receive Clock Input** It is continuous receive clock from the external PHY. It is 25MHz at the 100Base TX and 2.5MHz at the 10BaseT. Receive clock is used for timing reference of MII_RXD[3:0] and MII_RXDV. Rising Edge Sensitive.
/FDX	IDL	**Full-Duplex Select** 0 : Full-duplex 1 : Half-duplex It is input signal from PHY that indicates link status of external PHY. Most of PHYs support auto-negotiation and notifies the result to network indicator LED or other signals. It can be connected to those signals and also it can be configurable manually by connecting high or low.

Recommend for the better performance.

1. MII interface signal line length should not be more than 25cm if possible.
2. The length of MII_TXD[3:0] should be same if possible.
3. The length of MII_RXD[3:0] should be same if possible.
4. The length of MII_TXC should not be longer than MII_TXD[3:0] signal line by 2.5cm.
5. The length of MII_RXC should not be longer than MII_RXD[3:0] signal line by 2.5cm.

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1.6 Network Indicator LED Signals

The signals except for LINKLED, are used as multi-function PIN according to the configuration of TEST_MODE[3:0]. When using those signals as network indicator signals, internal PHY mode(TEST_MODE[3:0]="0000") should be configured.

Symbol	Type	Description
LINKLED	OL	**Link LED** It indicates the link status of media(10/100M).
/**TXLED**(MII_TXEN)	OML	**Transmit activity LED**/Transmit Enable It notifies the output of transmit data through TXOP/TXON (Transmit Activity).
/**RXLED**(MII_TXD3)	OML	**Receive activity LED**/Transmit Data It notifies the input of receive data from RXIP/RXIN (Receive Activity) cf> By binding /TXLED and /RXLED signals with 'AND' gate, it can be used for network activity LED.
/**COLLED**(MII_TXD2)	OML	**Collision LED**/Transmit Data It notifies when collisions occur. It is valid at half-duplex, and is ignored at full-duplex.
/**FDXLED**(MII_TXD1)	OML	**Full duplex LED**/Transmit Data It outputs low at the full-duplex and outputs high at the half-duplex according to auto-negotiation or manual configuration of OP_MODE[2:0].
/**SPDLED**(MII_TXD0)	OML	**Link speed LED**/Transmit Data It is asserted low at the 100Mbps and high at the 10Mbps according to auto-negotiation or manual configuration of OP_MODE[2:0].

1.7 Clock Signals

For the clock source of W5300, either a crystal or an oscillator may be used. 25MHz frequency from the clock source is created to 150MHz frequency using internal PLL logic. This 150MHz

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frequency is used for PLL_CLK(Period 6.67ns) and W5300 core operation clock.

Symbol	Type	Description
XTLP		**25MHz crystal input/output** 25MHz parallel-resonant crystal is used with matching capacitor for internal oscillator stabilization.
XTLN		Refer to “Clock Characteristic” of “7.Electrical Specifications” These can be used for internal PHY mode(TEST_MODE[3:0]=”0000”) or external PHY mode with crystal clock (TEST_MODE[3:0]=”0001”). When using oscillator at the internal PHY mode, be sure to use 1.8V level oscillator and connect only to XTLP. And let be float XTLN.
OSC25I	I	**25MHz Oscillator input** It is used only in external PHY mode with oscillator clock (TEST_MODE[3:0]=”0010”). In order to prevent the leakage current, be sure to keep XTLP high and float XTLN, and use 1.8v level oscillator.

1.8 Power Supply Signals

Symbol	Type	Description
VCC3A3	Power	**3.3V power supply for Analog part** Be sure to connect 10uF tantalum capacitor between VCC343 and GNDA in order to prevent power compensation.
VCC3V3	Power	**3.3V power supply for Digital part** Between each VCC and GND, 0.1uF decoupling capacitor can be selectively connected. VCC3V3 can be separated to 1uH ferrite bead and connected to VCC3A3.
VCC1A8	Power	**1.8V power supply for Analog part** Be sure to connect a 10uF tantalum capacitor and 0.1uF capacitor between VCC1A8 and GNDA for core power noise filtering.
VCC1V8	Power	**1.8V power supply for Digital part** Between each VCC and GND, 0.1uF decoupling capacitor can be selectively connected.
GNDA	Ground	**Analog ground** Make analogue ground plane as wide as possible when designing the PCB layout.
GND	Ground	**Digital ground** Make digital ground plane as wide as possible when designing the

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		PCB layout.
1V8O	O	**1.8V regulator output voltage** 1.8V/150mA power created by internal power regulator, is used for core operation power (VCC1A8, VCC1V8). Be sure to connect 3.3uF tantalum capacitor between 1V8O and GND for output frequency compensation, and selectively connect 10uF capacitor for high frequency noise decoupling. 1V8O is connected to VCC1V8, separated to 1uH ferrite bead and connected to VCC1A8. <Notice> 1V8O is the power for W5300 core operation. It should not be connected to the power of other devices.

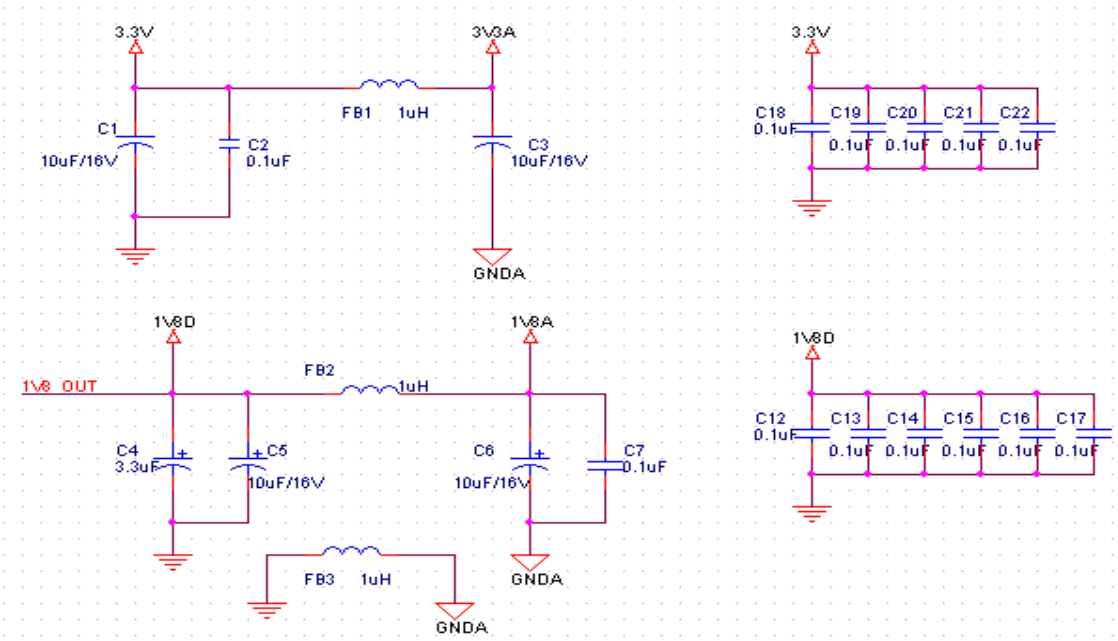

Fig 2. Power Design

Recommend for power design.

1. Locate decoupling capacitor as close as possible to W5300.
2. Use ground plane as wide as possible.
3. If ground plane width is adequate, having a separate analog ground plane and digital ground plane is good practice.

If ground plane is not wide, design analog and digital ground planes as a single ground plane, rather than separate them.

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2. System Memory Map

According to the host interface, W5300 supports direct address mode and indirect address mode.

The direct address mode is that the target host system can directly access W5300 registers after mapping the registers to T.M.S(Target host system Memory-mapped I/O Space).

Direct address mode memory map is composed of Mode register(MR), COMMON registers, and SOCKET registers. Those registers are mapped in T.M.S sequentially increasing by 2bytes from the BA(Base Address) of T.M.S. Using the mapping address, the target host system can directly access MR, COMMON registers and SOCKET registers. To use the direct address mode, total 0x400 bytes are required for memory space.

In indirect address mode, target host system indirectly accesses COMMON registers and SOCKET registers by using IDM_AR(Indirect Mode Address Register) and IDM_DR(Indirect Mode Data Register) which are just only directly mapped in T.M.S together with MR.

Indirect address mode memory map is composed of direct accessible MR, IDM_AR, IDM_DR and indirect accessible COMMON & SOCKET registers. Only MR, IDM_AR and IDM_DR are mapped in T.M.S sequentially increasing by 2Bytes from BA of T.M.S, but COMMON & SOCKET registers are not mapped in T.M.S because those register can be accessed indirectly using IDM_AR & IDM_DR. To use the indirect address mode, just 0x06 bytes are required for memory space.

When target host system access Interrupt register(IR) of COMMON registers at the indirect address mode, it is processed as below:

Host Write : Set IDM_AR to 0x0002, IR address (IDM_AR = 0x0002)
Set IDM_DR to 0xFFFF (IDM_DR = 0xFFFF)
Host Read : Set IDM_AR to 0x0002, IR address (IDM_AR = 0x0002)
Read IDM_DR and save as Value (Value = IDM_DR)

The host interface mode of W5300 is decided according to the value of 'IND' bit (0^{th} bit) of MR.

MR(0) = '0' => Direct address mode
MR(0) = '1' => Indirect address mode

The memory map of each address mode is as below:

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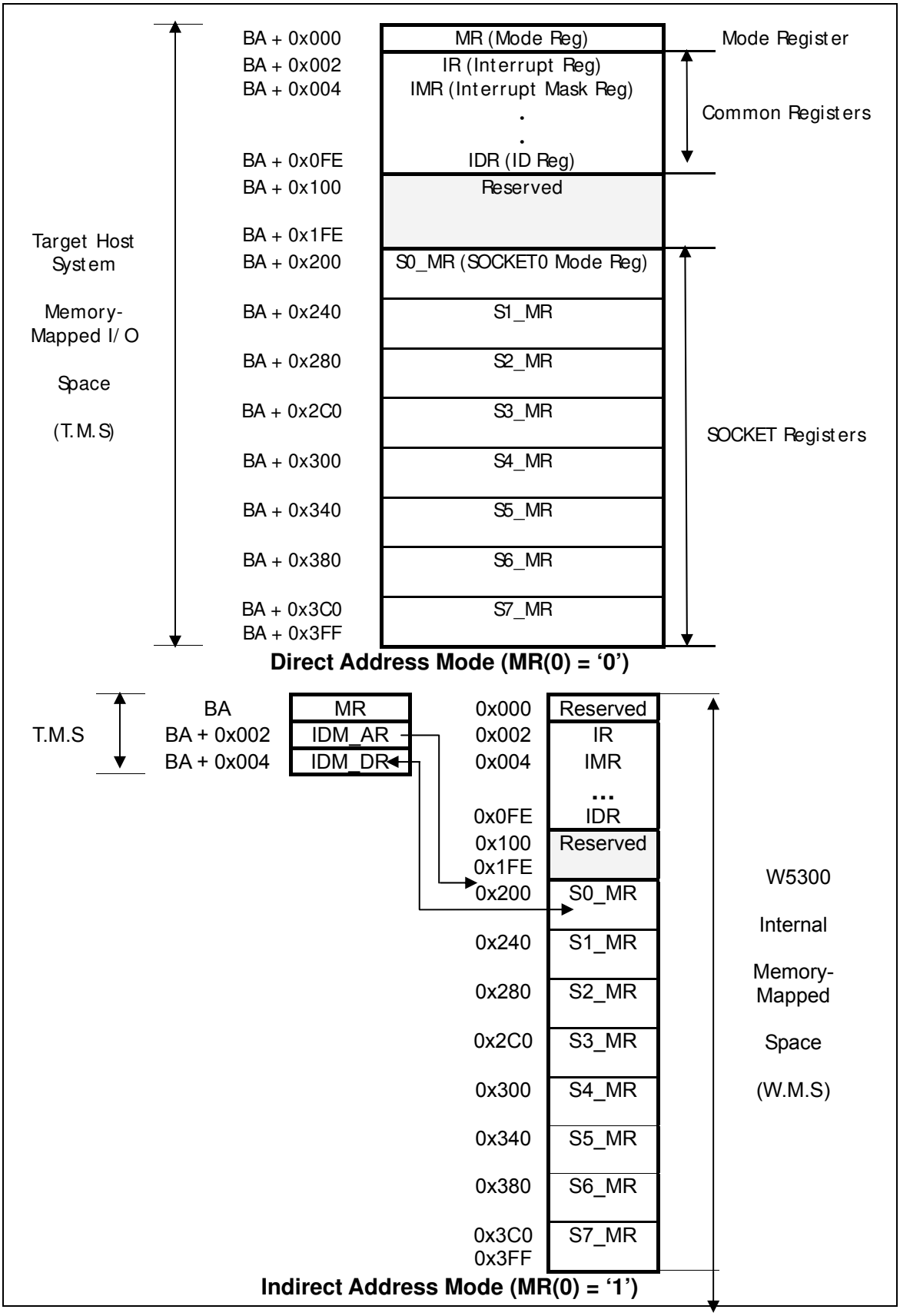

Fig 3. Memory Map

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3. W5300 Registers

W5300 register is composed of MR(to decide direct or indirect address mode), IDM_AR & IDM_DR(only used at the indirect address mode) and COMMON registers and SOCKET registers.

MR, IDM_AR, and IDM_DR register are mapped in T.M.S. COMMON & SOCKET registers are mapped in T.M.S or W.M.S (W5300 internal Memory Space) according to address mode.

All W5300 registers are 1Byte, 2Bytes, 4Bytes or 6Bytes. According to data bus width of target host system, the access is processed – 2bytes address offset at the 16bit data bus and 1 byte address offset at the 8bit data bus.

When mapping W5300 registers in T.M.S, the physical T.M.S address of W5300 register is calculated as below.

Physical Address of W5300 Reg **= Base Address** of T.M.S **+ Address offset** of W5300 Reg

The byte ordering of W5300 registers is big-endian – low address byte is used as the most significant byte.

[Register Notation]

MR : MR register
MR0 : Low address register of MR (Address offset - 0x000), Most significant byte
MR1 : High address register of MR (Address offset – 0x001), Least significant byte
MR(15:5) : 11 bit (from 15th bit to 5th bit of MR register)
MR(0) : 0th bit of MR register, 0th bit of MR1
MR(13) : 13th bit of MR register, 5th bit of MR0
MR0(7) : 15th bit of MR register, Most significant bit of MR0
MR(DWB) : MR의 DWB bit (DWB : Bit Symbol)

SHAR : Source Hardware Address Register
SHAR0 : 1ST address register of SHAR (Address offset – 0x008)
SHAR1 : 2nd address register of SHAR (Address offset – 0x009)
SHAR2 : 3rd address register of SHAR (Address offset – 0x00A)
SHAR3 : 4th address register of SHAR (Address offset – 0x00B)
SHAR4 : 5th Address register of SHAR (Address offset – 0x00C)
SHAR5 : 6th address register of SHAR (Address offset – 0x00D)

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3.1 Mode Register

Address offset		Symbol		Description
16Bit	8Bit	16Bit	8Bit	
0x000	0x000	MR	MR0	Mode Register
	0x001		MR1	

3.2 Indirect Mode Registers

Address offset		Symbol		Description
16Bit	8Bit	16Bit	8Bit	
0x002	0x002	IDM_AR	IDM_AR0	Indirect Mode Address Register
	0x003		IDM_AR1	
0x004	0x004	IDM_DR	IDM_DR0	Indirect Mode Data Register
	0x005		IDM_DR1	

3.3 COMMON registers

Address offset		Symbol		Description
16Bit	8Bit	16Bit	8Bit	
0x002	0x002	IR	IR0	Interrupt Register
	0x003		IR1	
0x004	0x004	IMR	IMR0	Interrupt Mask Register
	0x005		IRM1	
0x006	0x006			Reserved
	0x007			
0x008	0x008	SHAR	SHAR0	Source Hardware Address Register
	0x009		SHAR1	
0x00A	0x00A	SHAR2	SHAR2	
	0x00B		SHAR3	
0x00C	0x00C	SHAR4	SHAR4	
	0x00D		SHAR5	
0x00E	0x00E			Reserved
	0x00F			
0x010	0x010	GAR	GAR0	Gateway Address Register
	0x011		GAR1	
0x12	0x012	GAR2	GAR2	
	0x013		GAR3	

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