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8M × 8 BANKS × 16 BIT DDR3 SDRAM

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1. GENERAL DESCRIPTION

The W631GG6MB is a 1G bits DDR3 SDRAM, organized as 8,388,608 words × 8 banks × 16 bits. This device achieves high speed transfer rates up to 2133 MT/s (DDR3-2133) for various applications. This device is sorted into the following speed grades: -09, -11, -12, -15, 09I, 11I, 12I, 15I, 09J, 11J, 12J and 15J.

The -09 ,09I and 09J speed grades are compliant to the DDR3-2133 (14-14-14) specification (The 09I industrial grade which is guaranteed to support -40°C ≤ T_{CASE} ≤ 95°C, the 09J industrial plus grade which is guaranteed to support -40°C ≤ T_{CASE} ≤ 105°C).

The -11 ,11I and 11J speed grades are compliant to the DDR3-1866 (13-13-13) specification (The 11I industrial grade which is guaranteed to support -40°C ≤ T_{CASE} ≤ 95°C, the 11J industrial plus grade which is guaranteed to support -40°C ≤ T_{CASE} ≤ 105°C).

The -12, 12I and 12J speed grades are compliant to the DDR3-1600 (11-11-11) specification (The 12I industrial grade which is guaranteed to support -40°C ≤ T_{CASE} ≤ 95°C, the 12J industrial plus grade which is guaranteed to support -40°C ≤ T_{CASE} ≤ 105°C).

The -15, 15I and 15J speed grades are compliant to the DDR3-1333 (9-9-9) specification (The 15I industrial grade which is guaranteed to support -40°C ≤ T_{CASE} ≤ 95°C, the 15J industrial plus grade which is guaranteed to support -40°C ≤ T_{CASE} ≤ 105°C).

The W631GG6MB is designed to comply with the following key DDR3 SDRAM features such as posted CAS#, programmable CAS# Write Latency (CWL), ZQ calibration, on die termination and asynchronous reset. All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and CK# falling). All I/Os are synchronized with a differential DQS-DQS# pair in a source synchronous fashion.

2. FEATURES

- Power Supply: V_{DD}, V_{DDQ} = 1.5V ± 0.075V
- Double Data Rate architecture: two data transfers per clock cycle
- Eight internal banks for concurrent operation
- 8 bit prefetch architecture
- CAS Latency: 5, 6, 7, 8, 9, 10, 11, 13 and 14
- Burst length 8 (BL8) and burst chop 4 (BC4) modes: fixed via mode register (MRS) or selectable On-The-Fly (OTF)
- Programmable read burst ordering: interleaved or nibble sequential
- Bi-directional, differential data strobes (DQS and DQS#) are transmitted / received with data
- Edge-aligned with read data and center-aligned with write data
- DLL aligns DQ and DQS transitions with clock
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge, data and data mask are referenced to both edges of a differential data strobe pair (double data rate)
- Posted CAS with programmable additive latency (AL = 0, CL - 1 and CL - 2) for improved command, address and data bus efficiency
- Read Latency = Additive Latency plus CAS Latency (RL = AL + CL)
- Auto-precharge operation for read and write bursts

- Refresh, Self-Refresh, Auto Self-refresh (ASR) and Partial array self refresh (PASR)
- Precharged Power Down and Active Power Down
- Data masks (DM) for write data
- Programmable CAS Write Latency (CWL) per operating frequency
- Write Latency WL = AL + CWL
- Multi purpose register (MPR) for readout a predefined system timing calibration bit sequence
- System level timing calibration support via write leveling and MPR read pattern
- ZQ Calibration for output driver and ODT using external reference resistor to ground
- Asynchronous RESET# pin for Power-up initialization sequence and reset function
- Programmable on-die termination (ODT) for data, data mask and differential strobe pairs
- Dynamic ODT mode for improved signal integrity and preselectable termination impedances during writes
- 2K Byte page size
- Interface: SSTL_15
- Packaged in VFBGA 96 Ball (7.5x13 mm^2 with thickness of 1.0 mm), using lead free materials with RoHS compliant

3. ORDER INFORMATION

PART NUMBER	SPEED GRADE	OPERATING TEMPERATURE
W631GG6MB-09	DDR3-2133 (14-14-14)	0°C ≤ TCASE ≤ 95°C
W631GG6MB09I	DDR3-2133 (14-14-14)	-40°C ≤ TCASE ≤ 95°C
W631GG6MB09J	DDR3-2133 (14-14-14)	-40°C ≤ TCASE ≤ 105°C
W631GG6MB-11	DDR3-1866 (13-13-13)	0°C ≤ TCASE ≤ 95°C
W631GG6MB11I	DDR3-1866 (13-13-13)	-40°C ≤ TCASE ≤ 95°C
W631GG6MB11J	DDR3-1866 (13-13-13)	-40°C ≤ TCASE ≤ 105°C
W631GG6MB-12	DDR3-1600 (11-11-11)	0°C ≤ TCASE ≤ 95°C
W631GG6MB12I	DDR3-1600 (11-11-11)	-40°C ≤ TCASE ≤ 95°C
W631GG6MB12J	DDR3-1600 (11-11-11)	-40°C ≤ TCASE ≤ 105°C
W631GG6MB-15	DDR3-1333 (9-9-9)	0°C ≤ TCASE ≤ 95°C
W631GG6MB15I	DDR3-1333 (9-9-9)	-40°C ≤ TCASE ≤ 95°C
W631GG6MB15J	DDR3-1333 (9-9-9)	-40°C ≤ TCASE ≤ 105°C

4. KEY PARAMETERS

Speed Bin			DDR3-2133		DDR3-1866		DDR3-1600		DDR3-1333		Unit
CL-nRCD-nRP			14-14-14		13-13-13		11-11-11		9-9-9		
Part Number Extension			-09/09I/09J		-11/11I/11J		-12/12I/12J		-15/15I/15J		
Parameter		Sym.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum operating frequency using maximum allowed settings for Sup_CL and Sup_CWL		f_{CKMAX}	–	1066	–	933	–	800	–	667	MHz
Internal read command to first data		t_{AA}	13.09	20	13.91	20	13.75 (13.125)*5	20	13.5 (13.125)*5	20	nS
ACT to internal read or write delay time		t_{RCD}	13.09	–	13.91	–	13.75 (13.125)*5	–	13.5 (13.125)*5	–	nS
PRE command period		t_{RP}	13.09	–	13.91	–	13.75 (13.125)*5	–	13.5 (13.125)*5	–	nS
ACT to ACT or REF command period		t_{RC}	46.09	–	47.91	–	48.75 (48.125)*5	–	49.5 (49.125)*5	–	nS
ACT to PRE command period		t_{RAS}	33	9 * tREFI	34	9 * tREFI	35	9 * tREFI	36	9 * tREFI	nS
CL = 5	CWL = 5	$t_{CK(AVG)}$	3.0	3.3	3.0	3.3	3.0	3.3	3.0	3.3	nS
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	2.5	3.3	nS
CL = 7	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	Reserved		1.875	< 2.5	1.875	< 2.5	nS
CL = 8	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	nS
CL = 9	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	Reserved		1.5	< 1.875	1.5	< 1.875	nS
CL = 10	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	1.5	< 1.875	1.5	< 1.875	1.5	< 1.875	nS
CL = 11	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	Reserved		1.25	< 1.5	Reserved		nS
CL = 13	CWL = 9	$t_{CK(AVG)}$	1.07	< 1.25	1.07	< 1.25	Reserved		Reserved		nS
CL = 14	CWL = 10	$t_{CK(AVG)}$	0.938	< 1.07	Reserved		Reserved		Reserved		nS
Supported CL Settings		Sup_CL	5, 6, 7, 8, 9, 10, 11, 13, 14		5, 6, 8, 10, 13		5, 6, (7), 8, (9), 10, 11		5, 6, (7), 8, 9, 10		nCK
Supported CWL Settings		Sup_CWL	5, 6, 7, 8, 9, 10		5, 6, 7, 9		5, 6, 7, 8		5, 6, 7		nCK
Average periodic refresh Interval	-40°C ≤ TCASE ≤ 85°C	t_{REFI}	–	7.8*2, 3	–	7.8*2, 3	–	7.8*2, 3	–	7.8*2, 3	µS
	0°C ≤ TCASE ≤ 85°C		–	7.8*1	–	7.8*1	–	7.8*1	–	7.8*1	µS
	85°C < TCASE ≤ 95°C		–	3.9*4	–	3.9*4	–	3.9*4	–	3.9*4	µS
	95°C < TCASE ≤ 105°C		–	3.9*4	–	3.9*4	–	3.9*4	–	3.9*4	µS
Operating One Bank Active-Precharge Current		I_{DD0}	–	130	–	115	–	105	–	95	mA
Operating One Bank Active-Read-Precharge Current		I_{DD1}	–	160	–	140	–	130	–	115	mA
Operating Burst Read Current		I_{DD4R}	–	210	–	190	–	180	–	160	mA
Operating Burst Write Current		I_{DD4W}	–	230	–	210	–	190	–	170	mA
Burst Refresh Current		I_{DD5B}	–	170	–	160	–	150	–	140	mA
Normal Temperature Self-Refresh Current		I_{DD6}	–	10	–	10	–	10	–	10	mA
Operating Bank Interleave Current		I_{DD7}	–	270	–	240	–	220	–	200	mA

Notes: (Field value contents in blue font or parentheses are optional AC parameter and CL setting)

1. All speed grades support 0°C ≤ TCASE ≤ 85°C with full JEDEC AC and DC specifications.
2. The -09, -11, -12 and -15 speed grades, -40°C ≤ TCASE < 0°C is not available.
3. The 09I, 09J, 11I, 11J, 12I, 12J, 15I and 15J speed grades support -40°C ≤ TCASE ≤ 85°C with full JEDEC AC and DC specifications.
4. The -09, 09I, -11, 11I, -12, 12I, -15 and 15I speed grades, TCASE is able to extend to 95°C. The 09J, 11J, 12J and 15J speed grades, TCASE is able to extend to 105°C. They are with doubling Auto Refresh commands in frequency to a 32 mS period (tREFI = 3.9 µS), it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0_b and MR2 A7 = 1_b) or enable the Auto Self-Refresh mode (ASR) (MR2 A6 = 1_b, MR2 A7 is don't care).
5. For devices supporting optional down binning to CL=7 and CL=9, tAA/tRCD/tRP min must be 13.125 nS or lower. SPD settings must be programmed to match. For example, DDR3-1333 (9-9-9) devices supporting down binning to DDR3-1066 (7-7-7) should program 13.125 nS in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). DDR3-1600 (11-11-11) devices supporting down binning to DDR3-1333 (9-9-9) or DDR3-1066 (7-7-7) should program 13.125 nS in SPD bytes for tAAmin (Byte16), tRCDmin (Byte 18), and tRPmin (Byte 20). Once tRP (Byte 20) is programmed to 13.125 nS, tRCmin (Byte 21, 23) also should be programmed accordingly. For example, 49.125nS (tRASmin + tRPmin = 36 nS + 13.125 nS) for DDR3-1333 (9-9-9) and 48.125 nS (tRASmin + tRPmin = 35 nS + 13.125 nS) for DDR3-1600 (11-11-11).

5. BALL CONFIGURATION

1	2	3	4	5	6	7	8	9
VDDQ	DQU5	DQU7		A		DQU4	VDDQ	VSS
VSSQ	VDD	VSS		B		DQSU#	DQU6	VSSQ
VDDQ	DQU3	DQU1		C		DQSU	DQU2	VDDQ
VSSQ	VDDQ	DMU		D		DQU0	VSSQ	VDD
VSS	VSSQ	DQL0		E		DML	VSSQ	VDDQ
VDDQ	DQL2	DQSL		F		DQL1	DQL3	VSSQ
VSSQ	DQL6	DQSL#		G		VDD	VSS	VSSQ
VREFDQ	VDDQ	DQL4		H		DQL7	DQL5	VDDQ
NC	VSS	RAS#		J		CK	VSS	NC
ODT	VDD	CAS#		K		CK#	VDD	CKE
NC	CS#	WE#		L		A10/AP	ZQ	NC
VSS	BA0	BA2		M		NC	VREFCA	VSS
VDD	A3	A0		N		A12/BC#	BA1	VDD
VSS	A5	A2		P		A1	A4	VSS
VDD	A7	A9		R		A11	A6	VDD
VSS	RESET#	NC		T		NC	A8	VSS

6. BALL DESCRIPTION

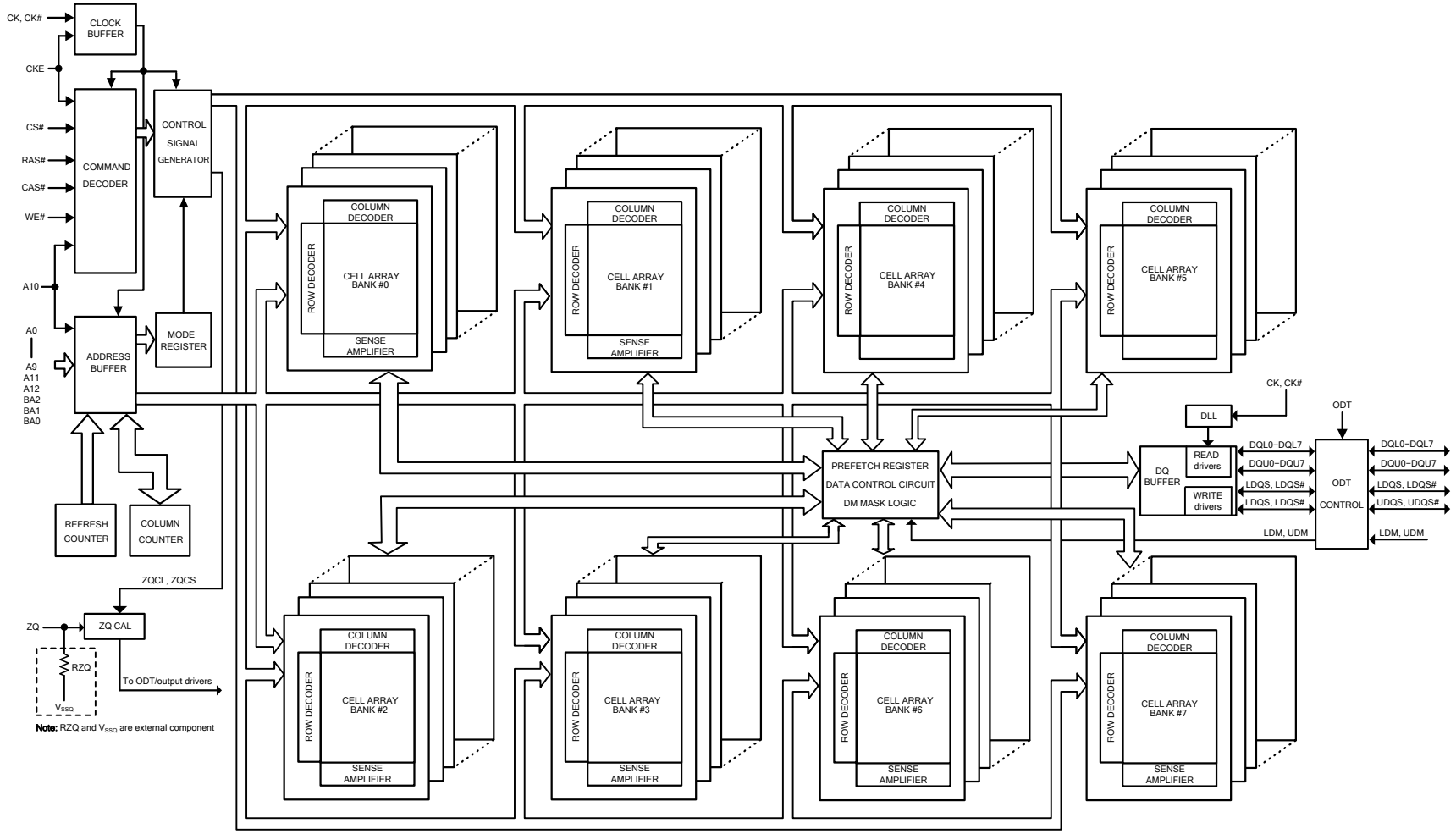
BALL NUMBER	SYMBOL	TYPE	DESCRIPTION
J7, K7	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.
K9	CKE	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power Down and Self-Refresh operation (all banks idle), or Active Power Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After V_{REFCA} and V_{REFDQ} have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK#, ODT and CKE, are disabled during power down. Input buffers, excluding CKE, are disabled during Self-Refresh.
L2	CS#	Input	Chip Select: All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.
K1	ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ, DQSU, DQSU#, DQSL, DQSL#, DMU, and DML signal. The ODT signal will be ignored if Mode Registers MR1 and MR2 are programmed to disable ODT and during Self Refresh.
J3, K3, L3	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
D3, E7	DMU, DML	Input	Input Data Mask: DMU and DML are the input mask signals control the lower or upper bytes for write data. Input data is masked when DMU/DML is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS.
M2, N8, M3	BA0−BA2	Input	Bank Address Inputs: BA0−BA2 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
N3, P7, P3, N2, P8, P2, R8, R2, T8, R3, L7, R7, N7	A0−A12	Input	Address Inputs: Provide the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC# have additional functions; see below). The address inputs also provide the op-code during Mode Register Set command. Row address: A0−A12. Column address: A0−A9.
L7	A10/AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Auto-precharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Auto-precharge; LOW: no Auto-precharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
N7	A12/BC#	Input	Burst Chop: A12/BC# is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See section 9.1 **"Command Truth Table"** on page 94 for details.
T2	RESET#	Input	Active Low Asynchronous Reset: Reset is active when RESET# is LOW, and inactive when RESET# is HIGH. RESET# must be HIGH during normal operation. RESET# is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD}, RESET# active is destructive to data contents.

E3, F7, F2, F8, H3, H8, G2, H7	DQL0−DQL7	Input/Output	Data Input/Output: Lower byte of Bi-directional data bus.
D7, C3, C8, C2, A7, A2, B8, A3	DQU0−DQU7	Input/Output	Data Input/Output: Upper byte of Bi-directional data bus.
F3, G3	DQSL, DQSL#	Input/Output	Lower byte data Strobe: Data Strobe output with read data, input with write data of DQL[7:0]. Edge-aligned with read data, centered in write data. DQSL is paired with DQSL# to provide differential pair signaling to the system during read and write data transfer. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
C7, B7	DQSU, DQSU#	Input/Output	Upper byte data Strobe: Data Strobe output with read data, input with write data of DQU[7:0]. Edge-aligned with read data, centered in write data. DQSU is paired with DQSU# to provide differential pair signaling to the system during read and write data transfer. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
B2, D9, G7, K2, K8, N1, N9, R1, R9	VDD	Supply	Power Supply: 1.5V ± 0.075V.
A9, B3, E1, G8, J2, J8, M1, M9, P1, P9, T1, T9	VSS	Supply	Ground.
A1, A8, C1, C9, D2, E9, F1, H2, H9	VDDQ	Supply	DQ Power Supply: 1.5V ± 0.075V.
B1, B9, D1, D8, E2, E8, F9, G1, G9	VSSQ	Supply	DQ Ground.
H1	VREFDQ	Supply	Reference voltage for DQ.
M8	VREFCA	Supply	Reference voltage for Control, Command and Address inputs.
L8	ZQ	Supply	External reference ball for output drive and On-Die Termination Impedance calibration: This ball needs an external 240 Ω ± 1% external resistor (RZQ), connected from this ball to ground to perform ZQ calibration.
J1, J9, L1, L9, M7, T3, T7	NC		No Connect: No internal electrical connection is present.

Note:

Input only balls (BA0-BA2, A0-A12, RAS#, CAS#, WE#, CS#, CKE, ODT and RESET#) do not supply termination.

7. BLOCK DIAGRAM



NOTE: The cell array configuration is 8192 * 1024 * 16

8. FUNCTIONAL DESCRIPTION

8.1 Basic Functionality

The DDR3 SDRAM is a high-speed dynamic random-access memory internally configured as an eight-bank DRAM. The DDR3 SDRAM uses an 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be activated (BA0-BA2 select the bank; A0-A12 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

8.2 RESET and Initialization Procedure

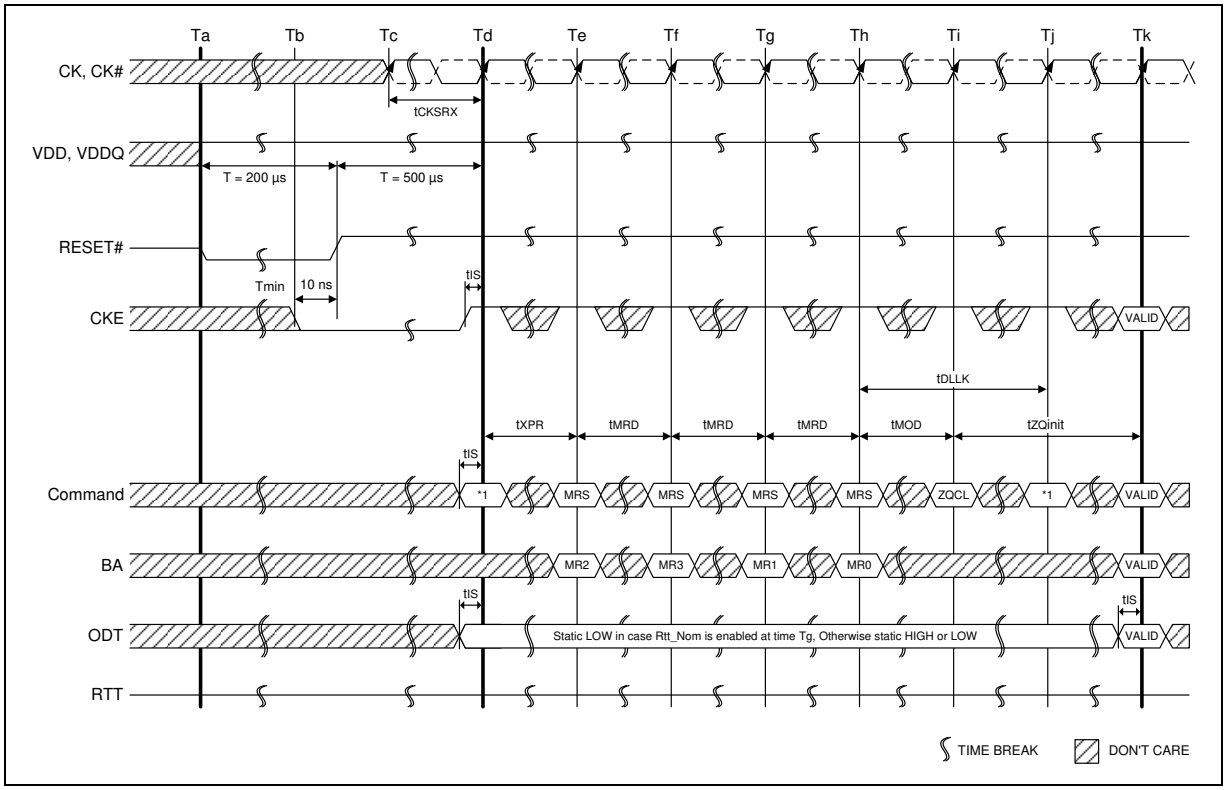
8.2.1 Power-up Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power (RESET# is recommended to be maintained below 0.2 * V_{DD}; all other inputs may be undefined). RESET# needs to be maintained for minimum 200 µS with stable power. CKE is pulled "Low" anytime before RESET# being de-asserted (min. time 10 nS). The power voltage ramp time between 300 mV to V_{DD} min. must be no greater than 200 mS; and during the ramp, $V_{DD} \geq V_{DDQ}$ and (V_{DD} - V_{DDQ}) < 0.3 Volts.
   - V_{DD} and V_{DDQ} are driven from a single power converter output, AND
   - The voltage levels on all pins other than V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side. In addition, V_{TT} is limited to 0.95 V max once power ramp is finished, AND
   - V_{REF} tracks $V_{DDQ}/2$.

   OR
   - Apply V_{DD} without any slope reversal before or at the same time as V_{DDQ}.
   - Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} & V_{REF}.
   - The voltage levels on all pins other than V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side.
2. After RESET# is de-asserted, wait for another 500 µS until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.
3. Clocks (CK, CK#) need to be started and stabilized for at least 10 nS or 5 t_{CK} (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (t_{IS}) must be met. Also, a NOP or Deselect command must be registered (with t_{IS} set up time to clock) before CKE goes active. Once the CKE is registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of t_{DLLK} and t_{ZQinit}.

4. The DDR3 SDRAM keeps its on-die termination in high-impedance state as long as RESET# is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after RESET# deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If Rtt_Nom is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. (tXPR=max (tXS ; 5 * tCK)
6. Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide "Low" to BA0 and BA2, "High" to BA1.)
7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide "Low" to BA2, "High" to BA0 and BA1.)
8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1-BA2).
9. Issue MRS Command to load MR0 with all application settings and "DLL reset". (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-2).
10. Issue ZQCL command to starting ZQ calibration.
11. Wait for both tDLLK and tZQinit completed.
12. The DDR3 SDRAM is now ready for normal operation.



Note:

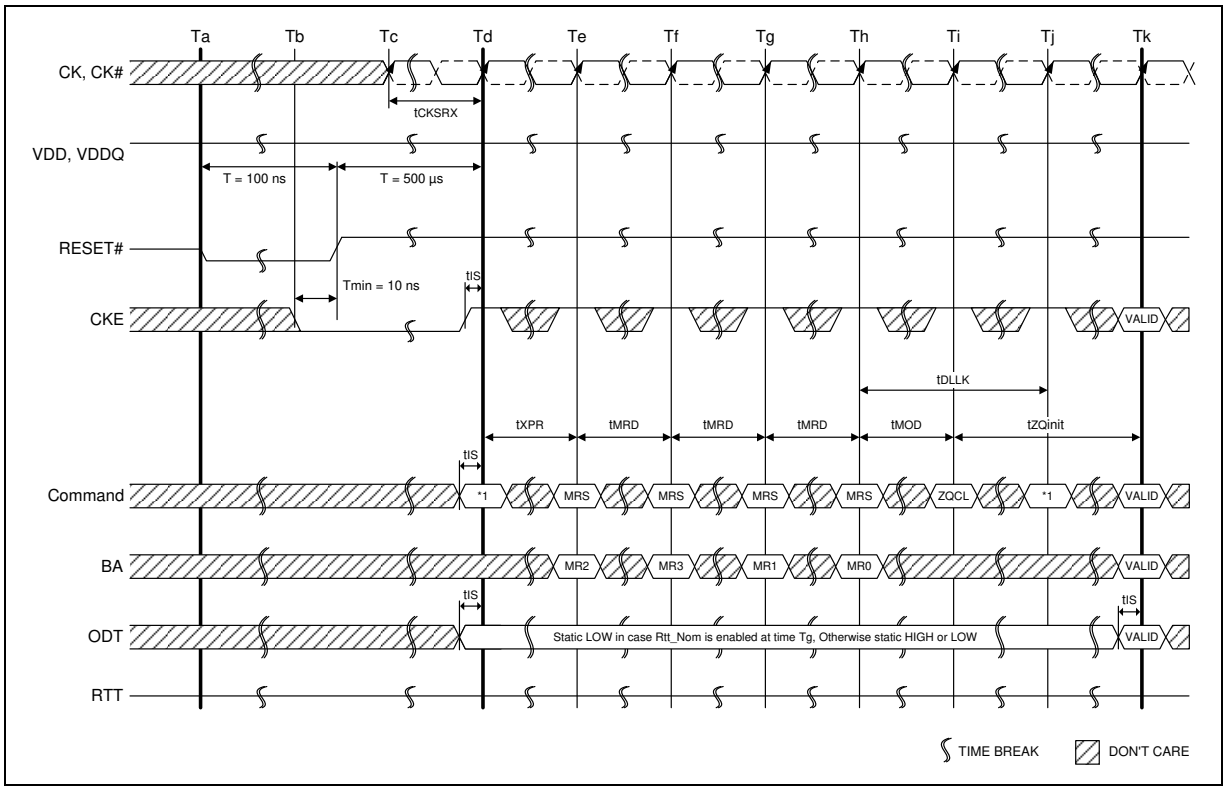
1. From time point "Td" until "Tk" NOP or DES commands must be applied between MRS and ZQCL commands.

Figure 1 – Reset and Initialization Sequence at Power-on Ramping

8.2.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Asserted RESET below 0.2 * VDD anytime when reset is needed (all other inputs may be undefined). RESET needs to be maintained for minimum 100 nS. CKE is pulled “LOW” before RESET being de-asserted (min. time 10 nS).
2. Follow Power-up Initialization Sequence steps 2 to 11.
3. The Reset sequence is now completed; DDR3 SDRAM is ready for normal operation.



Note:

1. From time point “Td” until “Tk” NOP or DES commands must be applied between MRS and ZQCL commands.

Figure 2 – Reset Procedure at Power Stable Condition

8.3 Programming the Mode Registers

For application flexibility, various functions, features, and modes are programmable in four Mode Registers, provided by the DDR3 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers (MR#) are not defined, contents of Mode Registers must be fully initialized and/or re-initialized, i.e., written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which mean these commands can be executed any time after power-up without affecting the array contents.

The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown in Figure 3.

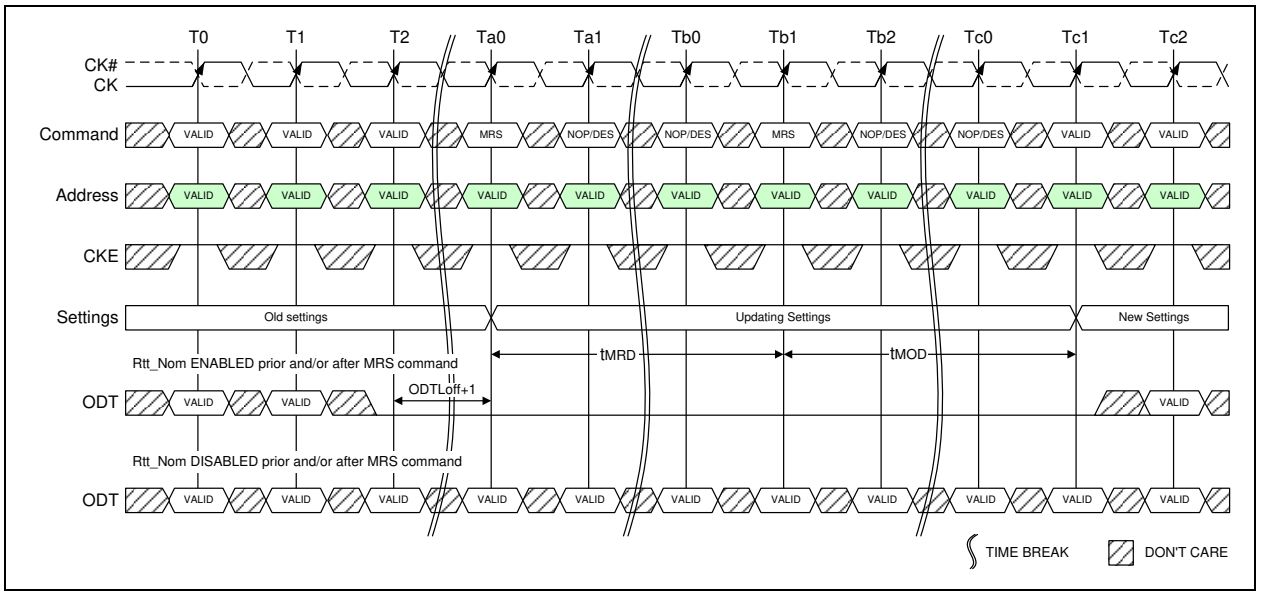


Figure 3 – tMRD Timing

The MRS command to Non-MRS command delay, tMOD is required for the DRAM to update the features, except DLL reset, and is the minimum time required from a MRS command to a non-MRS command excluding NOP and DES shown in Figure 4.

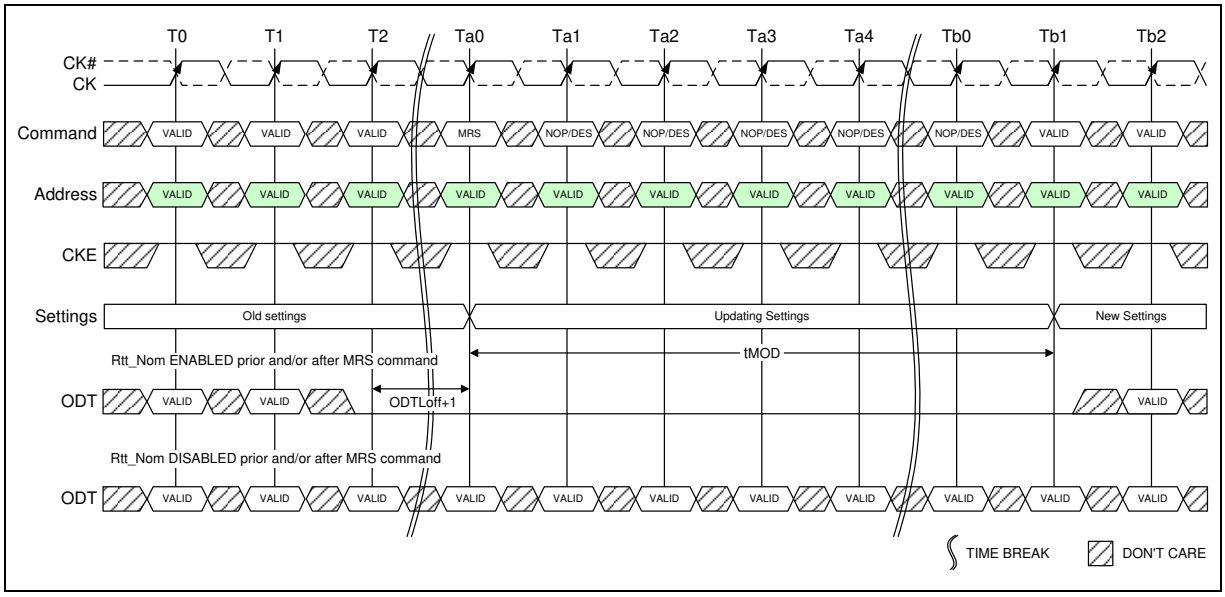
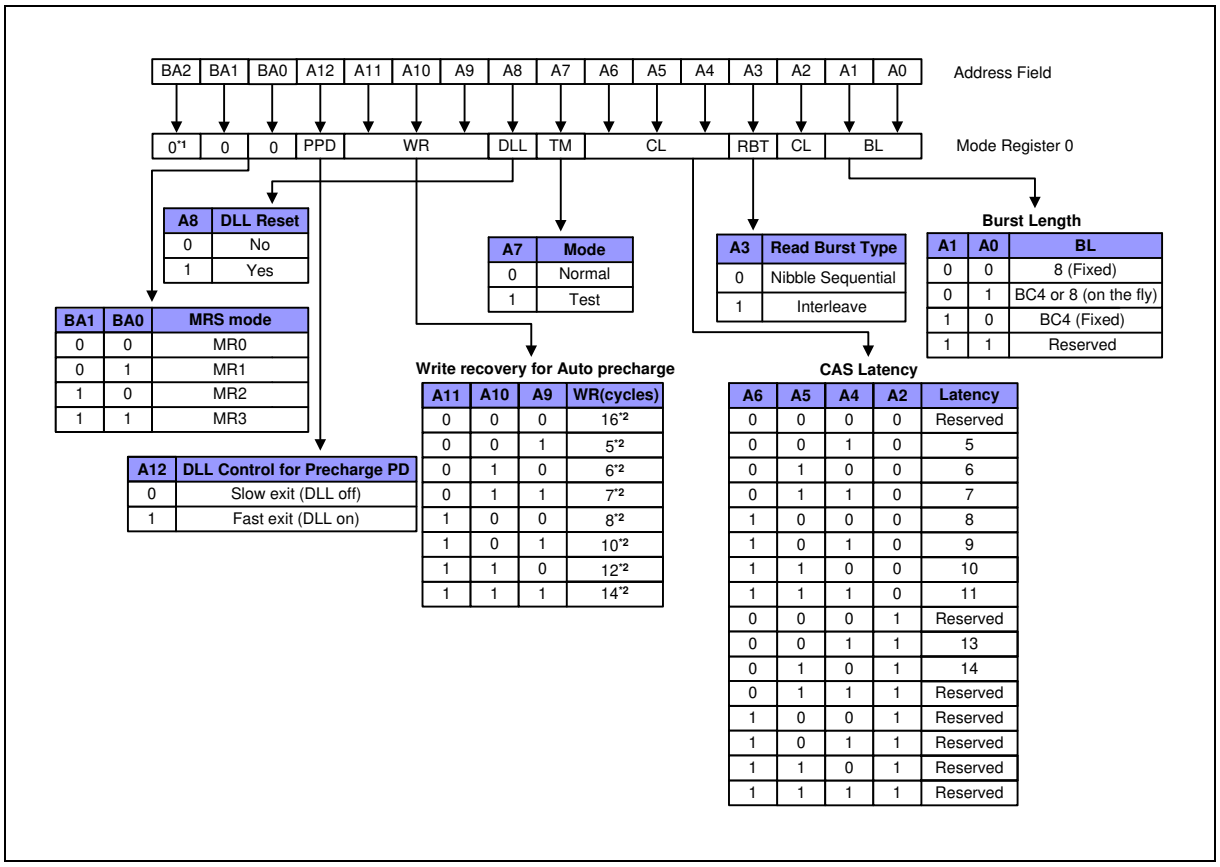


Figure 4 – tMOD Timing

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e., all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. If the Rtt_Nom Feature is enabled in the Mode Register prior and/or after a MRS command, the ODT signal must continuously be registered LOW ensuring RTT is in an off state prior to the MRS command. The ODT signal may be registered high after tMOD has expired. If the Rtt_Nom feature is disabled in the Mode Register prior and after a MRS command, the ODT signal can be registered either LOW or HIGH before, during and after the MRS command. The mode registers are divided into various fields depending on the functionality and/or modes.

8.3.1 Mode Register MR0

The mode register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR and DLL control for precharge Power Down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on CS#, RAS#, CAS#, WE#, BA0, BA1 and BA2, while controlling the states of address pins according to the Figure 5 below.



Notes:

1. BA2 is reserved for future use and must be programmed to "0" during MRS.
2. WR (write recovery for Auto precharge)min in clock cycles is calculated by dividing t_{WR} (in nS) by t_{CK} (in nS) and rounding up to the next integer: WRmin[cycles] = Roundup(t_{WR}[nS] / $t_{CK(avg)}$[nS]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with t_{RP} to determine t_{DAL}.
3. The table only shows the encodings for a given CAS Latency. For actual supported CAS Latency, please refer to **"Speed Bins"** tables for each frequency.
4. The table only shows the encodings for Write Recovery. For actual Write recovery timing, please refer to AC timing table.

Figure 5 – MR0 Definition

8.3.1.1 Burst Length, Type and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 as shown in Figure 5. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in Table 1. The burst length is defined by bits A0-A1. Burst length options include fixed BC4, fixed BL8 and 'on the fly' which allows BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC#.

Table 1 – Burst Type and Burst Order

Burst Length	READ/ WRITE	Starting Column Address (A2, A1, A0)	Burst type = Sequential (decimal) A3 = 0	Burst type = Interleaved (decimal) A3 = 1	NOTES
4 Chop	READ	0 0 0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	1, 2, 3
		0 0 1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T	1, 2, 3
		0 1 0	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	1, 2, 3
		0 1 1	3,0,1,2,T,T,T,T	3,2,1,0,T,T,T,T	1, 2, 3
		1 0 0	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	1, 2, 3
		1 0 1	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	1, 2, 3
		1 1 0	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	1, 2, 3
		1 1 1	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	1, 2, 3
	WRITE	0,V,V	0,1,2,3,X,X,X,X	0,1,2,3,X,X,X,X	1, 2, 4, 5
		1,V,V	4,5,6,7,X,X,X,X	4,5,6,7,X,X,X,X	1, 2, 4, 5
8	READ	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2
		0 0 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6	2
		0 1 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5	2
		0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4	2
		1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3	2
		1 0 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2	2
		1 1 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1	2
		1 1 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0	2
	WRITE	V,V,V	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2, 4

Notes:

1. In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC#, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.
2. 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.
3. T: Output driver for data and strobes are in high impedance.
4. V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.
5. X: Don't Care.

8.3.1.2 CAS Latency

The CAS Latency is defined by MR0 (bits A2, A4, A5 and A6) as shown in Figure 5. CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half-clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); RL = AL + CL. For more information on the supported CL and AL settings based on the operating clock frequency, refer to section 10.15 **"Speed Bins"** on page 134. For detailed Read operation refer to section 8.13 **"READ Operation"** on page 43.

8.3.1.3 Test Mode

The normal operating mode is selected by MR0 (bit A7 = 0) and all other bits set to the desired values shown in Figure 5. Programming bit A7 to a '1' places the DDR3 SDRAM into a test mode that is only used by the DRAM Manufacturer and should NOT be used. No operations or functionality is specified if A7 = 1.

8.3.1.4 DLL Reset

The DLL Reset bit is self-clearing, meaning that it returns back to the value of '0' after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time that the DLL reset function is used, t_{DLLK} must be met before any functions that require the DLL can be used (i.e., Read commands or ODT synchronous operations).

8.3.1.5 Write Recovery

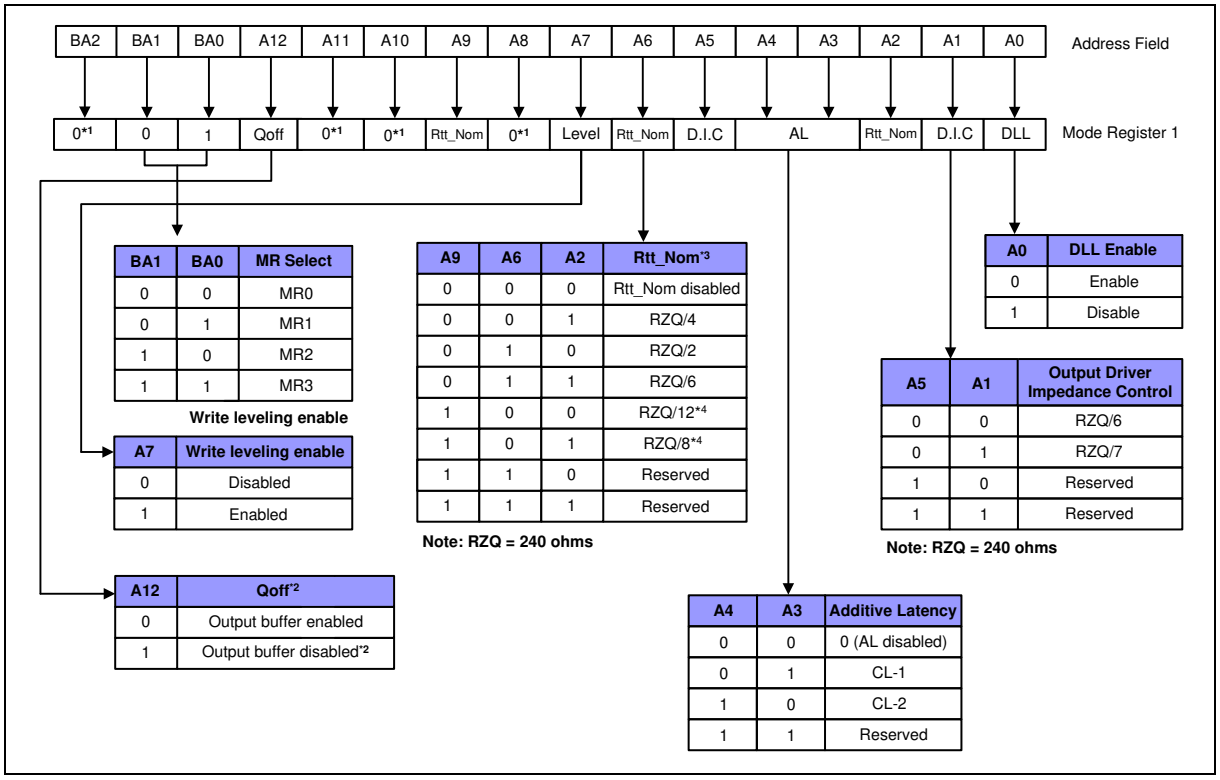
The programmed WR value MR0 (bits A9, A10 and A11) is used for the auto precharge feature along with t_{RP} to determine t_{DAL}. WR (write recovery for auto-precharge) min in clock cycles is calculated by dividing t_{WR} (in nS) by $t_{CK(avg)}$ (in nS) and rounding up to the next integer: WRmin[cycles] = Roundup(t_{WR}[nS]/$t_{CK(avg)}$[nS]). The WR must be programmed to be equal to or larger than t_{WR}(min).

8.3.1.6 Precharge PD DLL

MR0 (bit A12) is used to select the DLL usage during precharge power down mode. When MR0 (A12 = 0), or 'slow-exit', the DLL is frozen after entering precharge power down (for potential power savings) and upon exit requires t_{XPDLL} to be met prior to the next valid command. When MR0 (A12 = 1), or 'fast-exit', the DLL is maintained after entering precharge power down and upon exiting power down requires t_{XP} to be met prior to the next valid command.

8.3.2 Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, Rtt_Nom impedance, additive latency, Write leveling enable and Qoff. The Mode Register 1 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA0 and low on BA1 and BA2, while controlling the states of address pins according to the Figure 6 below.



Notes:

1. BA2, A8, A10 and A11 are reserved for future use and must be programmed to "0" during MRS.
2. Outputs disabled - DQs, DQSs, DQS#s.
3. In Write leveling Mode (MR1 A[7] = 1) with MR1 A[12]=1, all Rtt_Nom settings are allowed; in Write Leveling Mode (MR1 A[7] = 1) with MR1 A[12]=0, only Rtt_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.
4. If Rtt_Nom is used during Writes, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.

Figure 6 – MR1 Definition

8.3.2.1 DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1 (A0 = 0), the DLL is automatically disabled when entering Self Refresh operation and is automatically re-enabled upon exit of Self Refresh operation. Any time the DLL is enabled and subsequently reset, t_{DLLK} clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the t_{DQSCK}, t_{AON} or t_{AOF} parameters. During t_{DLLK}, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, except when Rtt_WR is enabled and the DLL is required for proper ODT operation. For more detailed information on DLL Disable operation refer to section 8.6 **"DLL-off Mode"** on page 25.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the Rtt_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2 {A10, A9} = {0,0}, to disable Dynamic ODT externally.

8.3.2.2 Output Driver Impedance Control

The output driver impedance of the DDR3 SDRAM device is selected by MR1 (bits A1 and A5) as shown in Figure 6.

8.3.2.3 ODT RTT Values

DDR3 SDRAM is capable of providing two different termination values (Rtt_Nom and Rtt_WR). The nominal termination value Rtt_Nom is programmed in MR1. A separate value (Rtt_WR) may be programmed in MR2 to enable a unique RTT value when ODT is enabled during writes. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.

8.3.2.4 Additive Latency (AL)

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. In this operation, the DDR3 SDRAM allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings. A summary of the AL register options are shown in Table 2.

Table 2 – Additive Latency (AL) Settings

A4	A3	AL
0	0	0 (AL Disabled)
0	1	CL - 1
1	0	CL - 2
1	1	Reserved

Note:

AL has a value of CL - 1 or CL - 2 as per the CL values programmed in the MR0 register.

8.3.2.5 Write leveling

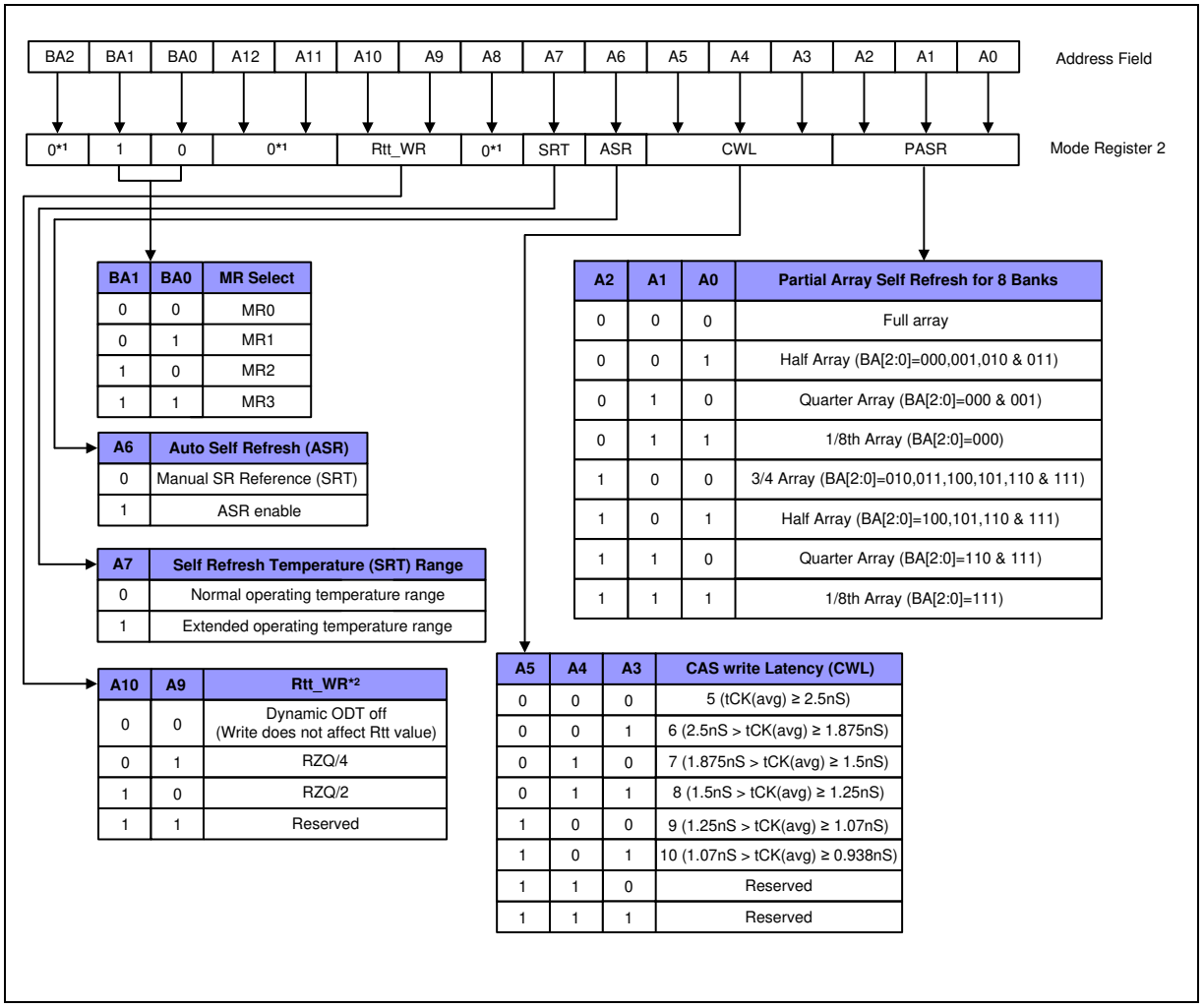
For better signal integrity, DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has the benefit of reducing the number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the controller to maintain t_{DQSS}, t_{DSS}, and t_{DSH} specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew. See section 8.9 **"Write Leveling"** on page 30 for more details.

8.3.2.6 Output Disable

The DDR3 SDRAM outputs may be enabled/disabled by MR1 (bit A12) as shown in Figure 6. When this feature is enabled (A12 = 1), all output pins (DQs, DQS, DQS#, etc.) are disconnected from the device, thus removing any loading of the output drivers. This feature may be useful when measuring module power, for example. For normal operation, A12 should be set to '0'.

8.3.3 Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, Rtt_WR impedance, and CAS write latency. The Mode Register 2 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and low on BA0 and BA2, while controlling the states of address pins according to the Figure 7 below.



BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A6	Auto Self Refresh (ASR)
0	Manual SR Reference (SRT)
1	ASR enable

A7	Self Refresh Temperature (SRT) Range
0	Normal operating temperature range
1	Extended operating temperature range

A10	A9	Rtt_WR*2
0	0	Dynamic ODT off (Write does not affect Rtt value)
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

A2	A1	A0	Partial Array Self Refresh for 8 Banks
0	0	0	Full array
0	0	1	Half Array (BA[2:0]=000,001,010 & 011)
0	1	0	Quarter Array (BA[2:0]=000 & 001)
0	1	1	1/8th Array (BA[2:0]=000)
1	0	0	3/4 Array (BA[2:0]=010,011,100,101,110 & 111)
1	0	1	Half Array (BA[2:0]=100,101,110 & 111)
1	1	0	Quarter Array (BA[2:0]=110 & 111)
1	1	1	1/8th Array (BA[2:0]=111)

A5	A4	A3	CAS write Latency (CWL)
0	0	0	5 (tCK(avg) ≥ 2.5nS)
0	0	1	6 (2.5nS > tCK(avg) ≥ 1.875nS)
0	1	0	7 (1.875nS > tCK(avg) ≥ 1.5nS)
0	1	1	8 (1.5nS > tCK(avg) ≥ 1.25nS)
1	0	0	9 (1.25nS > tCK(avg) ≥ 1.07nS)
1	0	1	10 (1.07nS > tCK(avg) ≥ 0.938nS)
1	1	0	Reserved
1	1	1	Reserved

Notes:

1. BA2, A8, A11~A12 are reserved for future use and must be programmed to “0” during MRS.
2. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled. During write leveling, Dynamic ODT is not available.

Figure 7 – MR2 Definition

8.3.3.1 Partial Array Self Refresh (PASR)

If PASR (Partial Array Self Refresh) is enabled, data located in areas of the array beyond the specified address range shown in Figure 7 will be lost if Self Refresh is entered. Data integrity will be maintained if tREFI conditions are met and no Self Refresh command is issued.

8.3.3.2 CAS Write Latency (CWL)

The CAS Write Latency is defined by MR2 (bits A3-A5), as shown in Figure 7. CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data.

DDR3 SDRAM does not support any half-clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); WL = AL + CWL. For more information on the supported CWL and AL settings based on the operating clock frequency, refer to section 10.15 **"Speed Bins"** on page 134. For detailed Write operation refer to section 8.14 **"WRITE Operation"** on page 56.

8.3.3.3 Auto Self Refresh (ASR) and Self Refresh Temperature (SRT)

DDR3 SDRAM must support Self Refresh operation at all supported temperatures. Applications requiring Self Refresh operation in the Extended Temperature Range must use the ASR function or program the SRT bit appropriately.

When ASR enabled, DDR3 SDRAM automatically provides Self Refresh power management functions for all supported operating temperature values. If not enabled, the SRT bit must be programmed to indicate TOPER during subsequent Self Refresh operation.

ASR = 0, Self Refresh rate is determined by SRT bit A7 in MR2.

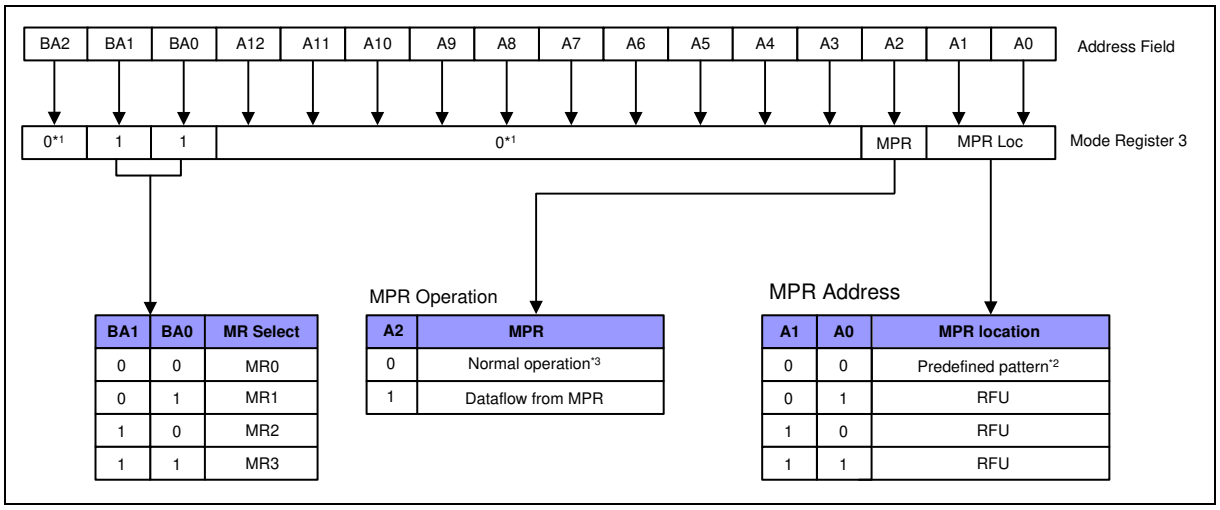
ASR = 1, Self Refresh rate is determined by on-die thermal sensor. SRT bit A7 in MR2 is don't care.

8.3.3.4 Dynamic ODT (Rtt_WR)

DDR3 SDRAM introduces a new feature **"Dynamic ODT"**. In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT settings. In Write leveling mode, only Rtt_Nom is available. For details on Dynamic ODT operation, refer to section 8.19.3 **"Dynamic ODT"** on page 83.

8.3.4 Mode Register MR3

The Mode Register MR3 controls Multi purpose registers. The Mode Register 3 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the Figure 8 below.



BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A2	MPR
0	Normal operation*3
1	Dataflow from MPR

A1	A0	MPR location
0	0	Predefined pattern*2
0	1	RFU
1	0	RFU
1	1	RFU

Notes:

1. BA2, A3~A12 are reserved for future use and must be programmed to "0" during MRS.
2. The predefined pattern will be used for read synchronization.
3. When MPR control is set for normal operation (MR3 A[2] = 0) then MR3 A[1:0] will be ignored.

Figure 8 – MR3 Definition

8.3.4.1 Multi Purpose Register (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and t_{RP} met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Power Down mode, Self Refresh, and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode. For detailed MPR operation refer to section 8.10 **"Multi Purpose Register"** on page 34.

8.4 No OPeration (NOP) Command

The No OPeration (NOP) command is used to instruct the selected DDR3 SDRAM to perform a NOP (CS# LOW and RAS#, CAS#, and WE# HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

8.5 Deselect Command

The DESELECT function (CS# HIGH) prevents new commands from being executed by the DDR3 SDRAM. The DDR3 SDRAM is effectively deselected. Operations already in progress are not affected.

8.6 DLL-off Mode

DDR3 DLL-off mode is entered by setting MR1 bit A0 to "1"; this will disable the DLL for subsequent operations until A0 bit is set back to "0". The MR1 A0 bit for DLL control can be switched either during initialization or later. Refer to section 8.8 **"Input clock frequency change"** on page 28.

The DLL-off Mode operations listed below are an optional feature for DDR3. The maximum clock frequency for DLL-off Mode is specified by the parameter $t_{CK(DLL\_OFF)}$. There is no minimum frequency limit besides the need to satisfy the refresh interval, t_{REFI}.

Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=6 and CWL=6.

DLL-off mode will affect the Read data Clock to Data Strobe relationship (t_{DQSCK}), but not the Data Strobe to Data relationship (t_{DQSQ}, t_{QH}). Special attention is needed to line up Read data to controller time domain.

Comparing with DLL-on mode, where t_{DQSCK} starts from the rising clock edge (AL+CL) cycles after the Read command, the DLL-off mode t_{DQSCK} starts (AL+CL - 1) cycles after the read command. Another difference is that t_{DQSCK} may not be small compared to t_{CK} (it might even be larger than t_{CK}) and the difference between t_{DQSCK} min and t_{DQSCK} max is significantly larger than in DLL-on mode.

The timing relations on DLL-off mode READ operation is shown in the following Timing Diagram (CL=6, BL=8):

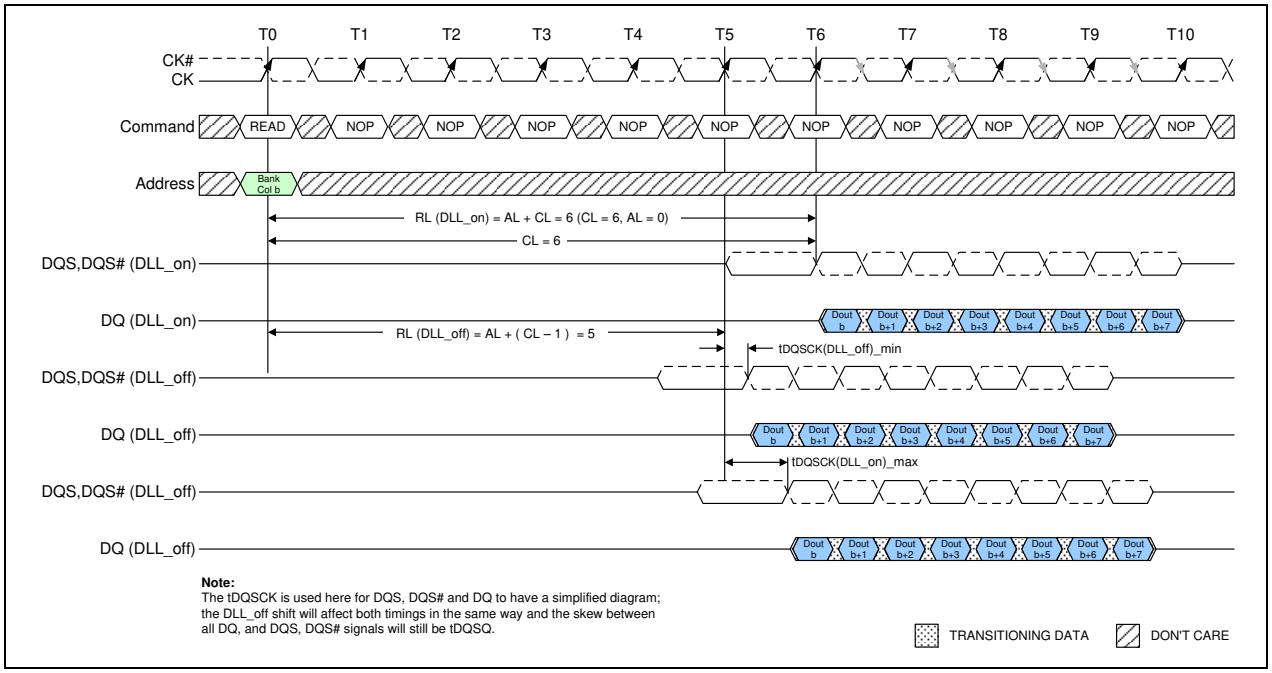


Figure 9 – DLL-off mode READ Timing Operation