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W681307 Product Datasheet

USB1.1 CODEC Microprocessor
Control Unit with 32KB Mask ROM
and 4KB RAM.

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AMENDMENT HISTORY

Ver	Date	Filename	Author	Changes (•: modified, √: added, ×: removed)	Reference
1.0	2006/11/22	W681307_Data Sheet_V1.0	MCSu		
1.1	2006/12/02	W681307_Data Sheet_V1.1	MCSu	• Modify register 0x14C4. • Modify Figure 14-2.	W681307_Data Sheet_V1.0
1.2	2006/12/28	W681307_Data Sheet_V1.2	MCSu	• Modify register 0x14E5.	W681307_Data Sheet_V1.1
1.3	2007/07/23	W681307_Data Sheet_V1.3	TYChiu	• Modify endpoint table 18.2.1.	W681307_Data Sheet_V1.2

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1. GENERAL DESCRIPTION

The main product targets for the USB CODEC MCU chip are：

- 27.648MHz four cycle 8032 MCU
- Support external Flash and easy transfer to low cost Mask ROM production
- Universal Serial Bus (USB) v1.1 compliant device controller and PHY, capable of full speed communication (12MHz) with up to 5 configuration end –points
- 8KHz voice sampling rate and 16bits of ADC/DAC
- Support AEC/AGC for on-chip speaker phone support
- Support Keypad function

Winbond MCU chip will be available in the following package

Device	Package	Description
W681307D xxxx	100 pin LQFP	Normal mode, Mask ROM 32K, x2 CLK

2. FEATURES

Micro controller

- Embedded 27.648MHz WINBOND® Turbo 8032 Micro-Controller with 4 Clocks per Machine Cycle
- 4K system RAM, 32K MASK ROM
- Core 1.9V, I/O 3.3V
- Power on Reset circuit
- Software Power Down mode
- In system Programming (ISP) for 29/39/49 series flash ROM
- Built-in Keypad Scan, Watchdog, Wait State

Speech Processor/Interface

- 4 Processor Channels
- Programmable input/output gain stage
- Programmable Auto Gain Control (AGC) stage
- Programmable Soft Clip gain stage
- Acoustic Echo Cancellation (AEC) with half duplex, absolute/relative mode
- PCM interface for External CODEC or PCM interface
- SNDR output
- Built in DTMF tone generator

PCM CODEC

- One Built-in PCM CODEC
- Analogue input amplifier with Internal programmable gain stage
- Analog output amplifier: Push pull drive, Internal programmable gain stage

USB 1.1

- Universal Serial Bus USB v1.1 compliant device controller and PHY, capable of full speed communication (12MHz) with up to 5 configuration end –points.

UART

- T8032 UART for data transmit application.

PCM Highway

- The 1st PCM Highway has four channels..
- All channels support 8/16 bits pcm format, and IOM2 mode.
- Works in master or slave modes with external CODEC.

W2S

- Support three EEPROM format page modes.
- Support six kinds of W2S bus clocks.

SPI interface

- Works in master or slave modes.

SPI Flash interface

- Works in master with the Winbond SPI interface of series flash.

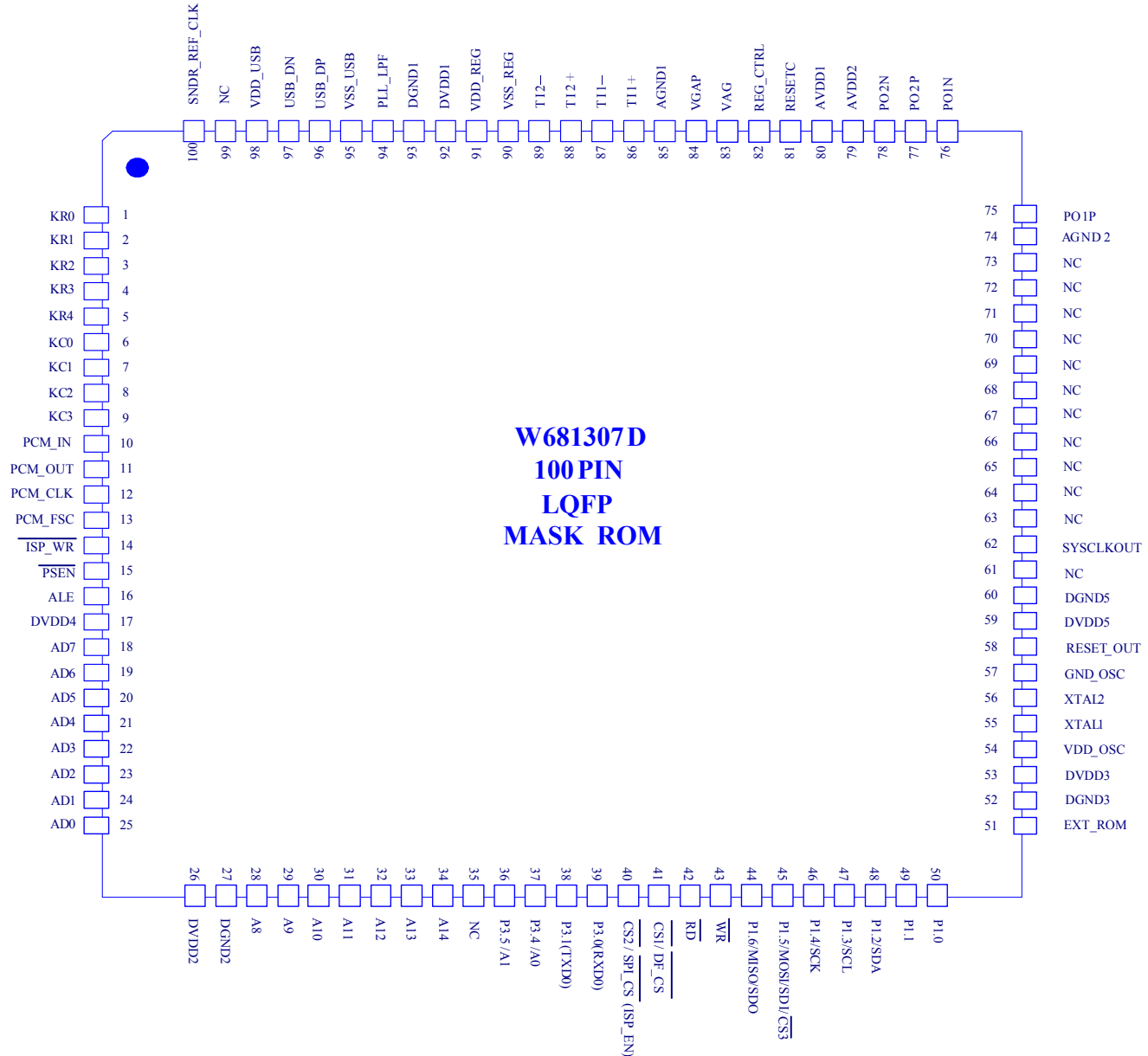
ISP

- In-system-Programming capability with software command via UART or USB interface.

Package

- 100 pin LQFP package

3. PIN CONFIGURATION



4. PINS DESCRIPTION

Pin no.	Pin name	I/O	State during Reset	State after Reset	Pin type section	Function Description	Alternative Function
1	KR0	I/O	Input H	Input H	PC3B01U	Keypad Scan row output	GPIO
2	KR1	I/O	Input H	Input H	PC3B01U	Keypad Scan row output	GPIO
3	KR2	I/O	Input H	Input H	PC3B01U	Keypad Scan row output	GPIO
4	KR3	I/O	Input H	Input H	PC3B01U	Keypad Scan row output	GPIO
5	KR4	I/O	Input H	Input H	PC3B01U	Keypad Scan row output	GPIO
6	KC0	I/O	Input L	Input L	PC3B01D	Keypad Scan column input	GPIO
7	KC1	I/O	Input L	Input L	PC3B01D	Keypad Scan column input	GPIO
8	KC2	I/O	Input L	Input L	PC3B01D	Keypad Scan column input	GPIO
9	KC3	I/O	Input L	Input L	PC3B01D	Keypad Scan column input	GPIO
10	PCM_IN	I/O	**Input H**	**Input H**	**PC3B02U**	PCM high way, Data input	GPIO
11	PCM_OUT	I/O	**Input H**	**Input H**	**PC3B02U**	PCM high way, Data output	GPIO
12	PCM_CLK	I/O	Input L	Input L	**PC3B02D**	PCM high way, Clock In/Output	GPIO
13	PCM_FSC	I/O	Input L	Input L	**PC3B02D**	PCM high way, Frame pluse In/Output	GPIO
14	**$\overline{\text{ISP_ WR}}$**	O	Input H	Input H	PC3B02U	In the normal mode operation, this pin is high. In the in-system-programming (PROG) state, this pin is used for $\overline{\text{WR}}$ function for writing flash memory program.	
15	$\overline{\text{PSEN}}$	O	Input H	Output H	PC3B02U	8032T for Program Memory Strobe Enable	
16	ALE	I/O	Input **H**	Output H	PC3B02U	Output address latch enable (ALE) function	
17	DVDD4	PWR	-	-	PVDDC	Digital supply voltage 4 (for digital I/O pads power)	
18	AD7	I/O	Input H	Input H	PC3B02U	8032T Multiplexed Address/Data pin 7	
19	AD6	I/O	Input H	Input H	PC3B02U	8032T Multiplexed Address/Data pin 6	
20	AD5	I/O	Input H	Input H	PC3B02U	8032T Multiplexed Address/Data pin 5	
21	AD4	I/O	Input H	Input H	PC3B02U	8032T Multiplexed Address/Data pin 4	
22	AD3	I/O	Input H	Input H	PC3B02U	8032T Multiplexed Address/Data pin 3	
23	AD2	I/O	Input H	Input H	PC3B02U	8032T Multiplexed Address/Data pin 2	
24	AD1	I/O	Input H	Input H	PC3B02U	8032T Multiplexed Address/Data pin 1	
25	AD0	I/O	Input H	Input H	PC3B02U	8032T Multiplexed Address/Data pin 0	
26	DVDD2	PWR	-	-	PVDDR	Digital supply voltage 2 (for digital I/O pads power)	
27	DGND2	PWR	-	-	PVSSR	Digital ground 2 (I/O ground)	

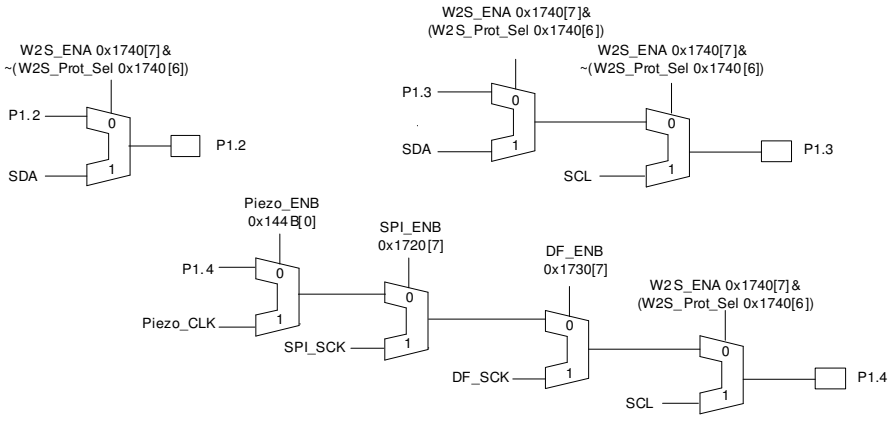
29	A9	I/O	Input H	Output H	PC3B02U	8032T Address Line 9	
30	A10	I/O	Input H	Output H	PC3B02U	8032T Address Line 10	
31	A11	I/O	Input H	Output H	PC3B02U	8032T Address Line 11	
32	A12	I/O	Input H	Output H	PC3B02U	8032T Address Line 12	
33	A13	I/O	Input H	Output H	PC3B02U	8032T Address Line 13	
34	A14	I/O	Input H	Output H	PC3B02U	8032T Address Line 14	
35	NC	I/O	Input H	Output H	PC3B02U	No connection	
36	P3.5 /A1	I/O	Input H	Input H	PC3B02U	Port3 Bit 5 of 8032T	
37	P3.4 /A0	I/O	Input H	Input H	PC3B02U	Port3 Bit 4 of 8032T	
38	P3.1 /TXD0	I/O	Input H	Input H	PC3B02U	Port 3 Bit 1 or TXD serial transmit data port of internal 8032 Turbo	
39	P3.0 /RXD0	I/O	Input H	Input H	PC3B02U	Port 3 Bit 0 or RXD serial receive data port of internal 8032 Turbo	
40	$\overline{CS2}$ / $\overline{SPI_CS}$	**I/O**	**Input H**	**Output H**	**PC3T02**	**External Chip Select**	**General Purpose Output**
41	$\overline{CS1}$ / $\overline{DF_CS}$	**I/O**	**Input H**	**Output H**	**PC3T02**	**External Chip Select**	**General Purpose Output**
42	$\overline{RD}$ /P3.7	I/O	Input H	Input H	PC3B02U	8032T Read Strobe	P3.7 is 8032 I/O
43	$\overline{WR}$ / P3.6	I/O	Input H	Input H	PC3B02U	8032T Write Strobe	P3.6 is 8032 I/O
44	P1.6 /MISO/SDI	I/O	Input H	Input H	PC3B02U	Port 1 Bit 6	SPI function
45	P1.5 /MOSI/SDO / $\overline{CS3}$	I/O	Input H	Input H	PC3B02U	Port 1 Bit 5	SPI function or External Chip Select
46	P1.4 /SCK	I/O	Input H	Input H	PC3B02U	Port 1 Bit 4 or SPI interface clock output	This pin also supports wait state function.
47	P1.3 /SCL	I/O	Input H	Input H	PC3B02U	Port 1 Bit 3 or W2S interface clock output of programming EEPROM.	
48	P1.2 /SDA	I/O	Input H	Input H	PC3B02U	Port 1 Bit 2 or W2S interface serial data of programming EEPROM.	
49	P1.1	I/O	Input H	Input H	PC3B02U	Port 1 Bit 1	
50	P1.0	I/O	Input H	Input H	PC3B02U	Port 1 Bit 0	
51	EXT_ROM	I	Input H	Input	PC3D01U	When set this pin to high then the chip goes into external ROM mode.	
52	DGND3	PWR	-	-	PVSSC	Digital ground 3 (core power ground)	
53	DVDD3	PWR	-	-	PVDDC	Digital supply voltage 3 for core power, which should connect to DVDD1.	
54	VDD_OSC	PWR	-	-	PVDDC	Oscillation circuits supply voltage.	
55	XTAL1	I	Active	Active	PAnalog	13.824Mhz Crystal oscillator output	
56	XTAL2	O	Active	Active	PAnalog	13.824Mhz Crystal oscillator input	
57	GND_OSC	PWR	-	-	PVSSC	Oscillation circuits ground	

58	RESETOUT	O	L	H	PC3o01	Chip reset indication output. Active high after the reset state.
59	DVDD5	PWR	-	-	PVDDC	Digital supply voltage 5 (for digital I/O pads power)
60	DGND5	PWR	-	-	PVSSC	Digital ground 5 (I/O ground)
61	NC	O	Tristate	Tristate	PC3T02	No connection
62	SYSCLKOUT	O	Tristate	L	PC3T02	13.824 MHz system clock output
63	NC	O	Tristate	Tristate	PC3T02	No connection
64	NC	O	Tristate	Tristate	PC3T01	No connection
65	NC	O	Tristate	Tristate	PC3B01	No connection
66	NC	O	Tristate	Tristate	PC3T01	No connection
67	NC	O	Tristate	Tristate	PC3T01	No connection
68	NC	O	Tristate	Tristate	PC3T02	No connection
69	NC	O	Tristate	Tristate	PC3T02	No connection
70	NC	O	Tristate	Tristate	PC3T02	No connection
71	NC	O	Tristate	Tristate	PC3T01	No connection
72	NC	O	Tristate	Tristate	Analog	No connection
73	NC	I	Hi-Z	Hi-Z	Analog	No connection
74	AGND2	PWR	-	-	PVSSC	Analog ground for OP2 output amplifier
75	PO1P	O	Tristate	Tristate	PAnalog	Power amplifier output (non-inverting) - This pin is the non-inverting power amplifier output, which is an inverted version of the signal at PO1N. This pin is capable of driving a 120 Ω load to PO1N at 3V supply power. This pin is D.C. referred to the VAG pin. This pin is tri-state when the chip is in analog CODEC power down mode.
76	PO1N	O	Tristate	Tristate	PAnalog	Power amplifier output (inverting) - This pin is the inverting power amplifier output. This pin is capable of driving a 120 Ω load to PO1P at 3V supply voltage. This pin is D.C. referenced to the VAG pin. The PO1P and PO1N outputs are differential. This pin is tri-state when the chip is in analog CODEC power down mode.
77	PO2P	O	Tristate	Tristate	PAnalog	Power amplifier output (non-inverting) - This pin is the non-inverting power amplifier output, which is an inverted version of the signal at PO2N. This pin is capable of driving a 16 Ω load to PO2N at 3V supply power. This pin is D.C. referred to the VAG pin. This pin is tri-state when the chip is in analog CODEC power down mode.
78	PO2N	O	Tristate	Tristate	PAnalog	Power amplifier output (inverting) - This pin is the inverting power amplifier output. This pin is capable of driving a 16 Ω load to PO2P at 3V supply voltage. This pin is D.C. referenced to the VAG pin. The PO2P and PO2N outputs are differential. This pin is tri-state when the chip is in analog CODEC power down mode.
79	AVDD2	PWR	-	-	PVDDC	Analog supply voltage for OP2 amplifier
80	AVDD1	PWR	-	-	PVDDC	Analog supply voltage
81	RESETC	O	Tristate	Tristate	PAnalog	It should connect a capacitor for internal power on reset circuit.
82	REG_CTRL	O	Active	Active	PAnalog	Output signal of 3V linear regulator to drive the PNP transistor.
83	VAG	O	Tristate	1.5V	PAnalog	Analog reference voltage. This pin possesses the analog virtual ground of internal CODEC circuits.
84	VBGP	O	1. 0V	1.0V	Panalog	The Band gap output voltage. It is 1.0V volt typically.
85	AGND1	PWR	-	-	PVSSC	Analog ground
86	TI1+	I	Hi-Z	Hi-Z	PAnalog	This is the non-inverting input of the transmission operational amplifier TG1.
87	TI1-	I	Hi-Z	Hi-Z	PAnalog	This is the inverting input of the transmission operational amplifier TG1.
88	TI2+	I	Hi-Z	Hi-Z	PAnalog	This is the non-inverting input of the transmission operational amplifier TG2.
89	TI2-	I	Hi-Z	Hi-Z	PAnalog	This is the non-inverting input of the transmission operational amplifier TG2.

90	VSS_REG	PWR	-	-	PVSSC	Ground of 3.0V linear regulator.
91	VDD_REG	PWR	-	-	PVDDC	3.3V input of 3.0V linear regulator.
92	DVDD1	PWR	-	-	PVDDC	1.9V linear regulator output for internal digital core power supply. Connect a large capacitor (>10uF) for output regulation.
93	DGND1	PWR	-	-	PVSSC	Digital ground 1 (core power ground)
94	PLL_LPF	O	Tristate	Tristate	Panalog	Internal 48MHz PLL charge pump output. Put a passive LPF filter in the pin to ground.
95	VSS_USB	PWR	-	-	PVSSC	USB analog front end ground.
96	USB_DP	Analog I/O	Hi-Z	Hi-Z	PAnalog	USB D+ connection. Series termination resistors (22Ω±1%) are required for impedance of USB bus. The USB Spec1.1 states that the impedance of each driver is required to be between 28 and 44Ω. This chip drive output resistance is 8 to 10Ω. Therefore, the 22Ω±1% series resistors are used.
97	USB_DN	Analog I/O	Hi-Z	Hi-Z	PAnalog	USB D- connection. Series termination resistors (22Ω±1%) are required for impedance of USB bus. The USB Spec1.1 states that the impedance of each driver is required to be between 28 and 44Ω. This chip drive output resistance is 8 to 10Ω. Therefore, the 22Ω±1% series resistors are used.
98	VDD_USB	PWR	-	-	PVDDC	USB analog front end supply power. Full speed devices are identified by pulling D+ to 3.3V±0.3 Volts via a 1.5kΩ±5 % resistor. The baseband chip inside has been built in the 1.5kΩ±20% resistor and the default is disconnected to VDD_USB. The
99	NC	I	Input	Input	PC3D21	No connection
100	SNDR	O	Output L	Output L	PC3B02U	Sounder output - This is a control pin to turn on/off the external transistor, which is used to supply the high peak currents that magnetic sounders typically require.

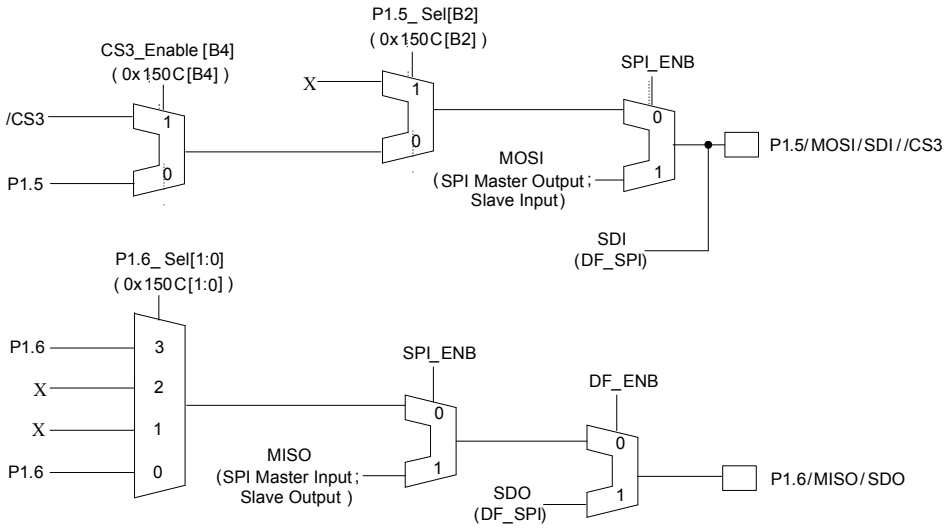
*** When /CS2 is pull low in the initial power on state. Then the chip will enter into the hardware ISP mode to download the system program code via UART or USB ports.**

* P1.2; 、P1.3 and P1.4 multiple functions：

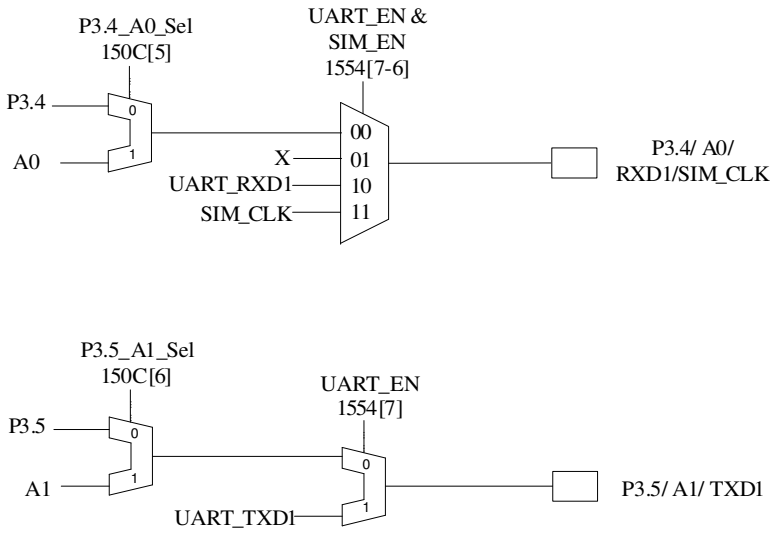


Publication Release Date: May, 2007
Revision 1.3

* P1.5 and P1.6 multiple functions：



* P3.4 and P3.5 multiple functions：

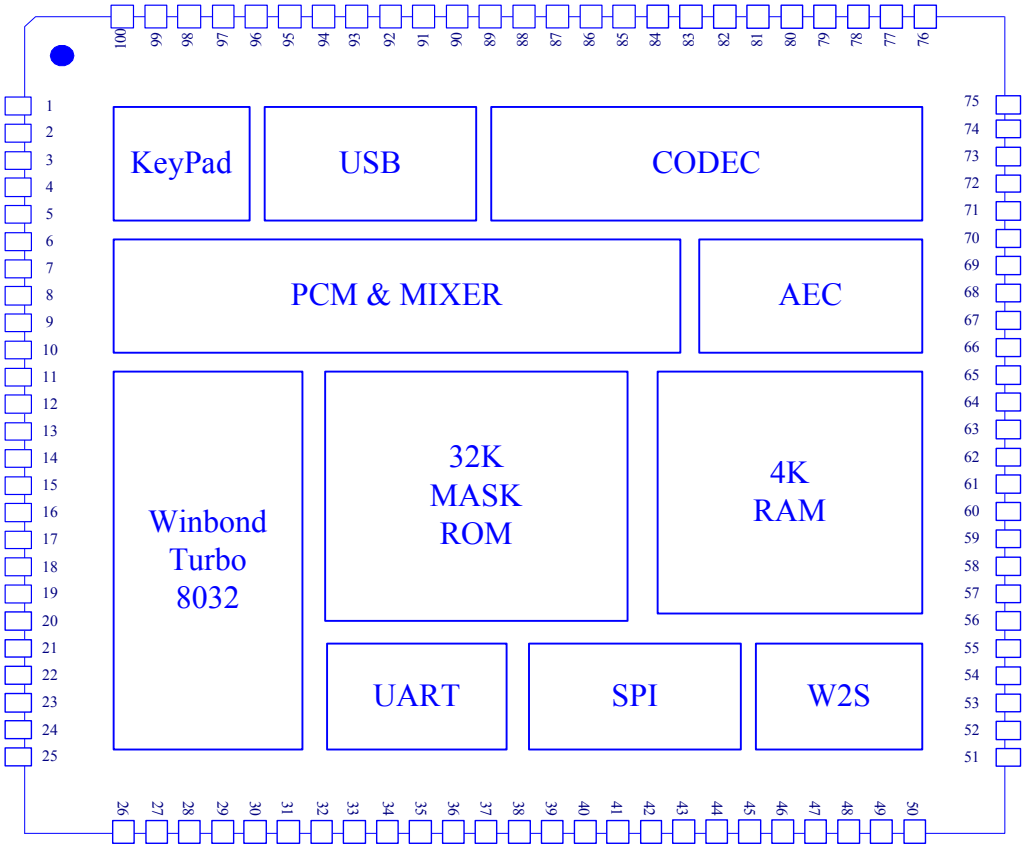


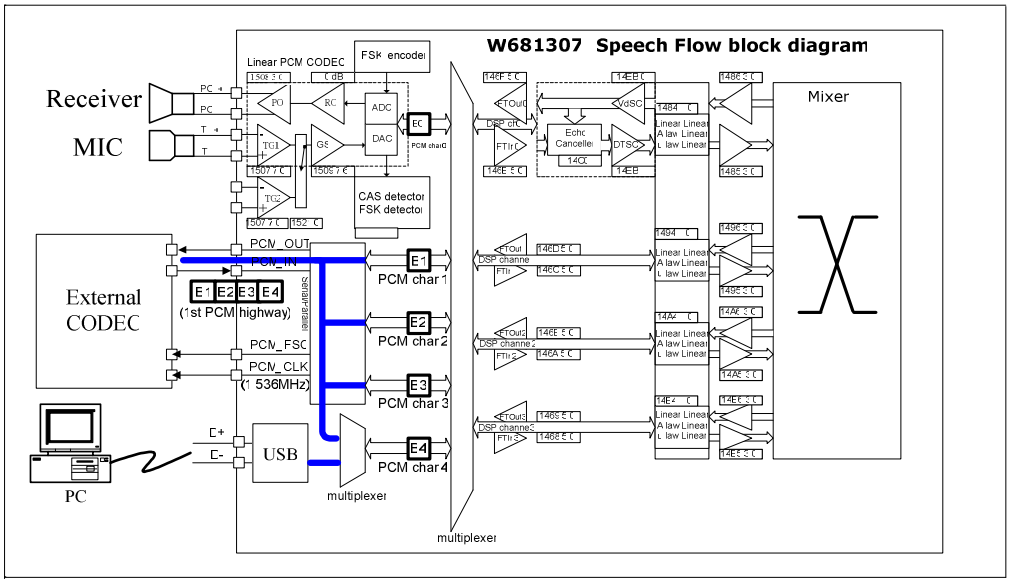
Publication Release Date: May, 2007
Revision 1.3

5. SYSTEM DIAGRAM

5.1 Function Block Diagram

The function block diagrams of the MCU chip and speech interface are shown below：





5.2 I/O Cells in Winbond MCU Chip

Chartered Semiconductor (Artisan) 0.25um Integral I/O cell library

PC3B02U
3V CMOS 3-State I/O Pad with Pull-up Resistor, 2mA

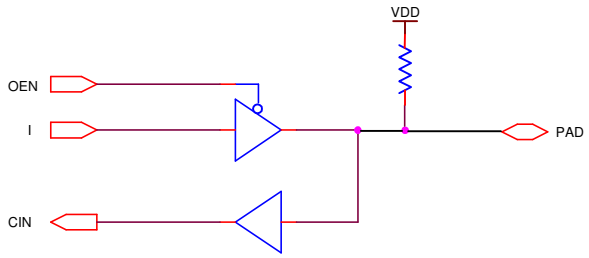


Figure 5-1: PC3B02U pad

PC3B02D
3V CMOS 3-State I/O Pad with Pull-down Resistor, 2mA

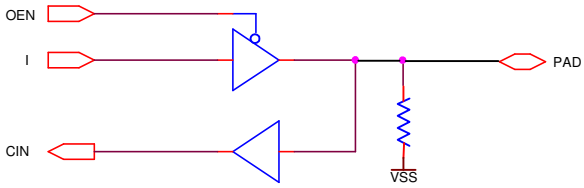


Figure 5-2: PC3B02D pad

PC3o02
3V CMOS Output Pad, 2mA

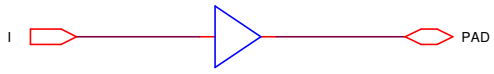


Figure 5-3: PC3o02 pad

PC3D01D
3V CMOS Input only Pad with Pull-down Resistor

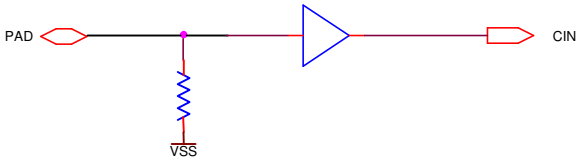


Figure 5-4: PC3D01D pad

PC3D01U
3V CMOS Input only Pad with Pull-up Resistor

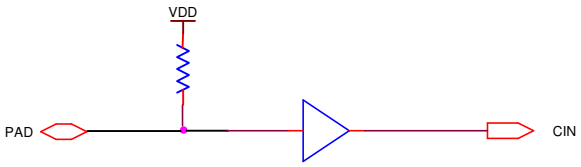


Figure 5-5: PC3D01U pad

PC3D21U
3V CMOS Schmitt non inverting Input only Pad with Pull-up Resistor

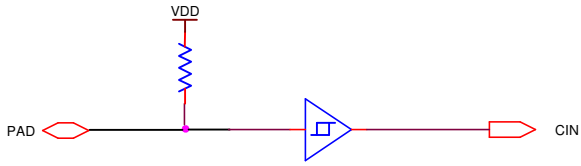


Figure 5-6: PC3D01D pad

PC3T01/02
3V CMOS 3-State Output Pad, 1mA/2mA

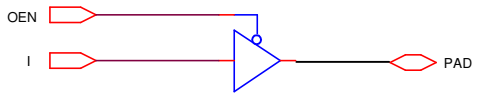


Figure 5-7: PC3T01 pad

6. ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

(Voltage Referenced to AGND pin)

PARAMETER	SYMBOL	RATING	UNIT
Core Power Supply Voltage, pin 53, 92	DVDD	1.9	V
I/O Power Supply Voltage, pin 17, 26, 59	IOVDD	2.7 ~ 3.6	V
Power Supply Voltage , pin 80	AVDD	3.0 ~ 3.6	V
DC Supply Voltage for USB Ouput Stage	VDD_USB	3.0 ~ 3.6	V
Operating Temperature	TOP	-10 to +55	℃
Storage Temperature	TSTG	-85 to +85	℃

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

6.2 DC Characteristics

(AGND = 0 volt TOP = -10 to +55 ℃)

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
Core Operating Current	Icore		-	6	-	mA
I/O Operating Current	II/O		-	6	-	mA
Analog Operating Current	IANA			5		mA
Input High Voltage	VIH	All digital input pins	VDD ×0.7	-	-	V
Input Low Voltage	VIL	All digital input pins	0	-	VDD ×0.3	V
Output High Voltage	VOH	DT, SSP Tx	VDD× 0.75	-	-	V
Output Low Voltage	VOL	DT, SSP Tx	0	-	VDD× 0.25	V
Input High Current	IIL	AGND ≤ Vin ≤ AVDD	-10	-	+10	µA
Input Low Current	IIH	AGND ≤ Vin ≤ AVDD	-10	-	+10	µA
Input Capacitance	CIN	All digital input pins to AGND	-	-	10	pF

6.3 Analog Transmission Characteristics

(AVDD =+3.0V ±5%, AGND = 0 volt , Top = -10 to +55° C ; all analog signal referenced to VAG; 64 Kbps PCM; FST = FSR = 8 KHz; BCLKT = BCLKR = 1.536 MHz; MCLK = 13.824 MHz ; Unless otherwise noted)

6.3.1 Amplitude Response for Analog Transmission Performance

PARAMETER	SYM.	CONDITION	TYP.	A/D		D/A		UNIT
				MIN.	MAX.	MIN.	MAX.	
Absolute Level *	LABS	0 dBm0 = -3.0 dBm @ 600	0.549	---	---	---	---	Vrms
Max. Transmit Level	TXMAX	---	VAG - 1dB	---	---	---	---	Vpk
Frequency Response, Relative to 0 dbm0 @ 1020Hz	GRTV	15 Hz	---	---	---	-60	-0.5	dB
		50 Hz	---	---	---	-40	-0.5	
		100 Hz	---	---	---	-20	-0.5	
		200 Hz	---	---	-3	-5	-0.5	
		300 to 3000 Hz	---	---	-0.20	+0.15	-0.20	
		3300 Hz	---	---	-0.35	+0.15	-0.35	
		3400 Hz	---	---	-0.5	0	-0.5	
		4000 Hz	---	---	---	-12	---	
		4600 to 7000 Hz	---	---	---	-40	---	
Gain Variation vs Level Tone (1020 Hz relative to -10 dBm0)	GLT	+3 to -40 dBm0	---	-0.3	+0.3	-0.2	+0.2	dB
		-40 to -50 dBm0	---	-1.0	+1.0	-0.4	+0.4	
		-50 to -55 dBm0	---	-1.6	+1.6	-0.8	+0.8	

6.3.2 Distortion Characteristics for Analog Transmission Performance

PARAMETER	SYM.	CONDITION	TYP.	TRANSMIT		RECEIVE		UNIT
				MIN.	MAX.	MIN.	MAX.	
Absolute Group Delay	DABS	1600 Hz	---	---	250	---	200	µS
Group Delay Referenced to 1600 Hz	DRTV	500 to 600 Hz	---	---	250	---	30	µS
		600 to 1000 Hz	---	---	200	---	20	
		1000 to 2600 Hz	---	---	70	---	70	
		2600 to 2800 Hz	---	---	100	---	120	
		2800 to 3000 Hz	---	---	145	---	200	
Total Distortion vs. Level Tone (1020 Hz, Mu-Law, C-Message)	DLT	+3 dBm0	---	36	---	34	---	dBC
		0 to -30 dBm0	---	36	---	36	---	
		-40 dBm0	---	29	---	30	---	
		-45 dBm0	---	25	---	25	---	

6.4 Analog Electrical Characteristics

(OP Amplifer TG and VAG; AVDD = +3.0V ±5%, AGND = 0V; Top = -10 to +55° C)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Current of TG		TI1+, TI1- TI2+, TI2-	---	±0.01	±1.0	µA
AC Input Impedance to VAG for TG (1 kHz)	R_{TIIN}	TI1+, TI1- TI2+, TI2-	---	1.0		M
Input Capacitance of TG	C_{TIIN}	TI1+, TI1- TI2+, TI2-	---	---		pF
Input Offset voltage of TG	V_{OFIN}	TI1+, TI1- TI2+, TI2-	---	---	25	mV
Input Common Mode Voltage of TG	V_{CMV}	TI1+, TI1- TI2+, TI2-	0.5	---	AVDD–0.8	V
Input Common Mode Rejection Ratio of TG		TI1+, TI1- TI2+, TI2-		60	100	dB
Gain Bandwidth Product of (10kHz) $R_{load} \geq 10$ K		TI1+, TI1- TI2+, TI2-		975		KHz
DC Open Loop Gain of TG $R_{load} \geq 10$ K		TI1+, TI1- TI2+, TI2-	80	95		dB
Bandgap voltage	V_{BGAP}	Ref to AGND		1.0		V
VAG Output Voltage	V_{VAG}	Ref to AGND		1.5		V
VAG Output Current with less than 50 mV change in output voltage	I_{VAG}	V_{VAG} . 50mV		1		mA
Power Supply Rejection Ratio	PSRR	TG	---	55	---	dB

6.5 Power Drivers – PO1, 2

(AVDD = +3.0V ±5%, AGND = 0V; Top = -10 to +55° C)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Offset Voltage of PO1+ (PO2+) relative to PO1-(PO2-)		Inverted Unity Gain for PO-			30	mV
PO1+(PO2+), PO1-(PO2-) Output Current @ VAG=1.5V, R_L=120, THD<1%		VAG-0.7 V ≤ PO+ ,PO- ≤ VAG+0.7 V		6		mA
PO1+(PO2+), PO1-(PO2-) Output Resistance		Inverted Unity Gain for PO-		10		Ω
Gain Bandwidth Product @ 10 kHz		Open Loop for PO-		433		kHz
Load Capacitance for PO	C_{LAP}	PO- to PO+	---	---	300	pF
Gain of PO1+(PO2+) relative to PO1-(PO2-)				0	0.2	dB
Load Resistance differentially for PO1	R_{LDAP}	PO1- to PO1+	---	120	---	Ω
Load Resistance differentially for PO2	R_{LDAP}	PO2- to PO2+	---	16	---	Ω

6.6 Programmable Output Linear Regulator

Linear Regulator 1 (REG1) T = 25°C, External Transistor PNP: BC807-25

PARAMETERS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Current Consumption during Operation	Idle,		50		uA
Current Consumption during Power off			1		nA
Drop Out Voltage	Iout= 100mA		0.3		V
Input Voltage		3.3		3.6	V
Programmable Output Voltage Range	Iout= 100mA	3.0		3.3	V
Maximum Output Current (PNP)	The characteristics vary with the associated external components (PNP).		250		mA
Load Regulation (PNP)	Vin= 3.3V, Vout=3.0V, Iout= 100mA		50		mV
Line Regulation (PNP)	Vin=3.3V...3.6V, Vout=3.0V, Iout= 100mA		50		dB
REG_CTRL Sink Current	Vin=3.3V, Vout=3.0V*0.95		Tbf		mA
REG_CTRL leakage Current during Power Off	Vin= 3.3V, Vout= tristate			0.1	uA

6.7 USB PHY Electronic Characteristics (25°C, VDD_USB = 3.3V, DVDD1, 3 =1.9V)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage for USB Ouput Stage	VDD_USB		3.0	3.3	3.6	V
Input Voltage Range for USB_DP/DN	USB_DP USB_DN		0	VDD_USB	3.6	V
Input High	V_{IH}		2.0			V
Input Low	V_{IL}				0.8	V
Differential Input Sensitivity	V_{DI}		0.2			V
Differential Common-mode Range	V_{CM}		0.8	---	2.5	V
Single-end Receiver threshold	V_{SE}		0.8		2.0	V
Output Low	V_{OL}				0.3	V
Output High	V_{OH}		2.8			V
Output signal cross Voltage	V_{CRV}		1.3		2.0	V
Pull-up Resistor	R_{UP}		1.2	1.5	1.8	KΩ
Driver Output Resistance	Z_{DRV}		8		12	Ω
Transceiver Capacitance	C_{IN}				20	pF
Driver Rise Time	T_R	C_L = 50pF	4	8	15	ns

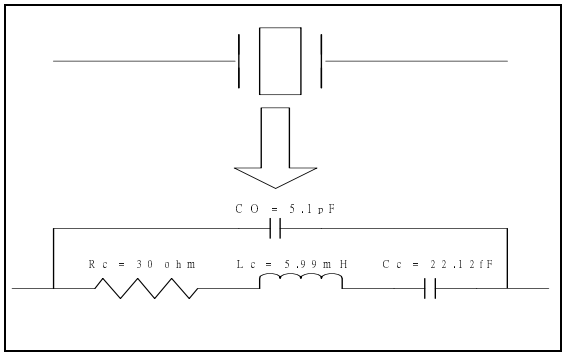
Driver Fall Time	T_F		4	8	15	ns
Rise and Fall Time Matching	T_{LRLF}	$T_{LRLF} = T_{LR}/T_{LF}$	90	100	111	%
VDD_USB Supply Current * (exclude internal pull high resistor)	I_{USB}	Standby			10	nA
		Input Mode			2	mA
		Output Mode			2	mA

6.8 USB PLL Electronic Characteristics (25°C, AVDD = 3.3V, DVDD1, 3 =1.9V)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operation Current	I_{PLL}	VCO_{FREQ} = 96MHz, $FOUT_{FREQ}$ = 48MHz				mA
PLL Shut-Down Current	I_{PLL_DN}					uA
Operation Voltage	V_{PLL}		3.0	3.3	3.6	V
Input Clock Frequency Range	F_{IN}			13.824		MHz
Comparison Frequency	F_{REF}			768		KHz
PLL Output Frequency	F_{OUT}			48		MHz
VCO Frequency	F_{VCO}		---	96	---	MHz
Ouput Duty Cycle			40	50	60	%
PLL Short-Term Peak To Peak Output Jitter	T_{JITTER}					ps
PLL Lock In Time	T_{READY}					ms

6.9 The Crystal Specification Requirement

The below figure is shown the electrical equivalent circuit for a crystal and the parameters are used for the crystal circuit.



6.10 Recommended Crystal Specification

The following crystal specifications are recommended for a proper cooperation between the crystal and baseband crystal oscillator. Correct coordination guarantees great reliability and low failure rates in production.

Parameter	Limit values			Unit	Condition
	Min.	Type.	Max.		
Frequency		13.824		MHz	Fundamental mode
Tolerance of center frequency	-10		+10	ppm	25°C ±3°C
Tolerance over operation range	-5		+5	ppm	0°C to 55°C
Crystal current					
Load capacitance		18		pF	
Dynamic capacitance Cc		22.12		fF	
Resonance resistance Rc		40		Ω	
Electrostatic capacitance		5.1		pF	
Aging			±3	ppm/year	