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nuvoTon

W681308

USB AUDIO CONTROLLER

Data Sheet

Revision 1.2

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1. General Description

W681308 USB Audio Controller from Nuvoton integrates fast 8051 Microcontroller Unit (MCU), Universal Serial Bus (USB) 2.0 Full Speed compliant controller with PHY, 16bit high quality Analog to Digital Converter / Digital to Analog Converter (ADC/DAC) with 8/16/48 KHz wide band sampling rates, speaker phone and echo cancellation, 8 KB One Time Programmable (OTP) program memory and 1 KB data memory in a single 48 pin Low-profile Quad Flat Package (LQFP). MCU includes Joint Test Access Group (JTAG) In-Circuit Emulation(ICE) interface and can handle customer programs such as keypad scan, LCD control, caller list download, and USB and CODEC control among other features. W681308 provides highest integration and low BOM cost solution with 8051-based development platform for USB Audio peripherals and USB VoIP devices such as Skype® , other IM and SIP-based application.

With Nuvoton's market proven CODEC product experience, W681308 is designed to provide high audio quality in VoIP and audio devices applications and deliver USB Audio/VoIP solution with the shortest time to market, time to volume and time to profit

2. Features

8 Bit Turbo MCU

- Embedded 12/24/48 MHz Turbo 8051 MCU with 4 Clocks per machine Cycle
- 1 KB system RAM, 8 KB OTP ROM
- 256 byte internal RAM (8051)
- Power on Reset circuit
- Software Idle mode
- In Circuit Emulation (ICE) through JTAG Interface
-

High Quality 16 bit Mono Audio Linear CODEC

- Built-in 8/16/48 KHz sampling rate wideband mono audio CODEC and true 16-bit resolution ADC/DAC with internal 24-bit audio processing for both record and playback
- Analog microphone(MIC) amplifier and speaker driver with internal programmable gain stage
- 82 dB Receive SNR @ 8 Ohm load

USB 2.0 Full speed (FS) Interface with integrated PHY

- USB 2.0 FS compliant device controller and PHY with 12 Mbps communication speed
- Support 6 USB endpoints configuration: Control, ISO IN/OUT, Bulk IN/OUT and Interrupt IN
- 512-Byte RAM-based USB descriptor for multiple USB device support through 8051 MCU
- Less than 500uA supply current in suspend mode
-
- Fully integrated cap-less microphone amplifier with microphone bias
- Dual earphone / speaker driver and buzzer
- Integrated DAC switch for earphone or speaker phone

Integrated Acoustic Echo Cancellation (AEC)

- Support both half-duplex AEC and 32ms full duplex AEC
- Built-in digital Auto Gain Control (AGC) with microphone input for speaker phone application

Integrated keypad control pins and GPIO

- Suitable for VoIP application
- Volume up and down
- Dial / hang up
- Microphone and speaker phone mute
- LED indicators

- Number pad control
- User programmable keys
- Keypad scanning
- LCD Module interface control

UART

- Programmable UART port for serial data application

PCM Interface

- Master linear PCM interface to external PCM device such as Nuvoton's ProX CODEC/SLIC

SPI interface

- Works in master mode to control Liquid Crystal Display (LCD) Module or other SPI slave devices
- Support Winbond serial flash device with SPI interface

W2S 2 Wire interface

- Support 2 wire interface for EEPROM three format page modes

USB 5V voltage supply

- Built-in linear regulator on chip supports 3.3V to 1.8V conversion for digital core power
- USB 5V to 3.3V supply power using external transistors

Package

- 48-pin LQFP package 7mmx7mmx1mm

Application

- USB audio peripheral box/ USB sound card
- USB microphone / USB mono headset
- Wired and Wireless USB VoIP phone with LCD
- USB VoIP ATA and Gateway
- PSTN and USB VoIP dual phone
- General USB MCU and audio application

3. Pin Configuration

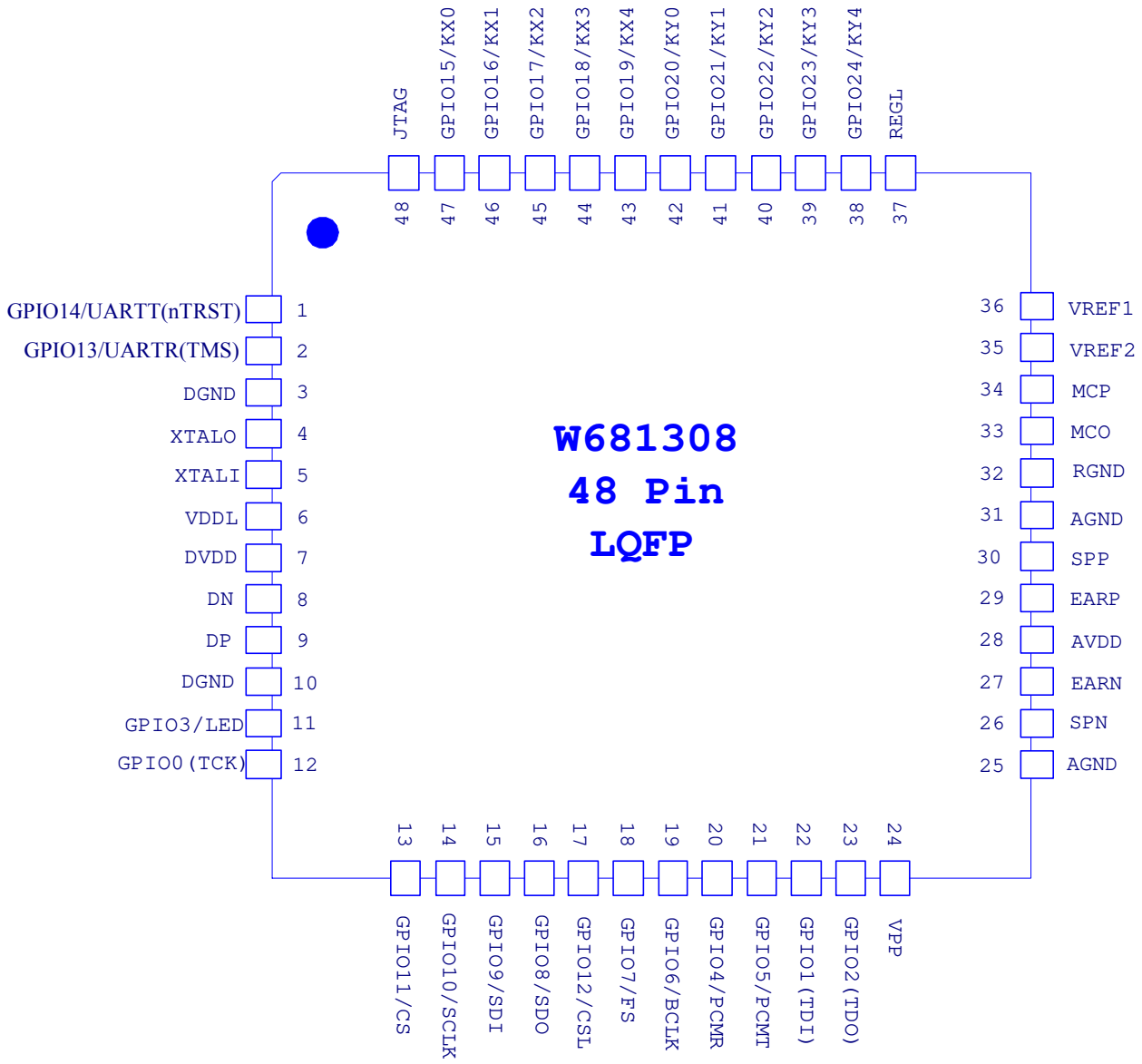


Figure 1 Pin diagram

4. Pin Description

Please refer to Design Guide for product design details.

Pin Name	Pin No	State in Reset	Functionality	Pin Type		Driver Strength
UARTT /nTRST /GPIO 14	1	Pull-H	UART TX data / JTAG TAP controller reset input /GPIO 14	D	I/O	2 mA
UARTR /TMS /GPIO 13	2	Pull-H	UART Rx data / JTAG TMS input / GPIO 13	D	I/O	2 mA
DGND	3		Digital ground supply voltage	D	P	—
XTALO	4		Crystal clock output	A	O	—
XTALI	5		Crystal clock input	A	I	—
VDDL	6		Logic supply voltage	D	P	—
DVDD	7		Digital supply voltage	D	P	—
DN	8		USB D- connection	A	I/O	—
DP	9		USB D+ connection	A	I/O	—
DGND	10		Digital ground supply voltage	D	P	—
LED/GPIO 3	11	Pull-H	LED connection / GPIO 3	D	I/O	16 mA
TCK/GPIO 0	12	Pull-H	JTAG Clock with internal pull up / GPIO 0	D	I/O	16 mA
CS/GPIO 11	13	Pull-H	Chip select (used for SPI flash or normal SPI) /GPIO 11	D	I/O	2 mA
SCLK/GPIO 10	14	Pull-L	Serial port bit clock (For SPI flash or normal SPI) /GPIO 10	D	I/O	2 mA
SDI/GPIO 9	15	Pull-L	Serial port data in (SPI flash/ SPI) /GPIO 9	D	I/O	2 mA
SDO/GPIO 8	16	Pull-H	Serial port data out (SPI flash/ SPI) /GPIO 8	D	I/O	2 mA
CSL/GPIO 12	17	Pull-H	LCD, LCM chip select /GPIO 12	D	I/O	2 mA
FS/GPIO 7	18	Pull-L	PCM Frame Sync output /GPIO 7	D	I/O	2 mA
BCLK/GPIO 6	19	Pull-L	PCM Bit Clock output or input / GPIO 6	D	I/O	2 mA
PCMR/GPIO 4	20	Pull-L	Serial PCM Receive data input / GPIO 4	D	I/O	2 mA
PCMT/GPIO 5	21	Pull-L	Serial PCM Transmit data output / GPIO 5	D	I/O	2 mA
TDI/GPIO 1	22	Pull-H	JTAG Data Input / GPIO 1	D	I/O	2 mA

Pin Name	Pin No	State in Reset	Functionality	Pin Type		Driver Strength
TDO/GPIO 2	23	Pull-L	JTAG Data Output / GPIO 2	D	I/O	2 mA
VPP	24		Reset signal for digital core. Tie this pin to 6.75V for programming the OTP ROM	A	P	—
AGND	25		Analog ground supply voltage	A	P	—
SPN	26		Speaker1 negative connection	A	O	—
EARN	27		Speaker2 negative connection	A	O	—
AVDD	28		Analog supply voltage	A	P	—
EARP	29		Speaker2 positive connection	A	O	—
SPP	30		Speaker1 positive connection	A	O	—
AGND	31		Analog ground supply voltage	A	P	—
RGND	32		Low noise ADC and DAC reference	A	P	—
MCO	33		The microphone amplifier output	A	G	—
MCP	34		Microphone positive connection	A	O	—
VREF2	35		Voltage reference	A	O	—
VREF1	36		Voltage reference	A	O	—
REGL	37		Linear regulator base control output	A	O	—
KY4/GPIO 24	38	Pull-H	Keypad row Y4 connection /GPIO 24	D	I/O	2 mA
KY3/GPIO 23	39	Pull-H	Keypad row Y3 connection /GPIO 23	D	I/O	2 mA
KY2/GPIO 22	40	Pull-H	Keypad row Y2 connection /GPIO 22	D	I/O	2 mA
KY1/GPIO 21	41	Pull-H	Keypad row Y1 connection /GPIO 21	D	I/O	2 mA
KY0/GPIO 20	42	Pull-H	Keypad row Y0 connection /GPIO 20	D	I/O	2 mA
KX4/GPIO 19	43	Pull-L	Keypad column X4 connection /GPIO 19	D	I/O	2 mA
KX3/GPIO 18	44	Pull-L	Keypad column X3 connection /GPIO 18	D	I/O	2 mA
KX2/GPIO 17	45	Pull-L	Keypad column X2 connection /GPIO 17	D	I/O	2 mA
KX1/GPIO 16	46	Pull-L	Keypad column X1 connection /GPIO 16	D	I/O	2 mA
KX0/GPIO 15	47	Pull-L	Keypad column X0 connection /GPIO 15	D	I/O	2 mA
JTAG	48	Pull-L	Tie to DGND for normal operation. Tie to DVDD to enable JTAG function.	D	I	2 mA

Table 1 Pin Description

NOTE: All GPIO pins modes are controlled by register settings.

5. Block Diagram

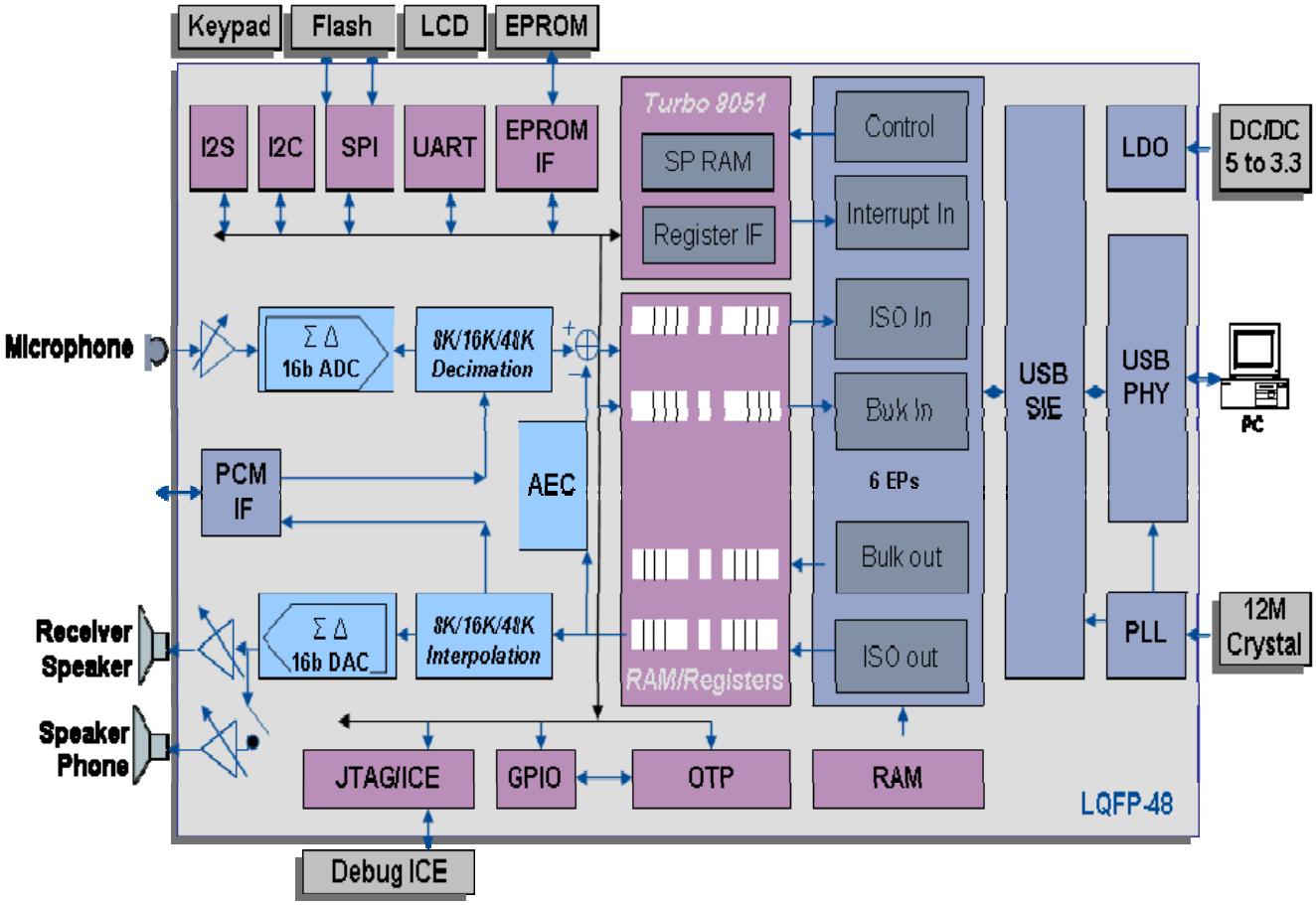


Figure 2 W681308 Function Block Diagram

There are 4 major function block groups in the USB Audio Controller:

- Turbo 8051 MCU, registers, OTP/RAM memory and peripheral ports
- 16-bit audio quality CODEC with AEC/AGC
- USB 2.0 FS interface with SIE, Full Speed PHY and 6 end points
- SPI / UART / I2C / PCM / I2S and GPIO interfaces.

6. Memory Map

6.1 Program Memory map

Memory is mapped into program memory and data memory. Program memory is mapped from 0x0000 to 0x1FFF (8 KB), it is used by internal OTP.

6.2 Data Memory map

Data memory address	Size (Byte)		Function
	Total	Available	
0x1440 ~ 0x1443	4	4	Interrupt Control Registers
0x144A ~ 0x145F	22	20	Keypad IO, LCD, UART and GPIO Control Registers
0x1460 ~ 0x146F	16	16	Gain stage and Mixer Control Registers
0x1470 ~ 0x1474	16	5	PCM Control Registers
0x1480 ~ 0x148A	16	11	CODEC Control Registers
0x14A0 ~ 0x14AF	16	15	SPI Control Registers
0x14B0 ~ 0x14BA	16	11	W2S Control Registers
0x14C0 ~ 0x14C5	16	5	Ring Tone(PWM) Control Registers
0x1600 ~ 0x167F	128	120	Full/Half Duplex AEC Control Registers
0x1680 ~ 0x16FF	128	16	AGC Control Registers
0x1800 ~ 0x19FF	512	57	USB Control Registers
0x2000 ~ 0x23FF	1024	1024	USB RAM Based Descriptor Field
0x2800 ~ 0x2FFF	2048	2048	Full Duplex AEC RAM
0x3000 ~ 0x33FF	1024	1024	System RAM

7. Registers

The registers are mapped by function.

7.1 MCU Clock Rate Select Register

Address	Name	Mode	Value At Reset	Function
0x1440	MCU Rate Select	R/W	0x00	MCU system clock rate selection

7.2 Interrupt Control Registers

Address	Name	Mode	Value At Reset	Function
0x1441	Interrupt Source	R/W	0x00	Enable / Disable Interrupt source
0x1442	Interrupt Enable	R/W	0x00	Enable / Disable Interrupt function
0x1443	Interrupt Priority	R/W	0x00	Set Interrupt priority

7.3 Keypad IO, LCD, UART and GPIO Control Registers

Address	Name	Mode	Value At Reset	Function
0x144A~ 0x144B	GPIO [14:0] Pull Up/Down Control	R/W	0x00	Enable/Disable GPIO [14:0] Pull Up/Down
0x144C~ 0x144F	Keypad I/O (GPIO [24:15]) and GPIO [14:0] Pull Up/Down Selection	R/W	0x00	Select Pull Up/Down for Keypad I/O (GPIO [24:15]) and GPIO [14:0]
0x1450~ 0x1453	Keypad I/O(GPIO [24:15]) and GPIO [14:0] Status	R/W	0x00	Indicate Keypad I/O(GPIO [24:15]) and GPIO [14:0] pin status
0x1454~ 0x1457	Keypad I/O(GPIO [24:15]) and GPIO [14:0 Direction Control	R/W	0x00	Select Keypad I/O(GPIO [24:15]) and GPIO [14:0] Input/Output Direction
0x1458~ 0x145B	Keypad I/O(GPIO [24:15]) and GPIO [14:0] Interrupt control	R/W	0x00	Enable/Disable Keypad I/O(GPIO [24:15]) and GPIO [14:0] Interrupt
0x145E	LCD Control	R/W	0x00	Enable/Disable LCD data, clock and chip selection control.
0x145F	UART I/O Control	R/W	0x00	Enable/Disable UART I/O control.

7.4 Gain Stage and Mixer Control Registers

Address	Name	Mode	Value At Reset	Function
0x1460	Gain Stage and Mixer Control	R/W	0x00	Enable/Disable Gain Stage for Side tone Gain, CODEC to AEC Gain, AEC to CODEC Gain, AEC to Mixer Gain, Mixer to AEC Gain and USB in/USB out Gain. Select Mixer mode for USB, CODEC and PCM.
0x1461~ 0x1467	Gain Stage Index	R/W	0x00	Set Audio Gain Index Register Value (Side tone Gain, CODEC to AEC Gain, AEC to CODEC Gain, AEC to Mixer Gain, Mixer to AEC Gain, USB in and USB out Gain)
0x1468~ 0x146B	MCU Record	R	0x00	Enable/Disable MCU to monitor USB ISO In/Out data
0x146C~ 0x146F	MCU Play	R/W	0x00	Enable/Disable MCU write data to USB and CODEC

7.5 PCM Control Registers

Address	Name	Mode	Value At Reset	Function
0x1470	PCM Control	R/W	0x00	Enable/Disable PCM Interface and Bit Clock / Frame Sync selection
0x1472	PCM Frame Sync Length	R/W	0x00	Set Frame Sync pulse length

7.6 CODEC Control Registers

Address	Name	Mode	Value At Reset	Function
0x1480	CODEC control	R/W	0x00	Enable/Disable CODEC, Select Sampling Rate and High Pass Frequency
0x1481	Dither Control	R/W	0x00	Enable/Disable Dither Function
0x1482~ 0x1483	CODEC ADC Digital Gain	R/W	0x04 0x00	Set Digital ADC Path Gain
0x1484~ 0x1485	CODEC DAC Digital Gain	R/W	0x04 0x00	Set Digital DAC Path Gain
0x1488	CODEC MIC Control	R/W	0x00	Set microphone bias voltage and bias resistor reference
0x1489	CODEC MIC Control	R/W	0x00	Select MIC interface mode and Set microphone gain
0x148A	CODEC Speaker Control	R/W	0x00	Attenuate speaker phone/ earphone speaker and Set speaker gain
0x148B	CODEC Analog Control	R/W	0x00	Enable/Disable CODEC Analog Block

7.7 SPI Control Registers

Address	Name	Mode	Value At Reset	Function
0x14A0	SPI Clock and Interface	R/W	0x00	Enable/Disable SPI interface and Select SPI bit clock rate
0x14A1	SPI Command Interface Control	R/W	0x00	Set SPI interface command length, R/W and other control
0x14A2	SPI Data Length	RW	0x00	Set SPI interface data field length
0x14A3	SPI Interrupt Control	R/W	0x00	Enable/Disable SPI interface interrupt
0x14A4~ 0x14A8	SPI Command Byte Control	RW	0x00	Set SPI interface command byte 1 to 5
0x14AB	SPI Clock Format Control	RW	0x00	Set SPI interface clock format
0x14AC	SPI FIFO Data	RW	0x00	Read/write data from SPI interface FIFO
0x14AD	SPI Byte Count	R	0x00	Current SPI interface FIFO counter value
0x14AE	SPI Write Count	R/W	0x00	MCU current Write point for SPI interface FIFO
0x14AF	SPI Read Count	R/W	0x00	MCU current Read point for SPI interface FIFO

7.8 W2S Control Registers

Address	Name	Mode	Value At Reset	Function
0x14B0	W2S Enable	R/W	0x00	Enable/Disable W2S bus controller
0x14B1	EEPROM control	R/W	0x00	Set different page mode and page size of EEPROM
0x14B2~ 0x14B3	W2S Clock	R/W	0x00	Set W2S bit clock rate
0x14B4	W2S R/W FIFO	R/W	0x00	Read/Write W2S compatible device
0x14B5	W2S R/W Operation Control	R/W	0x00	Set W2S Read/Write and FIFO control
0x14B6	W2S Status	R/W	0x00	Indicate W2S FIFO space and ACK signal status
0x14B7	FIFO Read Pointer	R/W	0x00	Indicate W2S FIFO read pointer
0x14B8	FIFO Write Pointer	R/W	0x00	Indicate W2S FIFO write pointer
0x14B9	ACK Failure Detect	R/W	0x00	Set ACK failure detect and indicate failure data pointer in FIFO
0x14BA	W2S Miscellaneous Control	R/W	0x00	Indicate status for SCL_in, finite state machine state and interrupt signal status

7.9 Ring Tone (PWM) Control Registers

Address	Name	Mode	Value At Reset	Function
0x14C0	PWM Clock	R/W	0x00	Enable/Disable PWM Operation Clock
0x14C2	PWM Tone1 Control	R/W	0x00	Set Tone 1 Volume
0x14C3	PWM Tone1 Frequency	R/W	0x00	Set Tone 1 Frequency
0x14C4	PWM Tone2 Control	R/W	0x00	Set Tone 2 Volume
0x14C5	PWM Tone2 Frequency	R/W	0x00	Set Tone 2 Frequency

7.10 Full/Half Duplex Acoustic Echo Cancellation (AEC) Control Registers

Address	Name	Mode	Value At Reset	Function
0x1600	AEC Configuration	R/W	0x96	Set AEC Configuration parameters
0x1601	AEC Reset Control	R/W	0x08	Set AEC power down and reset function
0x1602	AEC Mode Control	R/W	0x03	Set AEC Full/Half duplex mode and Noise suppressor
0x1605	Double Talk Long Term Power Time Constant	R/W	0x09	Set time constant for long term power estimation of double talk
0x1606	Double Talk Short Term Power Time Constant	R/W	0x0B	Set time constant for short term power estimation of double talk
0x1607~ 0x1608	Double Talk Hangover Time	R/W	0x0020	Set hangover time window of double talk detection algorithm
0x1609~ 0x160A	Double Talk Deviation Threshold	R/W	0x19A8	Set deviation power threshold of double talk
0x160B~ 0x161C	Double Talk Long Term Power Threshold	R/W	0x0000	Set power threshold for long term power estimation of double talk
0X160D~ 0x160E	Double Talk Short Term Power Threshold	R/W	0x1010	Set power threshold for short term power estimation of double talk
0X160F	AEC Divergence Threshold	R	0x0F	Set AEC Divergence threshold
0x1610	Voice Detect Long Term Power Time Constant	R/W	0x09	Set time constant for long term power estimation of Voice Detect
0x1611	Voice Detect Short Term Power Time Constant	R/W	0x0B	Set time constant for short term power estimation of Voice Detect
0x1612~ 0x1613	Voice Detect Hangover Time	R/W	0x0009	Set hangover time window of Voice Detect detection algorithm

Address	Name	Mode	Value At Reset	Function
0x1614~ 0x1615	Voice Detect Deviation Threshold	R/W	0x1998	Set deviation power threshold of Voice Detect
0x1616~ 0x1617	Voice Detect Long Term Power Threshold	R/W	0x1998	Set power threshold for long term power estimation of Voice Detect
0x1618~ 0x1619	Voice Detect Short Term Power Low Threshold	R/W	0x0BA8	Set Low power threshold for short term power estimation of Voice Detect
0X161A~ 0X161B	Voice Detect Short Term Power High Threshold	R/W	0x1038	Set high power threshold for short term power estimation of Voice Detect
0X161C~ 0X161D	Voice Detect Short Term Power Average Threshold	R/W	0x0000	Set average power threshold for short term power estimation of Voice Detect
0X161E~ 0X161F	Power Cut Off Control	R/W	0x1998	Set zero reference bias for power cut off estimation
0x1620~ 0x1621	AGC Threshold	R/W	0x2000	Set maximum output power of AGC
0x1622~ 0x1623	AGC Noise Threshold	R/W	0x0320	Set AGC calculated input power with time constant
0x1624	AGC Gain from AEC	R/W	0x02	Set maximum gain for post echo cancellation signal
0x1625	AGC Gain Time constant	R/W	0xBB	Set delay time constant for long term gain estimation
0x1626	AGC Gain Time constant	R/W	0x09	Set delay time constant for short term gain estimation
0x1628	Soft Clip Control	R/W	0x00	Enable/Disable soft clip(SC) function
0x1629	Soft Clip Normal Gain Index	R/W	0x00	Set gain index of voice detect for soft clip module at normal gain mode
0x162A	Soft Clip Low Gain Index	R/W	0x00	Set gain index of voice detect for soft clip module at low gain mode
0x162B~ 0x162C	Soft Clip Threshold	R/W	0x1000	Set threshold level to select soft clip gain mode
0x162D	Soft Clip Power Time Constant	R/W	0x07	Set time constant for short term power calculation of voice detect soft clip
0x162E	Soft Clip Gain Time Constant	R/W	0x07	Set time constant to smooth gain mode change of soft clip
0x1630	Acoustic Suppression 1 Time Constant	R/W	0x77	Set time constant of acoustic suppression (AS1) for convergence towards target
0x1631- 0x1632	Acoustic Suppression 1 attenuation	R/W	0x1CA8	Set maximum attenuation value for acoustic suppression (AS1) algorithm
0x1633	Acoustic Suppression 2 Time Constant	R/W	0x77	Set time constant of acoustic suppression (AS2) for convergence towards target
0x1634~ 0x1635	Acoustic Suppression 2 attenuation	R/W	0x1CA8	Set maximum attenuation value for acoustic suppression (AS2) algorithm
0x1638	Noise Suppressor Control	R/W	0xBB	Set noise suppressor gain index and short term power time constant
0x1639	Noise Suppressor Gain Time Constant	R/W	0xBB	Set time constant for rise and fall of noise suppressor gain index

Address	Name	Mode	Value At Reset	Function
0x163A~ 0X163B	Noise Suppressor Active Power Threshold	R/W	0x03E8	Set threshold level for active noise suppressor
0x1640~ 0x1641	Short Term Power voice detector	R	0x0000	Indicate Short Term Power calculated by the voice detector (VD).
0x1642~ 0x1643	Long Term Power Voice Detector	R	0x0000	Indicate Long Term Power calculated by the voice detector (VD).
0x1644~ 0x1645	Voice Detector Power Deviation	R	0x0000	Indicate Power Deviation estimated by the voice detector (VD).
0x1648~ 0x1649	Short Term Power Double Talk	R	0x0000	Indicate Short Term Power calculated by double-talk detector (DT).
0x164A~0x 164B	Long Term Power Double Talk	R	0x0000	Indicate Long Term Power calculated by double-talk detector (DT).
0x164C~0x 164D	Double Talk Power Deviation	R	0x0000	Indicate Power Deviation estimated by the double-talk detector (DT).
0x1680	AGC Control	R/W	0x00	Enable / Disable AGC and Set max gain control
0x1681	AGC Initial Gain Control	R/W	0x00	Enable/Disable AGC initial gain setting
0x1682	AGC Gain Time	R/W	0x00	Set decreasing and increasing gain time for AGC
0x1683	AGC Peak Release Time	R/W	0x00	Set release time for AGC peak voice level
0x1684	AGC Gain Monitor	R	0x00	Indicate AGC gain status
0x1685	AGC Gain Region Monitor	R	0x00	Indicate AGC gain status at increasing, target or decreasing region.
0x1687~ 0x1689	AGC Short Term Power	R	0x0000	Indicate AGC Short Term Power estimation
0x168A~0x 168B	AGC Target Threshold	R/W	0x0000	Set AGC target region threshold
0x168C~0x 168D	AGC Noise Low Threshold	R/W	0x0000	Set AGC Noise low threshold level
0x168E~0x 168F	AGC Noise High Threshold	R/W	0x0000	Set AGC Noise high threshold level

7.11 USB Controller Registers

Address	Name	Mode	Value At Reset	Function
0x1800	USB Enable	R/W	0x00	Enable/Disable USB 1.1 function control
0x1801~ 0x1803	USB Interrupt Register A	R/W	0x00	Set USB endpoints interrupt enable, status and clear.
0x1804 ~ 0x1806	USB Interrupt Register B	R/W	0x00	Set USB endpoints interrupt enable, status and clear.

Address	Name	Mode	Value At Reset	Function
0x1807 ~ 0x1809	USB Interrupt Register C	R/W	0x00	Set USB Audio Class interrupt enable, status and clear.
0x1810	Endpoint 0 – Control In/Out	R/W	0x00	Set USB Control in/out Endpoint control
0x1811	Control In Data	R/W	0x00	Control in Endpoint Data. Internal FIFO has 1 byte for Control In transmission. If the 3rd Token byte is not equal to 0x01 or 0x03 (HID set report application), this byte will be transmitted instead of Control-IN FIFO and Interrupt-IN FIFO content.
0x1828 ~ 0x182F	Control Out Data	R	0x00	Control Out Endpoint receiving data.
0x1830	Endpoint 1 and 2 – ISO In/Out	R/W	0x00	Set ISO In/Out Endpoint control register.
0x1831	Sampling Frequency	R	0x00	Indicate ISO Sampling Frequency
0x1832-0x1833	Record Volume	R	0x00	Indicate Current Record Volume
0x1834-0x1835	Play Volume	R	0x00	Indicate Current Play Volume
0x1836	HID Control Out Information	R	0x00	Indicate First Packet and Valid Length
0x1837	Max Volume	R	0x00	Indicate Audio Path Max Volume Gain
0x1838	HID Token Information	R/W	0x00	Set HID Token 3rd byte
0x1839	HID Descriptor Length	R/W	0x00	This register value must be equal to the USB descriptor with respect to the HID return length
0x1840 ~ 0x1847	ISO SYNC Speed	R/W	0x00	Set ISO SYNC speed tuning parameter register.
0x1848	Endpoint 3 – Bulk In Control Register	R/W	0x00	Set Bulk In Endpoint control register
0x1849	Bulk In Data	W	0x00	Set Bulk In transmission data register except final data.
0x184A	Bulk In Final Data	W	0x00	Set Bulk In transmission final data register.
0x184B	Bulk In FIFO Empty Flag	R	0x00	Indicate Bulk In transmission data FIFO empty flag.
0x1850	Endpoint 4 – Bulk Out Control Register	R/W	0x00	Set Bulk Out Endpoint control register

Address	Name	Mode	Value At Reset	Function
0x1851	Bulk Out FIFO Length	R	0x00	Indicate Bulk Out Endpoint receiving data FIFO length.
0x1852	Bulk Out Data	R	0x00	Bulk Out Endpoint receiving data FIFO.
0x1858	Endpoint 5 – Interrupt In Control Register	R/W	0x00	Set Interrupt In Endpoint control register
0x1859	USB Interrupt Data Length	R/W	0x00	Interrupt In Endpoint transmission data length
0x1880	USB ISO MCU Enable	R/W	0x00	Enable ISO IN/OUT FIFO access by MCU
0x1881	USB ISO IN FIFO Depth	R	0x00	ISO OUT FIFO depth indication
0x1882	USB ISO OUT FIFO Depth	R	0x00	ISO IN FIFO depth indication
0x1883~ 0x1884	USB ISO IN DATA	R/W	0x00	ISO IN data sample will be written by MCU
0x1885~ 0x1886	USB ISO OUT DATA	R	0x00	ISO IN data sample will be read by MCU
0x2000- 0x21FF	USB Descriptor RAM data filed	R/W	0x00	USB Descriptor
0x2200- 0x223F	HID Control-IN data field	R/W	0x00	HID Control-IN data field
0x2240- 0x227F	HID Interrupt-IN data field	R/W	0x00	HID Interrupt-IN data field
0x2300- 0x233F	HID Control-OUT data field	R/W	0x00	HID Control-OUT data field

8. Microcontroller

8.1 Features

- 8-bit Turbo 8051 Microcontroller with 12/24/48 MHz speed
- 256 bytes of on chip internal data RAM and 1K bytes external data RAM
- Instruction set compatible with Nuvoton Turbo 8051
- Three 8-bit I/O ports
- Three 16-bit timers
- One Full-duplex serial port
- On-Chip debugger via JTAG (Joint Test Access Group) port
- 7 interrupt sources with two level priorities
- Programmable Watchdog Timer
- Two 16-bit data pointers
- On Chip 8 KB OTP (One time programmable) memory

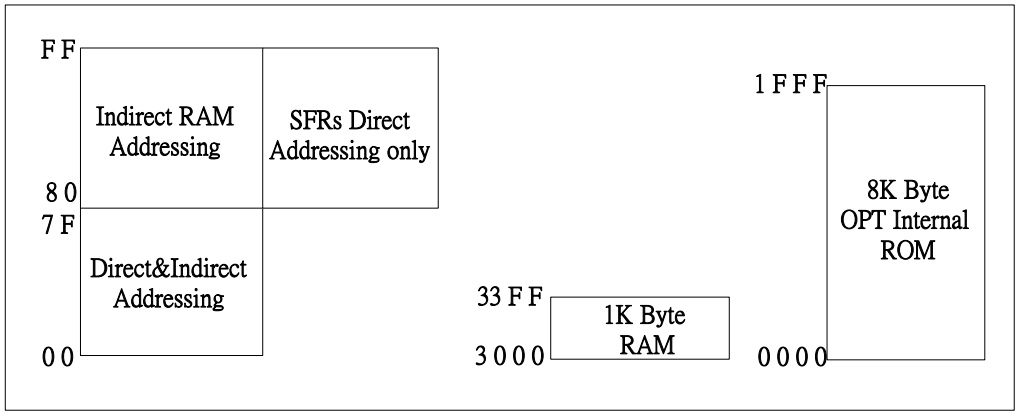
8.2 Memory Organization

8.2.1 Program Memory

On-chip 8k OTP Memory:
All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

8.2.2 Data Memory

The MCU can access 1K bytes of external Data Memory. This memory region is accessed by the MOVX instruction. Additionally it has 256 bytes on chip RAM which can be accessed either by direct addressing or by indirect addressing. Some Special Function Registers (SFRs) can only be accessed by direct addressing.



8.2.3 Special Function Registers (SFR)

Address	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
F8	EIP							
F0	B							
E8	EIE							
E0	ACC							
D8	WDCON							
D0	PSW							
C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2		
C0					PMR	STATUS		TA
B8	IP	SADEN						
B0	P3							
A8	IE	SADDR						
A0	P2	XRAMAH						
98	SCON	SBUF						
90	P1							
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	
80	P0	SP	DPL	DPH	DPL1	DPH1	DPS	PCON

Table 2 W681308 MCU SFR location

8.3 Power Management

The W681308 has IDLE mode operation features that manage and save power consumption of the device.

Enable IDLE mode

The user can set the device into idle mode by writing 1 to the PCON bit of SFR. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle mode, the clock to the MCU is halted but not to the Interrupt, Timer, Watchdog timer, and Serial ports blocks. This forces the MCU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The ALE and PSEN pins are held high during the idle state. The port pins hold the logical states they had at the time Idle was activated.

The Idle mode can be terminated in two ways:

- **Activation of any enabled interrupt**

Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically clear the Idle bit, terminate the Idle mode, and the Interrupt Service Routine (ISR) will be executed. After the ISR, execution of the program will continue from the instruction which put the device into idle mode.

- **Activation of reset**

The Idle mode can also be exited by activating the reset. The device can be put into reset either by applying a high on the external RST pin, a Power on reset condition or a Watchdog timer reset. The external reset pin has to be held high for at least two machine cycles i.e. 8 clock periods to be recognized as a valid reset. In the reset condition the program counter is reset to 0000h and all the SFRs are set to the reset condition. Since the clock is already running there is no delay and execution starts immediately. In Idle mode, the Watchdog timer continues to run, and if enabled, a time-out will cause a watchdog timer interrupt which will wake up the device. The software must reset the Watchdog timer in order to preempt the reset which will occur after 512 clock periods of the time-out. When the W681308 is exiting from an idle mode with a reset, the instruction following the one which put the device into idle mode is not executed. So there is no danger of unexpected writes.

8.4 Reset Conditions

There are two ways to put device into reset state: external reset and watchdog reset.

8.4.1 External Reset

The device continuously samples the RST pin at state C4 of every machine cycle. Therefore the RST pin must be held for at least 2 machine cycles to ensure detection of a valid RST high. The reset circuitry then synchronously applies the internal reset signal. Thus the reset is synchronous operation and requires the clock to be running to cause an external reset. Once the device is in reset condition, it will remain so long as RST is 1. Even after RST is deactivated, the device will continue to be in reset state for up to two machine cycles, and then begin program execution from 0000h.

8.4.2 Watchdog Reset

The Watchdog timer is a free-running timer with programmable time-out intervals. The user can clear the watchdog timer at any time, causing it to restart the count. When the time-out interval is reached an interrupt flag is set. If the Watchdog reset is enabled and the watchdog timer is not cleared, then 512 clocks from the flag being set, the watchdog timer will generate a reset. This places the device into the reset condition. The reset condition is maintained by hardware for two machine cycles. Once the reset is removed the device will begin execution from 0000h.

8.5 Interrupts

The W681308 MCU has three priority levels interrupt structure with 7 interrupt sources. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. Additionally, all the interrupts can be globally enabled or disabled.

Source	Flag	Priority	Vector address
External Interrupt 0	IE0	1 (highest)	0003h
Timer 0 Overflow	TF0	2	000Bh
External Interrupt 1	IE1	3	0013h
Timer 1 Overflow	TF1	4	001Bh
Serial Port	RI + TI	5	0023h
Timer 2 Overflow	TF2 + EXF2	6	002Bh
Watchdog Timer	WDIF	7 (lowest)	0063h

Table 3 Interrupt Priority Structure

8.6 Programming Timers and Counters

The MCU of W681308 has three 16-bit programmable timers/counters and one programmable Watchdog timer. The Watchdog timer is operationally quite different from the other three timers.

8.6.1 Timers/Counters 0 and 1

Timer 0 (TM0) and Timer 1 (TM1) are 16-bit Timer/Counters and are nearly identical. Each of these Timers/Counters has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. The two timers can be configured to operate either as timers to count machine cycles or as counters counting external inputs.

In Timer mode, the timer counts clock cycles. The timer clock can be programmed to be thought of as 1/12 of the system clock or 1/4 of the system clock.

In Counter mode, the register is incremented on the falling edge of the corresponding external input pins, T0 for Timer 0 and T1 for Timer 1. The T0 and T1 inputs are sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine cycles to recognize a negative transition on the pin, the minimum period at which counting will take place is double of the machine cycle.

In either the Timer or Counter mode, the count register will be updated at C3. Therefore, in the Timer mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine cycle following the one in which the negative edge was detected.

The Timer or Counter function is selected by the C/T bit in the TMOD Special Function Register. Each Timer/Counter has one selection bit for its own. Bit 2 of TMOD selects the function for Timer/Counter 0 and bit 6 of TMOD selects the function for Timer/Counter 1.

89H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMOD	GATE	C/T	M1	M0	GATE	C/T	M1	M0
88H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Table 4 Timer Mode/Control TMOD/TCON SFR

8.6.2 Timer/Counter 2

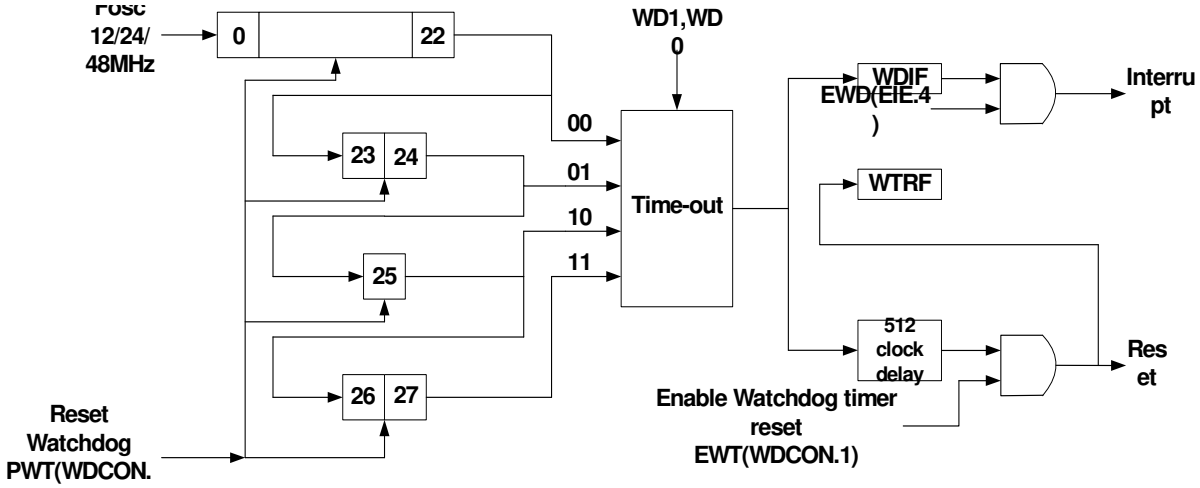
Timer/Counter 2 is a 16 bit up/down counter which is configured by the T2MOD register and controlled by the T2CON register. Timer/Counter 2 is equipped with a capture/reload capability. As with the Timer 0 and Timer 1 counters, they provide wide selection and control of the clock and selection of the operating modes. The clock source for Timer/ Counter 2 can be selected for the crystal oscillator, which is divided by 12 or 4 (C/T2 = 0). The clock is then enabled when TR2 is a 1, and disabled when TR2 is a 0.

C9H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2MOD	-	-	-	-	T2CR	-	-	DCEN
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2

Table 5 Timer 2 Mode/Control TMOD/TCON SFR

8.6.3 Watchdog Timer

The Watchdog timer is a free-running timer that can be programmed by the user to serve as a system supervisor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs the flag WDIF is set, which can cause an interrupt if enabled, and a system reset can also be caused if it is enabled. The interrupt will occur if the individual interrupt enable and the global enable are set. The interrupt and reset functions are independent of each other and may be used separately or together depending on the software employed.



When used as a simple timer, the reset and interrupt functions are disabled. The timer will set the WDIF flag each time the timer completes the selected time interval. The WDIF flag is polled to detect a time-out and the RWT allows software to restart the timer. The Watchdog timer can also be used as a very long timer. The interrupt feature is enabled in this case. Every time the time-out occurs an interrupt will occur if the global interrupt enable EA is set.