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W681360

3V SINGLE-CHANNEL
13-BIT LINEAR
VOICE-BAND CODEC

Data Sheet
Revision A.5

1. GENERAL DESCRIPTION

The W681360 is a general-purpose single channel 13–bit linear PCM CODEC with 2s complement data format. It operates from a single +3V power supply and is available in 20-pin SOG(SOP), SSOP and TSSOP package options. The primary function of the device is the digitization and reconstruction of voice signals, including the band limiting and smoothing required for PCM systems. The W681360 performance is specified over the industrial temperature range of –40°C to +85°C.

The W681360 includes an on-chip precision voltage reference. The analog section is fully differential, reducing noise and improving the power supply rejection ratio. The V_{AG} reference pin allows for decoupling of the internal circuitry that generates the reference voltage to the V_{SS} power supply ground, minimizing clock noise on the analog circuitry when external analog signals are referenced to V_{SS}.

The data transfer protocol supports both long-frame and short-frame, synchronous and asynchronous communications for PCM applications. The W681360 accepts eight master clock rates between 256kHz and 4.800MHz, and an on-chip pre-scaler automatically determines the division ratio for the required internal clock. An additional on-chip power amplifier is capable of driving 300Ω loads differentially up to a level of 3.544V peak-to-peak.

For fast evaluation a development kit (W681360DK) is available.
For fast prototyping purposes a low-cost evaluation board (W681360ES) is also available.

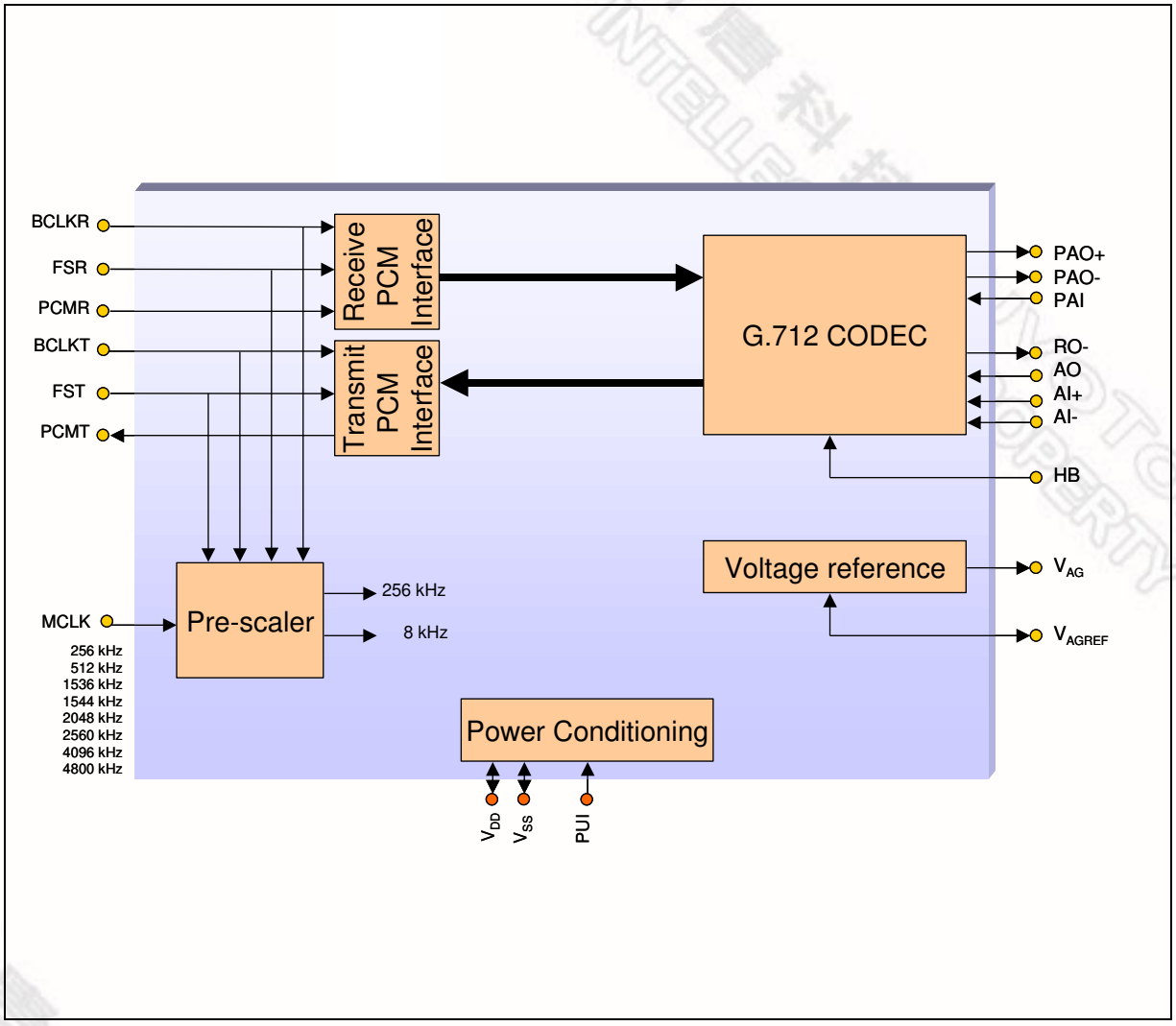
2. FEATURES

- Single +3V power supply (2.7V to 5.25V)
- Typical power dissipation: 9.8mW
  Standby power dissipation: 3µW
  Power-Down dissipation: 0.09µW
- Fully-differential analog circuit design for low noise
- 13-bit linear A/D & D/A conversions with 2s complement data format
- CODEC A/D and D/A filtering compliant with ITU G.712
- Eight master clock rates of 256kHz to 4.800 MHz
- 256KHz – 4.8MHz bit clock rates on the serial PCM port
- On-chip precision reference of 0.886 V for a -5 dBm TLP at 600 Ω (436mV_{RMS})
- Programmable receive gain: 0 to –21dB in 3dB steps
- Industrial temp. range (–40°C to +85°C)
- 20-pin SOG (SOP), SSOP and TSSOP as well as a QFN-32L package
- Pb-Free / RoHS package options available

Applications

- VoIP, Voice over Networks equipment
- Digital telephone and communication systems
- Wireless Voice devices
- DECT/Digital Cordless phones
- Broadband Access Equipment
- Bluetooth Headsets
- Fiber-to-curb equipment
- Enterprise phones
- Digital Voice Recorders

3. BLOCK DIAGRAM



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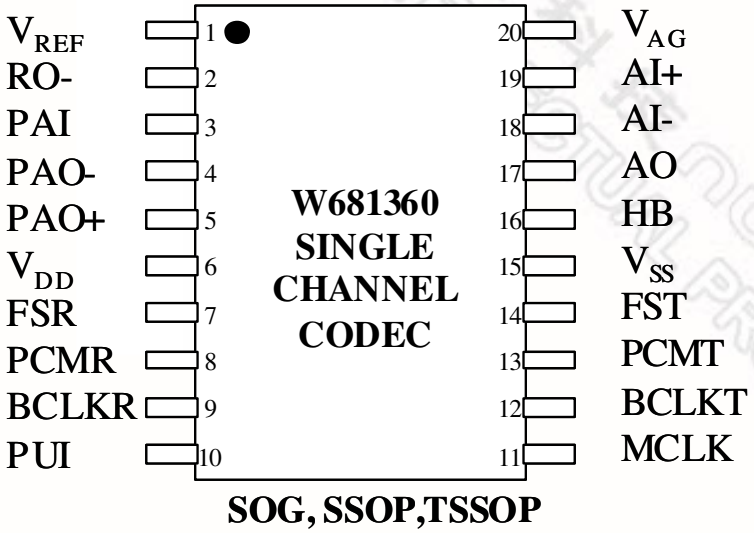
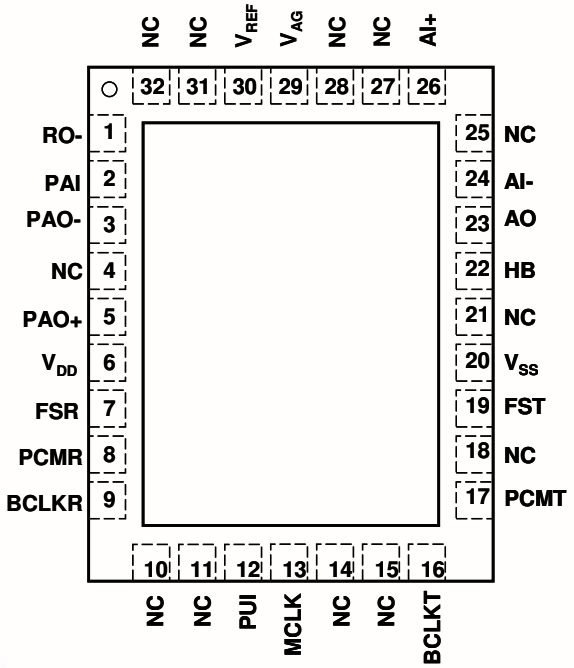
5. PIN CONFIGURATION



SOG, SSOP,TSSOP



QFN-32L

6. PIN DESCRIPTION

Pin Name	Pin No.		Functionality
	non-QFN	QFN	
V_{REF}	1	30	This pin is used to bypass the on–chip $V_{DD}/2$ voltage reference for the V_{AG} output pin. This pin should be bypassed to V_{SS} with a 0.1μF ceramic capacitor using short, low inductance traces. The V_{REF} pin is only used for generating the reference voltage for the V_{AG} pin. Nothing is to be connected to this pin except the bypass capacitor.
RO-	2	1	Inverting output of the receive smoothing filter. This pin can typically drive a 2kΩ load to $0.886V_{PEAK}$ referenced to analog ground.
PAI	3	2	Inverting input to the power amplifier. The non-inverting input is tied internally to V_{AG} voltage.
PAO-	4	3	Inverting power amplifier output. The PAO- and PAO+ can drive a 300Ω load differentially to $1.772V_{PEAK}$.
PAO+	5	5	Non-inverting power amplifier output. The PAO- and PAO+ can drive a 300Ω load differentially to $1.772V_{PEAK}$.
V_{DD}	6	6	Power supply. Should be decoupled to V_{SS} with a 0.1μF ceramic capacitor.
FSR	7	7	8kHz Frame Sync input for the PCM receive section. FSR can be asynchronous to FST in either Long Frame Sync or Short Frame Sync mode.
PCMR	8	8	PCM input data receive pin. The data needs to be synchronous with the FSR and BCLKR pins.
BCLKR	9	9	PCM receive bit clock input pin. Can accept any bit clock frequency from 256 to 4800kHz. When not clocked it can be used to select the 16 sign-bit extended synchronous mode (BCLKR=0) or the receive gain adjust synchronous mode (BCLKR=1)
PUI	10	12	Power up input signal. When this pin is tied to V_{DD}, the part is powered up. When tied to V_{SS}, the part is powered down.
MCLK	11	13	System master clock input. Possible input frequencies are 256kHz, 512kHz, 1536kHz, 1544kHz, 2048kHz, 2560kHz, 4096kHz & 4800kHz. For performance reasons, it is recommended that MCLK be synchronous and aligned to the FST signal. This is a requirement in the case of 256 and 512kHz frequencies.
BCLKT	12	16	PCM transmit bit clock input pin. Can accept any bit clock frequency from 256 to 4800kHz.
PCMT	13	17	PCM output data transmit pin. The output data is synchronous with the FST and BCLKT pins.
FST	14	19	8kHz transmit frame sync input. This pin synchronizes the transmit data bytes.
V_{SS}	15	20	This is the supply ground. This pin should be connected to 0V.

Pin Name	Pin No.		Functionality
	non-QFN	QFN	
HB	16	22	High-pass Bypass. Determines if the transmit high-pass filter is used (HB='0') or bypassed (HB='1'). When the high pass is bypassed the frequency response extends to DC.
AO	17	23	Analog output of the first gain stage in the transmit path.
AI-	18	24	Inverting input of the first gain stage in the transmit path.
AI+	19	26	Non-inverting input of the first gain stage in the transmit path.
V_{AG}	20	29	Mid-Supply analog ground pin, which supplies a $V_{DD}/2$ volt reference voltage for all-analog signal processing. This pin should be decoupled to V_{SS} with a 0.01μF capacitor. This pin becomes high impedance when the chip is powered down.

7. FUNCTIONAL DESCRIPTION

W681360 is a single-rail, single channel PCM CODEC for voiceband applications. The CODEC complies with the specifications of the ITU-T G.712 recommendation. The CODEC block diagram in Section 3 illustrates the main components of the W681360. The chip consists of a PCM interface, which can process long and short frame sync formats. The pre-scaler of the chip provides the internal clock signals and synchronizes the CODEC sample rate with the external frame sync frequency. The power conditioning block provides the internal power supply for the digital and the analog section, while the voltage reference block provides a precision analog ground voltage for the analog signal processing.

The calibration level for both the Analog to Digital Converter (ADC) and the Digital to Analog Converter (DAC) is referenced to μ-Law with the same bit voltage weighing about the zero crossing, resulting in the 0dBm0 calibration level 3.2dB below the peak sinusoidal level before clipping, Based on the reference voltage of 0.886V the calibration level is 0.436 Vrms or –5dBm at 600Ω.

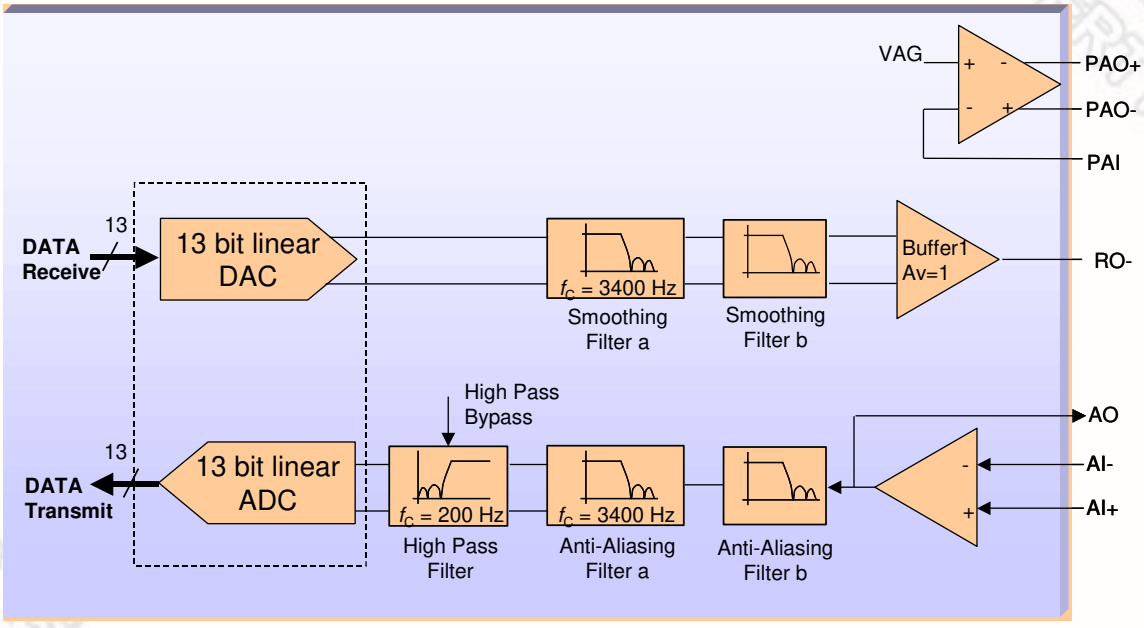


FIGURE 7.1: THE W681360 SIGNAL PATH

7.1. Transmit Path

The first stage of the A-to-D path of the CODEC is an analog input operational amplifier with externally configurable gain settings. A differential analog input may be applied to the Inputs AI+ and AI-. Alternately the input amplifier may be powered down and a single-ended input signal can be applied to either the AO pin or the AI- pin. The input amplifier can be powered down by connecting the AI+ pin to

either V_{DD} or V_{SS} which also determines whether AO or AI+ is selected as input according to Table 7.1. When the input operational amplifier is powered down the AO pin becomes high input impedance.

TABLE 7.1: INPUT AMPLIFIER MODES OF OPERATION

AI+ (Pin 19)	**Input Amplifier**	**Input**
V_{DD}	Powered Down	AO (Pin 17)
1.2 to V_{DD}-1.2	Powered Up	AI+, AI- (Pins 19, 18)
V_{SS}	Powered Down	AI- (Pin 18)

When the input amplifier is powered down, the input signal at AO or AI- should be referenced to the analog ground voltage V_{AG}.

The output of the input operational amplifier is first fed through a low-pass filter to prevent aliasing at the switched capacitor 3.4kHz low pass filter. Subsequently the 3.4kHz switched capacitor low pass filter bandlimits the input signals well below 4kHz. Signals above 4kHz would be aliased at the sampling rate of 8kHz. A high pass filter with a 200Hz cut-off frequency prevents DC coupling. All filters are designed according to the G.712 ITU-T specification. The high-pass filter may be bypassed depending on the logic level on the HB pin. If the high pass is removed the frequency response of the device extends down to DC.

After filtering the signal is digitized as a 13-bit linear PCM code and fed to the PCM interface for serial transmission at the sample rate supplied by the external frame sync FST.

7.1.1 Input Operational Amplifier Gain

The gain of the input operational amplifier can be adjusted using external resistors. For single-ended input operation the gain is given by a simple resistive ratio.

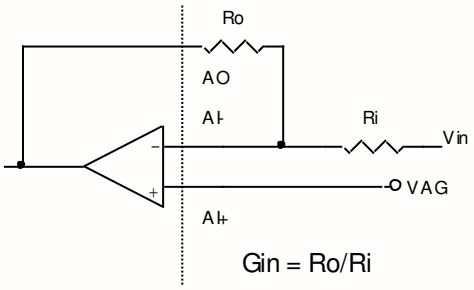


FIGURE 7.2: INPUT OPERATIONAL AMPLIFIER GAIN – SINGLE-ENDED INPUT

For differential input operation the external resistor network is more complex but the gain is expressed in the same way. Of course, a differential input also has an inherent 6dB advantage over a corresponding single-ended input.

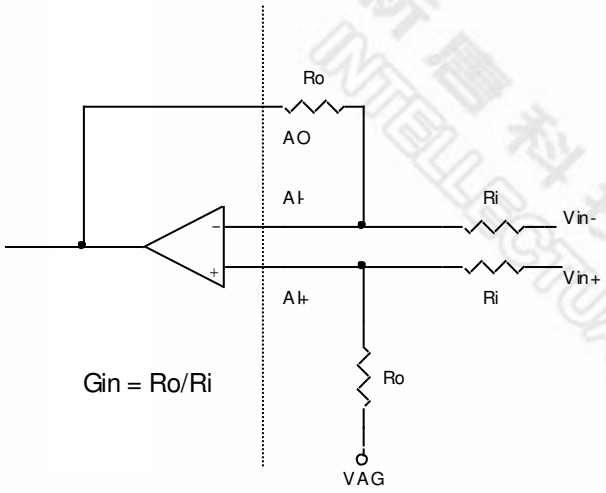


FIGURE 7.3: INPUT OPERATIONAL AMPLIFIER GAIN – DIFFERENTIAL INPUT

The gain of the operational amplifier will be typically be set to 30dB for microphone interface circuits. However the gain may be used for more than 30dB but this will require a compact layout with minimal trace lengths and good isolation from noise sources. It is also recommended that the layout be as symmetrical as possible as imbalances work against the noise canceling advantages of the differential design.

7.2. Receive Path

The 13-bit digital input samples for the D-to-A path are serially shifted in by the PCM interface and converted to parallel data bits. During every cycle of the frame sync FSR, the parallel data bits are fed through the 13-bit linear DAC and converted to analog samples. The analog samples are filtered by a low-pass smoothing filter with a 3.4kHz cut-off frequency, according to the ITU-T G.712 specification. A sin(x)/x compensation is integrated with the low pass smoothing filter. The output of this filter is buffered to provide the receive output signal RO-. The output may be also be attenuated when the device is in the receive path adjust mode. If the device is operated half–channel with the FST pin clocking and FSR pin held LOW, the receive filter input will be connected to the V_{AG} voltage. This minimizes transients at the RO– pin when full–channel operation is resumed by clocking the FSR pin.

The RO- output can be externally connected to the PAI pin to provide a differential output with high driving capability at the PAO+ and PAO- pins. By using external resistors various gain settings of this output amplifier can be achieved. If the transmit power amplifier is not in use, it can be powered down by connecting PAI to V_{DD}. The bias voltage and signal reference of the PAO+ & PAO– outputs is the V_{AG} pin. The V_{AG} pin cannot source or sink as much current as these pins, and therefore low impedance loads must be placed between PAO+ and PAO–. The PAO+ and PAO– differential drivers are also capable of driving a 100Ω resistive load or a 100nF piezoelectric transducer in series with a 20Ω resister with a small increase in distortion. These drivers may be used to drive resistive loads of 32Ω when the gain of PAO– is set to 1/4 or less.

7.2.1. Receive Gain Adjust Mode

The W681360 can be put in the receive path adjust mode by applying a logic "1" to the BCLKR pin while all other clocks are clocked normally. The device is then in a position to read 16-bits of data, with three additional coefficient bits an addend to the 13-bit digital voice data. These three coefficients are used to program a receive path attenuation, thereby allowing the receive signal to be attenuated according to the values in the following table. If the feature is not used the default value is 0dB.

Coefficient	Attenuation (dB)
000	0
001	3
010	6
011	9
100	12
101	15
110	18
111	21

TABLE 7.2: ATTENUATION COEFFICIENT RELATIONSHIP IN RECEIVE GAIN ADJUST MODE

7.3. POWER MANAGEMENT

7.3.1. Analog and Digital Supply

The power supply for the analog and digital parts of the W681360 must be 2.7V to 5.25V. This supply voltage is connected to the V_{DD} pin. The V_{DD} pin needs to be decoupled to ground through a 0.1 μF ceramic capacitor.

7.3.2. Analog Ground Reference Bypass

The system has an internal precision voltage reference which generates the $V_{DD}/2$ mid-supply analog ground voltage. This voltage needs to be decoupled to V_{SS} at the V_{REF} pin through a 0.1 μF ceramic capacitor.

7.3.3. Analog Ground Reference Voltage Output

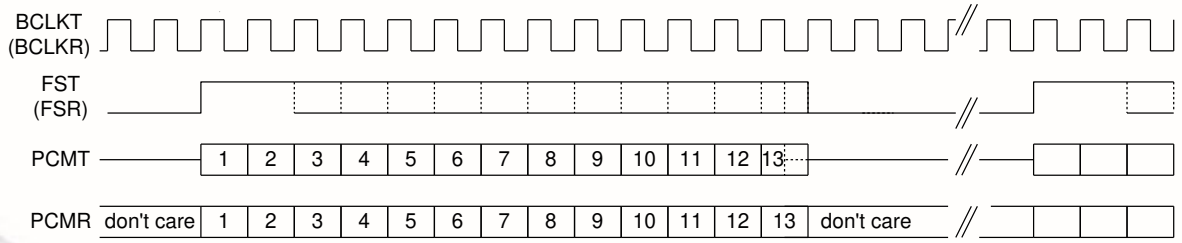
The analog ground reference voltage is available for external reference at the V_{AG} pin. This voltage needs to be decoupled to V_{SS} through a 0.01 μF ceramic capacitor. The analog ground reference voltage is generated from the voltage on the V_{REF} pin and is also used for the internal signal processing.

7.4. PCM INTERFACE

The PCM interface is controlled by pins BCLKR, FSR, BCLKT & FST. The input data is received through the PCMR pin and the output data is transmitted through the PCMT pin.
The Long Frame Sync or Short Frame Sync interface mode can be selected by connecting the BCLKR or BCLKT pin to a 256kHz to 4.800 MHz clock and connecting the FSR or FST pin to the 8kHz frame sync. The device synchronizes the data word for the PCM interface and the CODEC sample rate on the positive edge of the Frame Sync signal. Long Frame Sync is recognized when the FST pin is held HIGH for two consecutive falling edges of the bit-clock at the BCLKT pin. Short Frame Sync Mode is recognized when the Frame Sync signal at pin FST is HIGH for one and only one falling edge of the bit-clock at the BCLKT pin.

7.4.1. Long frame sync

The device recognizes a Long Frame Sync when the FST pin is held HIGH for two consecutive falling edges of the bit-clock at the BCLKT pin. The length of the Frame Sync pulse can vary from frame to frame, as long as the positive frame sync edge occurs every 125 μsec. During data transmission in the Long Frame Sync mode, the transmit data pin PCMT will become low impedance when the Frame Sync signal FST is HIGH or when the 13-bit data word is being transmitted. The transmit data pin PCMT will become high impedance when the Frame Sync signal FST becomes LOW while the data is transmitted or when half of the LSB is transmitted. The internal decision logic will determine whether the next frame sync is a long or a short frame sync, based on the previous frame sync pulse. To avoid bus collisions, the PCMT pin will be high impedance for two frame sync cycles after every power down state. Long Frame Sync mode is illustrated below. More detailed timing information can be found in the interface timing section.



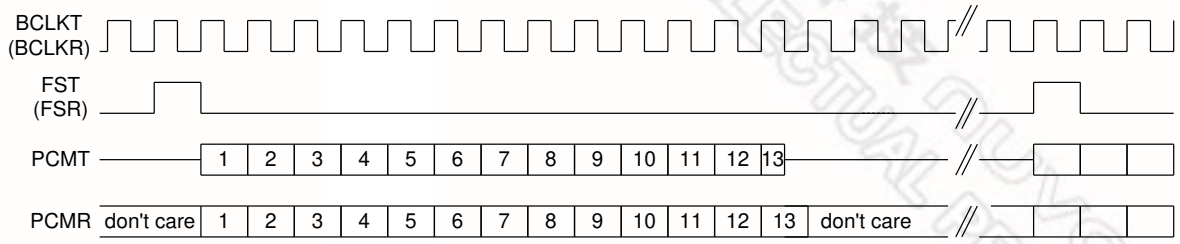
Long Frame Sync (Transmit and Receive Have Individual Clocking)

FIGURE 7.4: LONG FRAME SYNC PCM MODE

7.4.2. Short frame sync

The W681360 operates in the Short Frame Sync Mode when the Frame Sync signal at pin FST is HIGH for one and only one falling edge of the bit-clock at the BCLKT pin. On the following rising edge of the bit-clock, the W681360 starts clocking out the data on the PCMT pin, which will also change from high to low impedance state. The data transmit pin PCMT will go back to the high impedance state halfway through the LSB. The Short Frame Sync operation of the W681360 is based on a 13-bit data word. When receiving data on the PCMR pin, the data is clocked in on the first falling edge after

the falling edge that coincides with the Frame Sync signal. The internal decision logic will determine whether the next frame sync is a long or a short frame sync, based on the previous frame sync pulse. To avoid bus collisions, the PCMT pin will be high impedance for two frame sync cycles after every power down state. Short Frame Sync mode is illustrated below. More detailed timing information can be found in the interface timing section.



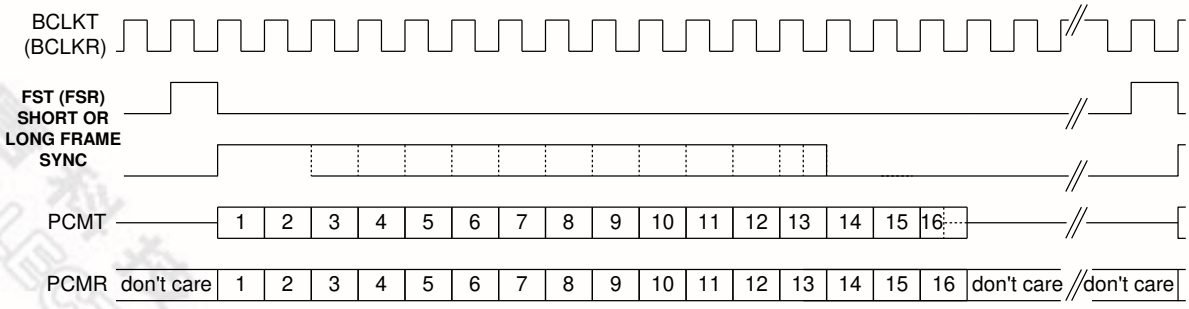
Short Frame Sync (Transmit and Receive Have Individual Clocking)

FIGURE 7.5: SHORT FRAME SYNC PCM MODE

7.4.3. Special 16-bit Receive Modes

7.4.3.1. Sign-Extended Mode Timing

The Sign-bit extended mode is entered by applying a logic “0” to the BCLKR pin while all other clocks are clocked normally. In standard 13-bit mode the first bit is the sign bit. In this mode the device transmits and receives 16-bit data where the sign bit is extended to the first four data bits. The PCM timing for this mode is illustrated below.

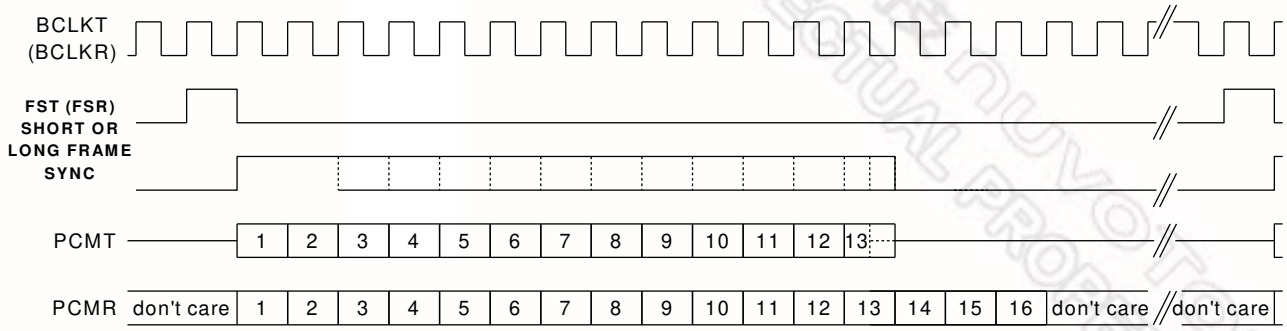


Sign-Extended (BCLKR=0)
Transmit and Receive both use BCLKT, and the first four data bits are the sign bit.
FST may occur at a different time than FSR

FIGURE 7.6: SIGN EXTENDED MODE

7.4.3.2. Receive Gain Adjust Mode Timing

The Receive Path Adjust Mode is entered by applying a logic “1” to the BCLKR pin while all other clocks are clocked normally. In this mode the device receives 16-bit data where the last three bits are coefficients to program the Receive Gain Adjust Attenuation described above. The PCM timing for this mode is illustrated below.



Receive Gain Adjust (BCLKR=1)
Transmit and Receive both use BCLKT. FST may occur at a different time than FSR.
Bits 14, 15, and 16, clocked into PCMR, are used for attenuation control for the receive analog output.

FIGURE 7.7: RECEIVE GAIN ADJUST TIMING MODE

7.4.4. System Timing

The system can work at 256kHz, 512kHz, 1536kHz, 1544kHz, 2048kHz, 2560kHz, 4096kHz & 4800kHz master clock rates. The system clock is supplied through the master clock input MCLK and can be derived from the bit-clock if desired. An internal pre-scaler is used to generate a fixed 256kHz and 8kHz sample clock for the internal CODEC. The pre-scaler measures the master clock frequency versus the Frame Sync frequency and sets the division ratio accordingly. If both Frame Syncs are LOW for the entire frame sync period while the MCLK and BCLK pin clock signals are still present, the W681360 will enter the low power standby mode. Another way to power down is to set the PUI pin to LOW. When the system needs to be powered up again, the PUI pin needs to be set to HIGH and the transmit Frame Sync pulse needs to be present. It will take two transmit Frame Sync cycles before the pin PCMT becomes low impedance.

7.5. ON-CHIP POWER AMPLIFIER

The on-chip power amplifier is typically used to drive an external loudspeaker. The inverting input to the power amplifier is available at pin PAI. The non-inverting input is tied internally to V_{AG}. The inverting output PAO– is used to provide a feedback signal to the PAI pin to set the gain of the power amplifier outputs (PAO+ and PAO-). These push–pull outputs are capable of driving a 300Ω load to 1.772 V_{PEAK}.
Connecting PAI to V_{DD} will power down the power driver amplifiers and the PAO+ and PAO– outputs will be high impedance.

8. TIMING DIAGRAMS

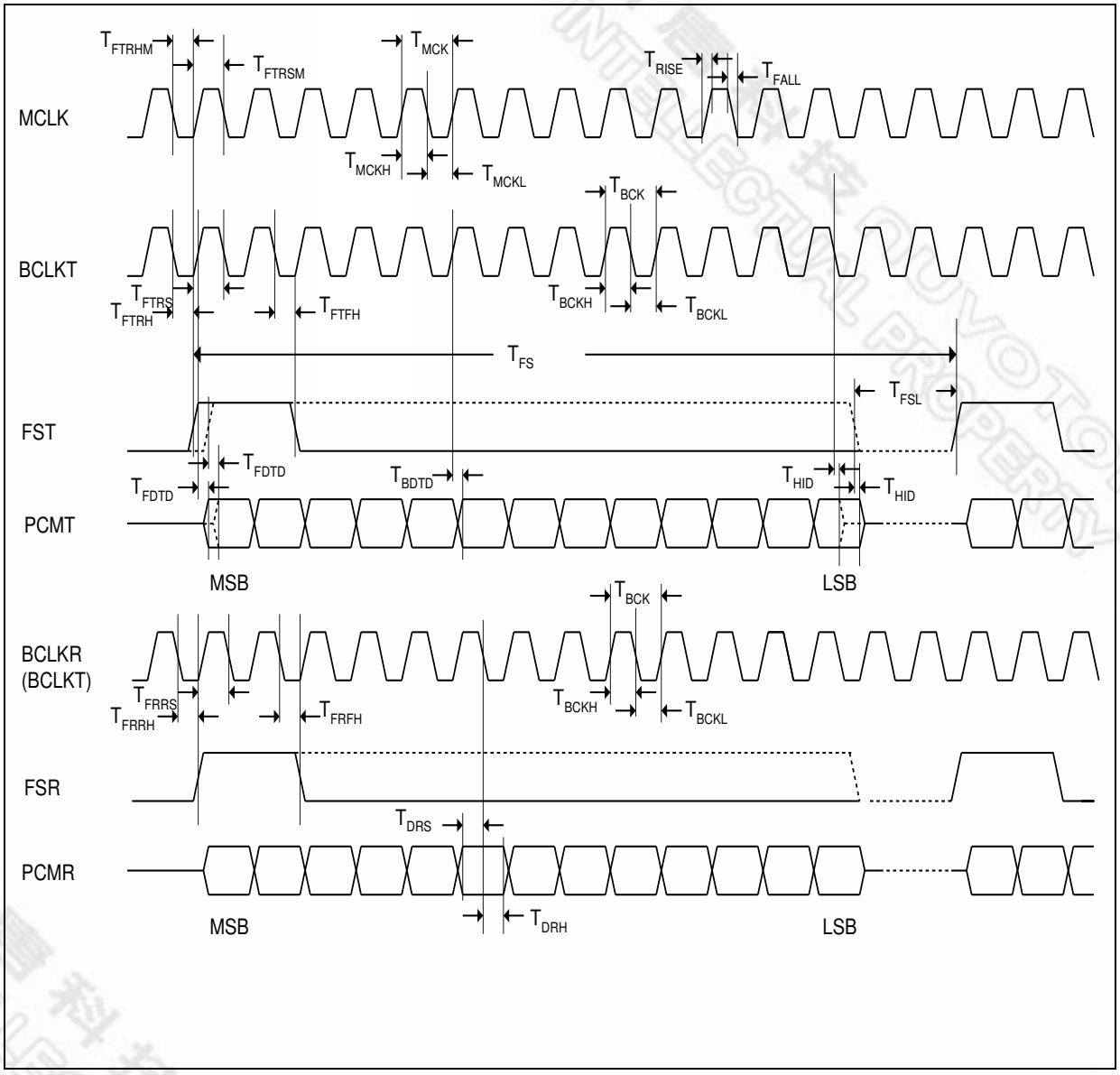


FIGURE 8.1: LONG FRAME SYNC PCM TIMING

NOTE: The Data is clocked out on the rising edge of BCLK.
The Data is clocked in on the falling edge of BCLK.

TABLE 8.1: LONG FRAME SYNC PCM TIMING PARAMETERS

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
$1/T_{FS}$	FST, FSR Frequency	---	8	---	kHz
T_{FSL}	FST / FSR Minimum LOW Width [1]	T_{BCK}			sec
$1/T_{BCK}$	BCLKT, BCLKR Frequency [1]	256	---	4800	kHz
T_{BCKH}	BCLKT, BCLKR HIGH Pulse Width	50	---	---	ns
T_{BCKL}	BCLKT, BCLKR LOW Pulse Width	50	---	---	ns
T_{FTRH}	BCLKT Falling Edge to FST Rising Edge Hold Time	20	---	---	ns
T_{FTRS}	FST Rising Edge to BCLKT Falling edge Setup Time	80	---	---	ns
T_{FTFH}	BCLKT Falling Edge to FST Falling Edge Hold Time	50	---	---	ns
T_{FDTD}	The later of BCLKT rising edge, or FST rising edge to first valid PCMT Bit Delay Time	---	---	60	ns
T_{BDTD}	BCLKT Rising Edge to Valid PCMT Delay Time	---	---	60	ns
T_{HID}	Delay Time from the Later of FST Falling Edge, or BCLKT Falling Edge of last PCMT Bit to PCMT Output High Impedance	10	---	60	ns
T_{FRRH}	BCLKR Falling Edge to FSR Rising Edge Hold Time	20	---	---	ns
T_{FRRS}	FSR Rising Edge to BCLKR Falling edge Setup Time	80	---	---	ns
T_{FRFH}	BCLKR Falling Edge to FSR Falling Edge Hold Time	50	---	---	ns
T_{DRS}	Valid PCMR to BCLKR Falling Edge Setup Time	1	---	---	ns
T_{DRH}	PCMR Hold Time from BCLKR Falling Edge	50	---	---	ns

[1] T_{FSL} must be at least ≥ T_{BCK}

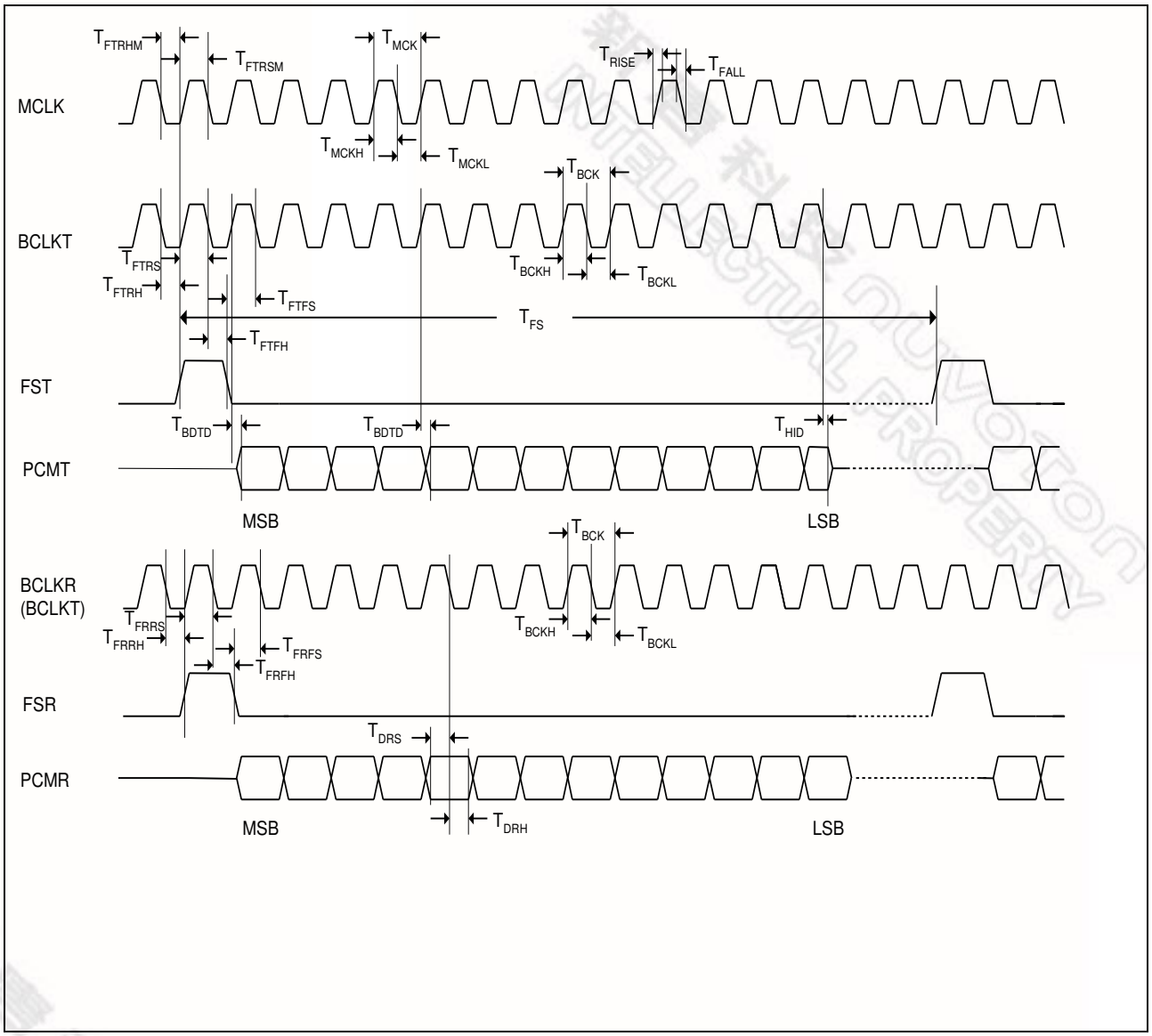


FIGURE 8.2: SHORT FRAME SYNC PCM TIMING

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
$1/T_{FS}$	FST, FSR Frequency	---	8	---	kHz
$1/T_{BCK}$	BCLKT, BCLKR Frequency	256	---	4800	kHz
T_{BCKH}	BCLKT, BCLKR HIGH Pulse Width	50	---	---	ns
T_{BCKL}	BCLKT, BCLKR LOW Pulse Width	50	---	---	ns
T_{FTRH}	BCLKT Falling Edge to FST Rising Edge Hold Time	20	---	---	ns
T_{FTRS}	FST Rising Edge to BCLKT Falling edge Setup Time	80	---	---	ns
T_{FTFH}	BCLKT Falling Edge to FST Falling Edge Hold Time	50	---	---	ns
T_{FTFS}	FST Falling Edge to BCLKT Falling Edge Setup Time	50	---	---	ns
T_{BDTD}	BCLKT Rising Edge to Valid PCMT Delay Time	10	---	60	ns
T_{HID}	Delay Time from BCLKT Falling Edge at last PCMT bit (LSB) to PCMT Output High Impedance	10	---	60	ns
T_{FRRH}	BCLKR Falling Edge to FSR Rising Edge Hold Time	20	---	---	ns
T_{FRRS}	FSR Rising Edge to BCLKR Falling edge Setup Time	80	---	---	ns
T_{FRFH}	BCLKR Falling Edge to FSR Falling Edge Hold Time	50	---	---	ns
T_{FRFS}	FSR Falling Edge to BCLKR Falling Edge Setup Time	50	---	---	ns
T_{DRS}	Valid PCMR to BCLKR Falling Edge Setup Time	1	---	---	ns
T_{DRH}	PCMR Hold Time from BCLKR Falling Edge	50	---	---	ns

TABLE 8.2: SHORT FRAME SYNC PCM TIMING PARAMETERS

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
$1/T_{MCK}$	Master Clock Frequency	---	256 512 1536 1544 2048 2560 4096 4800	---	kHz
T_{MCKH} / T_{MCK}	MCLK Duty Cycle for 256kHz Operation	45%		55%	
T_{MCKH}	Minimum Pulse Width HIGH for MCLK(512kHz or Higher)	50	---	---	ns
T_{MCKL}	Minimum Pulse Width LOW for MCLK (512kHz or Higher)	50	---	---	ns
T_{FTRHM}	MCLK falling Edge to FST Rising Edge Hold Time	50	---	---	ns
T_{FTRSM}	FST Rising Edge to MCLK Falling edge Setup Time	50	---	---	ns
T_{RISE}	Rise Time for All Digital Signals	---	---	50	ns
T_{FALL}	Fall Time for All Digital Signals	---	---	50	ns

Table 8.3: General PCM Timing Parameters

9. ABSOLUTE MAXIMUM RATINGS

9.1. ABSOLUTE MAXIMUM RATINGS

Condition	Value
Junction temperature	150^0C
Storage temperature range	-65^0C to $+150^0$C
Voltage applied to any pin	(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
Voltage applied to any pin (Input current limited to +/-20 mA)	(V_{SS} – 1.0V) to (V_{DD} + 1.0V)
V_{DD} - V_{SS}	-0.5V to +6V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

9.2. OPERATING CONDITIONS

Condition	Value
Industrial operating temperature	-40^0C to $+85^0$C
Supply voltage (V_{DD})	+2.7V to +5.25V
Ground voltage (V_{SS})	0V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

10. ELECTRICAL CHARACTERISTICS

10.1. GENERAL PARAMETERS

V_{DD}=2.7V – 3.6V; V_{SS}=0V; T_A=-40°C to +85°C;

Symbol	Parameters	Conditions	Min (2)	Typ (1)	Max (2)	Units
V_{IL}	Input LOW Voltage				0.6	V
V_{IH}	Input HIGH Voltage		2.2			V
V_{OL}	PCMT Output LOW Voltage	I_{OL} = 1.6 mA			0.4	V
V_{OH}	PCMT Output HIGH Voltage	I_{OL} = -1.6 mA	V_{DD}–0.5			V
I_{DD}	V_{DD} Current (Operating) - ADC + DAC	No Load		3.25	4.7	mA
I_{SB}	V_{DD} Current (Standby)	FST&FSR =V_{ss} ; PUI=V_{DD} (3)		1	100	µA
I_{PD}	V_{DD} Current (Power Down)	PUI= V_{ss} (3)		0.03	10	µA
I_{IL}	Input Leakage Current	V_{SS}<V_{IN}<V_{DD}	-10		+10	µA
I_{OL}	PCMT Output Leakage Current	V_{SS}<PCMT<V_{DD} High Z State	-10		+10	µA
C_{IN}	Digital Input Capacitance				10	pF
C_{OUT}	PCMT Output Capacitance	PCMT High Z			15	pF

1. *Typical values: T_A = 25°C , V_{DD} = 3.0 V*
2. *All min/max limits are guaranteed by Nuvoton via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *No DC load from VREF & VAG to Vss*

10.2. ANALOG SIGNAL LEVEL AND GAIN PARAMETERS

V_{DD}=2.7V to 3.6V; V_{SS}=0V; T_A=-40°C to +85°C; all analog signals referred to V_{AG}; 0dBm0 = 0.436 Vrms = -5dBm @ 600 Ohm; FST =FSR = 8kHz;MCLK=BCLK= 2.048 MHz

PARAMETER	SYM.	CONDITION	TYP.	TRANSMIT (A/D)		RECEIVE (D/A)		UNIT
				MIN.	MAX.	MIN.	MAX.	
Absolute Level	L_{ABS}	0 dBm0 = -5dBm @ 600Ω	0.616 0.436	---	---	---	---	V_{PK} V_{RMS}
Max. Transmit Level	T_{XMAX}		3.2 0.886	---	---	---	---	dBm0 V_{PK}
Absolute Gain (0 dBm0 @ 1020Hz; T_A=+25°C)	G_{ABS}	0 dBm0 @ 1020Hz; T_A=+25°C	0	-0.20	+0.20	-0.20	+0.20	dB
Absolute Gain variation with Temperature	G_{ABST}	T_A=0°C to T_A=+70°C T_A=-40°C to T_A=+85°C	0	-0.05 -0.10	+0.05 +0.10	-0.05 -0.10	+0.05 +0.10	dB
Frequency Response, Relative to 0dBm0 @ 1020Hz (HB=0)	G_{RTV}	15Hz 50Hz 60Hz 200Hz 300 to 1600Hz 1600 to 2400Hz 2400 to 3000Hz 3300Hz 3400Hz 3600Hz 4000Hz 4600Hz to 100kHz	--- --- --- --- --- --- --- --- --- --- --- ---	--- --- --- -1.4 -0.2 -0.2 -0.2 -0.2 -0.7 --- --- ---	-45 -30 -26 -0.4 +0.2 +0.2 +0.2 +0.2 +0.15 0 -12.5 -32	-0.5 -0.5 -0.5 -0.5 -0.2 -0.2 -0.25 -0.4 -0.8 --- --- ---	0 0 0 0 +0.2 +0.25 +0.2 +0.15 0 0 -12.5 -30	dB

10.3. ANALOG DISTORTION AND NOISE PARAMETERS

V_{DD}=2.7V to 3.6V; V_{SS}=0V; T_A=-40°C to +85°C; all analog signals referred to V_{AG}; 0dBm0 = 0.436 Vrms = -5dBm @ 600 Ohm; FST =FSR = 8kHz;MCLK=BCLK= 2.048 MHz

PARAMETER	SYM.	CONDITION	TRANSMIT (A/D)			RECEIVE (D/A)			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Total Distortion vs. Level Tone (1020Hz, C-Message Weighted)	D_{LT}	+3 dBm0 0 dBm0 -10 dBm0 -20 dBm0 -30 dBm0 -40 dBm0 -50 dBm0 -60 dBm0	45 50 51 50 41 32 22 12	55 60 60 54 44 34 24 14	--- --- --- --- --- --- --- ---	50 48 45 48 45 35 25 14	60 63 60 55 47 37 27 17	--- --- --- --- --- --- --- ---	dBC
Spurious Out-Of-Band at RO- (300Hz to 3400Hz @ 0dBm0)	D_{SPO}	4600Hz to 7600Hz 7600Hz to 8400Hz 8400Hz to 100000Hz	--- --- ---	--- --- ---	--- --- ---	--- --- ---	--- --- ---	-30 -40 -30	dB
Crosstalk (1020Hz @ 0dBm0)	D_{XT}		---	---	-75	---	---	-75	dB
Absolute Group Delay	τ_{ABS}	1200Hz (HB=0)	---	---	360	---	---	240	μsec
Group Delay Distortion (relative to group delay @ 1200Hz)	τ_D	500Hz 600Hz 1000Hz 2600Hz 2800Hz	--- --- --- --- ---	--- --- --- --- ---	750 380 130 130 750	--- --- --- --- ---	--- --- --- --- ---	750 370 120 120 750	μsec
Idle Channel Noise	N_{IDL}	C-message weighted Psophometric weighted	--- ---	--- ---	18 -72	--- ---	--- ---	16 -74	dBrnc0 dBm0p

10.4. ANALOG INPUT AND OUTPUT AMPLIFIER PARAMETERS

V_{DD}=2.7V to 3.6V; V_{SS}=0V; T_A=-40°C to +85°C; all analog signals referred to V_{AG};

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT.
AI Input Offset Voltage	$V_{OFF,AI}$	AI+, AI-	---	---	±25	mV
AI Input Current	$I_{IN,AI}$	AI+, AI-	---	±0.1	±1.0	μA
AI Input Resistance	$R_{IN,AI}$	AI+, AI- to V_{AG}	10	---	---	MΩ
AI Input Capacitance	$C_{IN,AI}$	AI+, AI-	---	---	10	pF
AI Common Mode Input Voltage Range	$V_{CM,AI}$	AI+, AI-	1.2	---	V_{DD}-1.2	V
AI Common Mode Rejection Ratio	$CMRR_{TI}$	AI+, AI-	---	60	---	dB
AI Amp Gain Bandwidth Product	GBW_{TI}	AO, R_{LD}≥10kΩ	---	2500	---	kHz
AI Amp DC Open Loop Gain	G_{TI}	AO, R_{LD}≥10kΩ	---	95	---	dB
AI Amp Equivalent Input Noise	N_{TI}	C-Message Weighted	---	-24	---	dBrnC
AO Output Voltage Range	V_{TG}	R_{LD}=2kΩ to V_{AG}	0.4	---	V_{DD}-0.4	V
Load Resistance	R_{LDTGRO}	AO, RO to V_{AG}	2	---	---	kΩ
Load Capacitance	C_{LDTGAO}	AO	---	---	100	pF
Load Capacitance	C_{LDTGRO}	RO	---	---	200	pF
AO & RO Output Current	I_{OUT1}	0.5 ≤AO,RO-≤ V_{DD}-0.5	±1.0	---	---	mA
RO- Output Resistance	R_{RO-}	RO-, 0 to 3400Hz	---	1	---	Ω
RO- Output Offset Voltage	$V_{OFF,RO-}$	RO- to V_{AG}	---	---	±25	mV
Analog Ground Voltage	V_{AG}	Relative to V_{SS} (no load)	V_{DD}/2-0.1	V_{DD}/2	V_{DD}/2+0.1	V