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W7500P Datasheet Manual

Version 1.0.6

http://www.wiznet.co.kr

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1 Documentation conventions

1.1 Glossary

ARP	Address Resolution Protocol
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
AFC	Alternate Function Controller
ADC	Analog-to-Digital Converter
BOD	BrownOut Detection
CPU	Central Processing Unit
CRG	Clock Reset generator
DMA	Direct Memory Access
EOP	End Of Packet
EXTINT	External Interrupt
GPIO	General Purpose Input/Output
IrDA	Infrared Data Association
I/O	Input/Output
ICMP	Internet Control Message Protocol
IGMP	Internet Group Management Protocol
IPv4	Internet Protocol version 4
IRQ	interrupt request
NMI	NonMaskable Interrupt
PADCON	Pad Controller
PLL	Phase-Locked Loop
PHY	Physical Layer
PPPoE	Point-to-Point Protocol over Ethernet
POR	Power Of Reset
PWM	Pulse Width Modulator
RAM	Random Access Memory
RNG	Random number generator
SR	Status Register
SSP	Synchronous Serial Port

SYSCFG	System configuration controller
TOE	TCPIPCore Offload Engine
TTL	Transistor-Transistor Logic
TCP	Transmission Control Protocol
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
UDP	User Datagram Protocol
WOL	Wake On Lan
WDT	Watchdog Timer

1.2 Register Bit Conventions

Each register is shown with a key indicating the accessibility of the each individual bit, and the initial condition:

Key	Bit Accessibility
rw	Read/Write
r	Read Only
r0	Read as 0
r1	Read as 1
W	Write Only

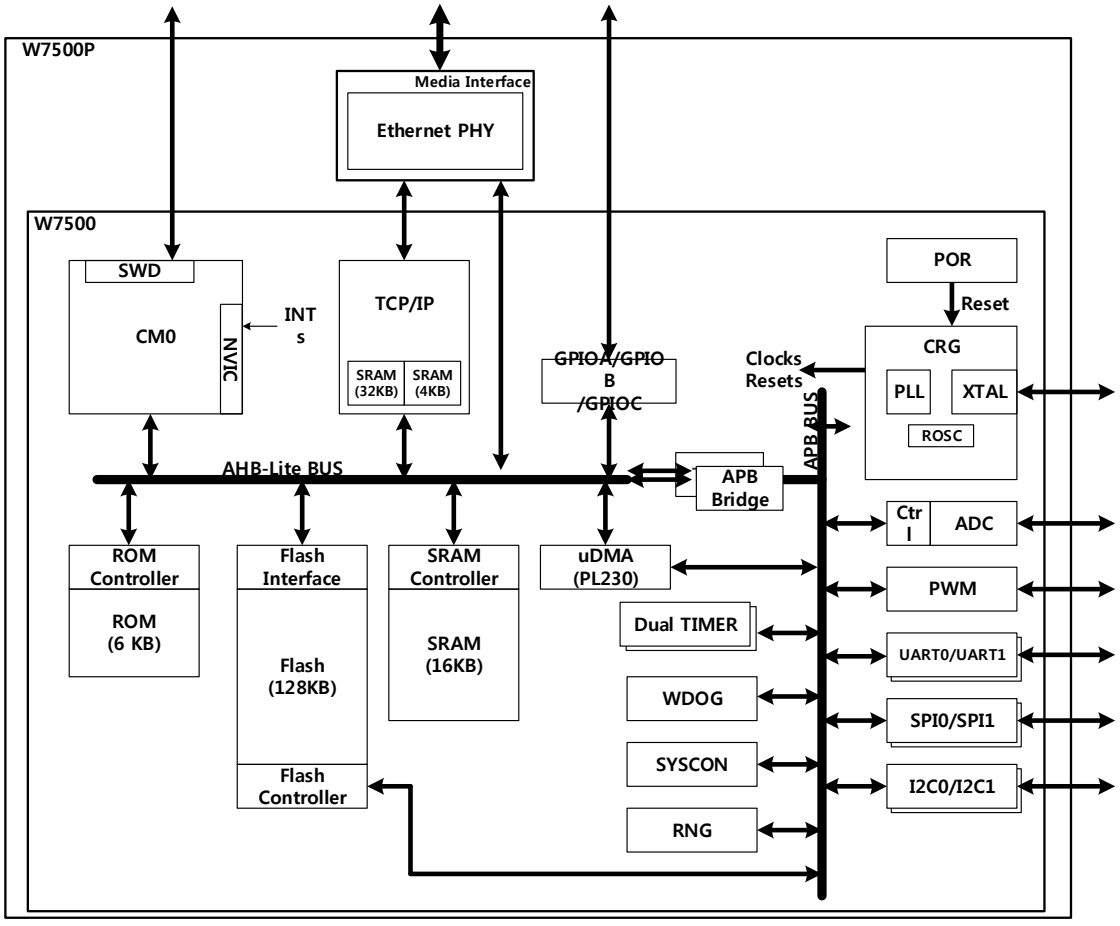
2 System and memory overview

2.1 System architecture

Main system consists of :

- Ethernet :
  - IP101G
- Two masters :
  - Cortex-M0 core
  - uDMAC (PL230, 6channel)
- Ten slaves :
  - Internal BOOT ROM
  - Internal SRAM
  - Internal Flash memory
  - Two AHB2APB bridge which connects all APB peripherals
  - Four AHB dedicated to 16bit GPIOs
  - TCPIP Hardware core

System architecture and AHB-Lite bus architecture shown in



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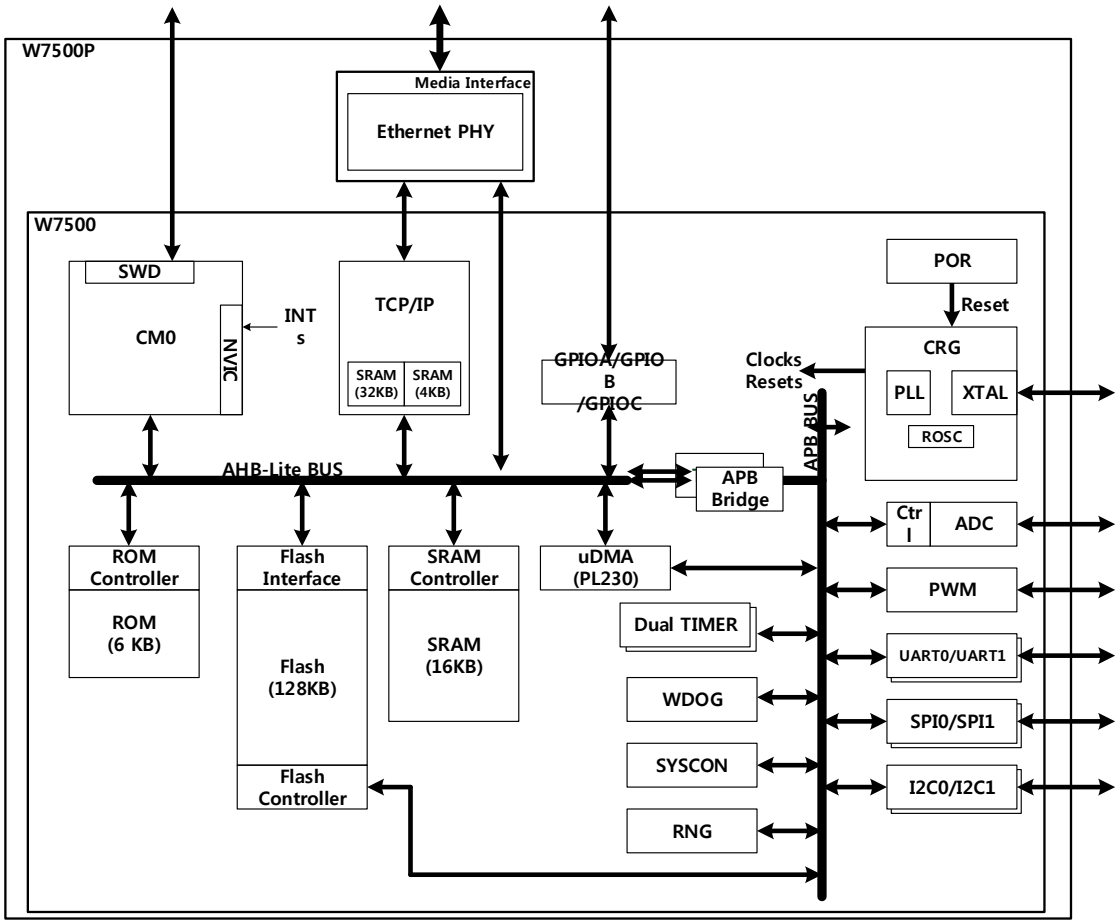

Figure 1 W7500P System Architecture

AHB-Lite BUS

- This bus connects the two masters (Cortex-M0 and uDMAC) and ten AHB slaves.

Two APB BUSs

- These buses connect Seventeen APB peripherals (Watchdog, two dual timers, pwm, two UARTs, simple UART, two I2Cs, two SSPs, random number generator, real time clock, 12bits analog digital converter, clock controller, IO configuration, PAD MUX controller)

2.2 Memory organization

2.2.1 Introduction

Program memory, data memory, registers and I/O ports are organized within the same linear 4-Gbyte address space.

The bytes are coded in memory in Little Endian format. The lowest numbered byte in a word is considered the word's least significant byte and the highest numbered byte the most significant.

2.2.2 Memory map

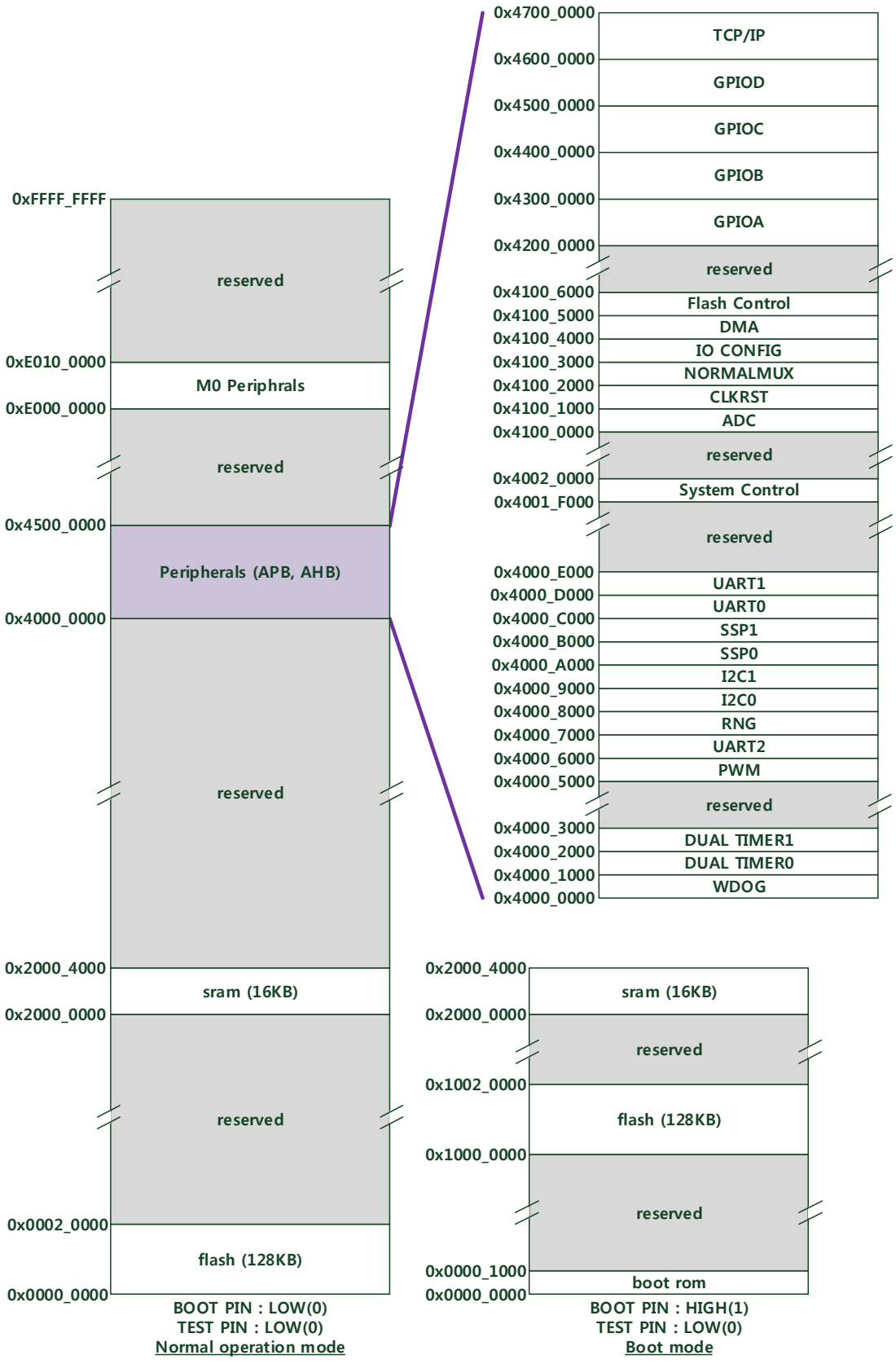

Figure 2 W7500P memory map

3 System configuration controller (SYSCFG)

3.1 Introduction

Main purposes of the system configuration controller are the following

- Control of the memory remap feature
- The ability to enable an automatic reset if the system locks up
- Information about the cause of the last reset

4 Interrupt and events

4.1 Introduction

W7500P contains interrupt service and event service as below

- 26ea interrupt request (IRQ) lines.
- One NonMaskable Interrupt (NMI).
- One event signal

4.2 Interrupt assignments

Table 1 describes the W7500P interrupt assignments.

Table 1 W7500P interrupt assignments

IRQ/NMI	Device	Description	Address
NMI	Watchdog	Watchdog interrupt	0x0000_0008
IRQ[0]	SSP0	SSP0 global interrupt	0x0000_0040
IRQ[1]	SSP1	SSP1 global interrupt	0x0000_0044
IRQ[2]	UART0	UART0 global interrupt	0x0000_0048
IRQ[3]	UART1	UART1 global interrupt	0x0000_004C
IRQ[4]	UART2	UART2 global interrupt	0x0000_0050
IRQ[5]	I2C0	I2C0 global interrupt	0x0000_0054
IRQ[6]	I2C1	I2C1 global interrupt	0x0000_0058
IRQ[7]	GPIOA	GPIOA global interrupt	0x0000_005C
IRQ[8]	GPIOB	GPIOB global interrupt	0x0000_0060
IRQ[9]	GPIOC	GPIOC global interrupt	0x0000_0064
IRQ[10]	GPIOD	GPIOD global interrupt	0x0000_0068
IRQ[11]	DMA	DMA channel 1 ~ channel 5 interrupt	0x0000_006C
IRQ[12]	Dualtimer0	Dualtimer0 global interrupt	0x0000_0070

IRQ[13]	Dualtimer1	Dualtimer1 global interrupt	0x0000_0074
IRQ[14]	PWM0	PWM0 global interrupt	0x0000_0078
IRQ[15]	PWM1	PWM1 global interrupt	0x0000_007C
IRQ[16]	PWM2	PWM2 global interrupt	0x0000_0080
IRQ[17]	PWM3	PWM3 global interrupt	0x0000_0084
IRQ[18]	PWM4	PWM4 global interrupt	0x0000_0088
IRQ[19]	PWM5	PWM5 global interrupt	0x0000_008C
IRQ[20]	PWM6	PWM6 global interrupt	0x0000_0090
IRQ[21]	PWM7	PWM7 global interrupt	0x0000_0094
IRQ[22]	reserved		0x0000_0098
IRQ[23]	ADC	ADC acquisition end interrupt	0x0000_009C
IRQ[24]	TCPIP	TCPIP global interrupt	0x0000_00A0
IRQ[25]	EXT_INT	External pin interrupt	0x0000_00A4
IRQ[26]	reserved		0x0000_00A8
IRQ[27]	reserved		0x0000_00AC
IRQ[28]	reserved		0x0000_00B0
IRQ[29]	reserved		0x0000_00B4
IRQ[30]	reserved		0x0000_00B8
IRQ[31]	reserved		0x0000_00BC

4.3 Event

W7500P is able to handle internal events in order to wake up the core(WFE). The wakeup event can be generated by

- When after DMA process finished

5 Power supply

5.1 Introduction

W7500P embeds a voltage regulator in order to supply the internal 1.5V digital power domain.

- Require a 2.7V ~ 5.5V operating supply voltage (VDD)
- ADC ref voltage is same as VDD

5.2 Voltage regulator

The voltage regulator is always enabled after Reset and works in only one mode.

- In Run mode, the regulator supplies full power to the 1.5V domain.
- There is no power down or sleep mode

5.3 Power supply supervisor

W7500P has an integrated reset (POR) circuit which is always active and ensures proper operation above a threshold of 0.6V

- The POR monitors only the VDD supply voltage. During the startup phase VDD must arrive first and be greater or equal to 0.6V

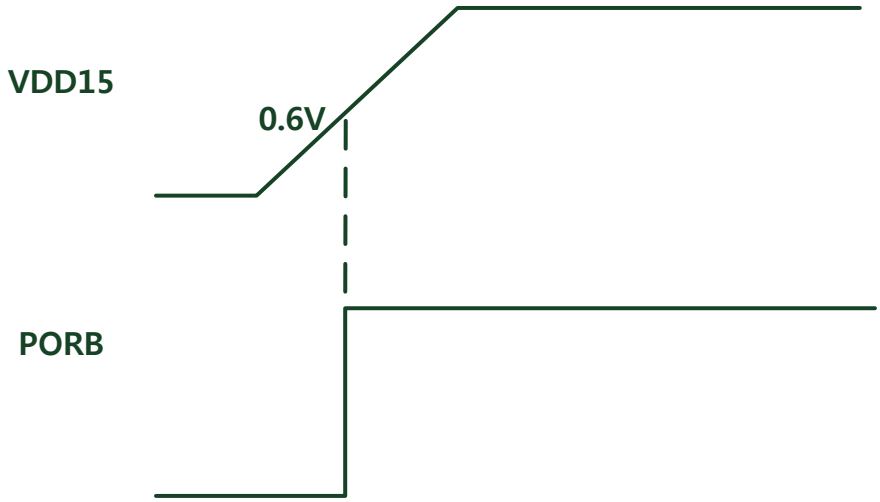

Figure 3 POR reset waveform

5.4 Low-power modes

W7500P is in RUN mode after a system or power reset. There are two low power modes to save power when the CPU does not need to be kept running. These modes are useful for instances like when the CPU is waiting for an external interrupt. Please note that there is no power-off mode for W7500P.

The device features two low-power modes:

- Sleep mode
- Deep Sleep mode

Additionally, the power consumption can be reducing by following method:

- User can slow down the system clocks
- User can gate the clocks to the peripherals when they are unused.

5.4.1 Sleep mode

W7500P has two kinds of sleep modes. One is Sleep mode and the other is Deep sleep mode.

Two of them are almost the same except the clock gated peripherals kinds. Table 2 shows the Sleep mode summary.

Table 2 W7500P sleep mode summary

Mode	Entry	Wakeup	Effect on clocks
Sleep mode	DEEPSLEEP = 0 Enable WFI	Any interrupt	CPU clock OFF APB Bus Clock ON AHB Bus clock ON Memory clocks ON
	DEEPSLEEP = 0 Enable WFE	Wakeup event	
Deep Sleep mode	DEEPSLEEP = 1 Enable WFI	Any interrupt	CPU clock OFF APB Bus Clock OFF AHB Bus clock OFF Memory clocks OFF
	DEEPSLEEP = 1 Enable WFE	Wakeup event	

5.4.2 Peripheral clock gating

In Run mode, individual clocks can be stopped at any time to reduce power.

Peripheral clock gating is controlled by the CRG block.

Below is the list of clocks which can be gating in CRG block.

- ADC clock (ADCCLK)
- SSP0, SSP1 clock (SSPCLK)
- UART0, UART1 clock (UARTCLK)
- Two Timer clocks (TIMCLK0, TIMCLK1)
- 8ea PWM clocks (PWMCLK0 ~ PWMCLK7)
- WDOG clock (WDOGCLK)
- Random number generator clock (RNGCLK)

6 System tick timer

6.1 Introduction

System tick timer(SysTick) is part of the ARM Cortex-M0 core

6.2 Features

Simple 24bit timer.

Clocked internally by the system clock or the system clock/2.

6.3 Functional description

The SysTick timer is an integral part of Cortex-M0. The SysTick timer is intended to generated a fixed 10 millisecond interrupt for use by an operating system or other system management software.

Since the SysTick timer is a part of the Cortex-M0, it facilitates porting of software by providing a standard timer that is available on Cortex-M0 based devices. The SysTick timer can be used for :

- An RTOS tick timer which fires at a programmable rate (for example 100 Hz) and invokes a SysTick routine.
- A high-speed alarm timer using the core clock.
- A simple counter. Software can use this to measure time to completion and time used.
- An internal clock source control based on missing/meeting durations. The COUNTFLAG bit-field in the control and status register can be used to determine if an action completed within a set duration, as part of a dynamic clock management control loop.

7 TCPIPCore Offload Engine (TOE)

7.1 Introduction

The TCP/IPCore Offlead Engine (TOE) is a Hardwired TCP/IP embedded Ethernet controller that provides easier Internet connection to embedded systems. TOE enables users to have Internet connectivity in their applications by using the TCP/IP stack.

WIZnet's Hardwired TCP/IP is the market-proven technology that supports TCP, UDP, IPv4, ICMP, ARP, IGMP, and PPPoE protocols. TOE embeds the 32Kbyte internal memory buffer for the Ethernet packet processing. Using TOE allows users to implement the Ethernet application by adding the simple socket program. It's faster and easier than using any other Embedded Ethernet solutions. 8 independent hardware sockets can be used simultaneously.

TOE also provides WOL (Wake on LAN) to reduce power consumption of the system.

7.2 Features

- Supports Hardwired TCP/IP Protocols : TCP, UDP, ICMP, IPv4, ARP, IGMP, PPPoE
- Supports 8 independent sockets simultaneously
- Supports Power down mode
- Supports Wake on LAN over UDP
- Internal 32Kbytes Memory for TX/RX Buffers
- Not supports IP Fragmentation

7.3 Functional description

Figure 4 shows the TOE block diagram.

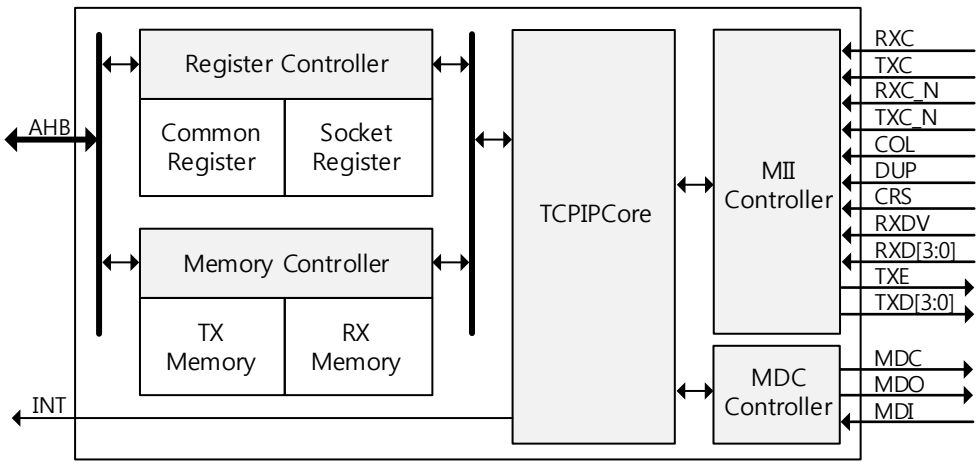

Figure 4 TOE block diagram

7.4 TOE Memory map

TOE has one Common Register Block, eight Socket Register Blocks, and TX/RX Buffer Blocks allocated to each Socket. Figure 5 shows the selected block by the base address and the available offset address range of Socket TX/RX Buffer Blocks. Each Socket's TX Buffer Block physically exists in one 16KB TX memory and is initially allocated with 2KB. Also, Each Socket's RX Buffer Block physically exists in one 16KB RX Memory and is initially allocated with 2KB.

Regardless of the allocated size of each Socket TX/RX Buffer, it can be accessible within the 16 bits offset address range (From 0x0000 to 0xFFFF).

Refer to 'Chapter 7.4.3' for more information about 16KB TX/RX Memory organization and access method.

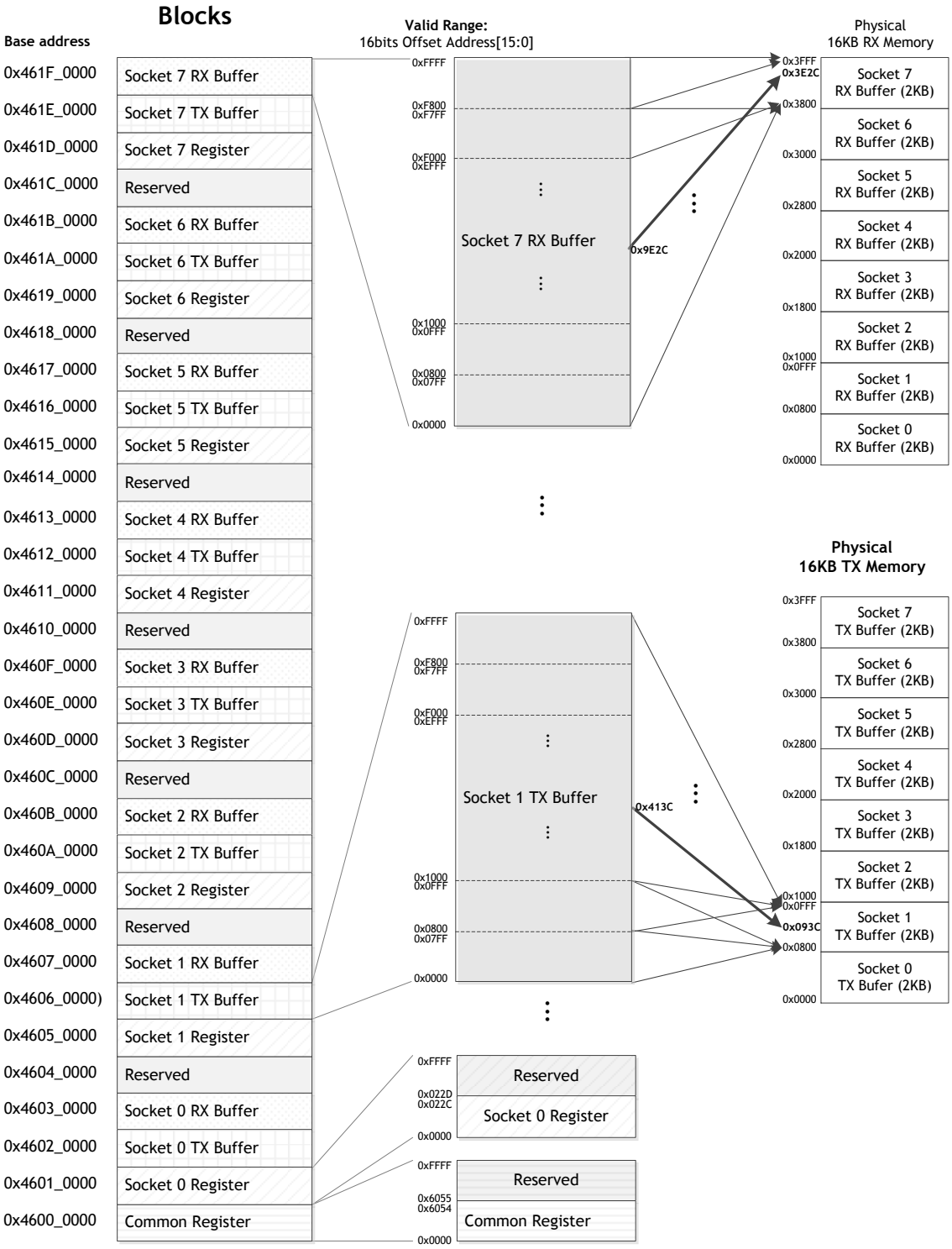

Figure 5. Register & Memory Organization