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## 8-BIT MICROCONTROLLER

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## 1 GENERAL DESCRIPTION

The W78E054D/W78E052D/W78E051D series is an 8-bit microcontroller which can accommodate a wider frequency range with low power consumption. The instruction set for the W78E054D/W78E052D/ W78E051D series is fully compatible with the standard 8052.

The W78E054D/W78E052D/W78E051D series contains 16K/8K/4K bytes Flash EPROM programmable by hardware writer; a 256 bytes RAM; four 8-bit bi-directional (P0, P1, P2, P3) and bit-addressable I/O ports; an additional 4-bit I/O port P4; three 16-bit timer/counters; a hardware watchdog timer and a serial port. These peripherals are supported by 8 sources 4-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W78E054D/W78E052D/W78E051D series allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

The W78E054D/W78E052D/W78E051D series microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor. The W78E054D/W78E052D/W78E051D series contains In-System Programmable (ISP) 2KB LDROM for loader program, operating voltage from 3.3V to 5.5V.

**Note:** If the applied  $V_{DD}$  is not stable, especially with long transition time of power on/off, it's recommended to apply an external RESET IC to the RST pin for improving the stability of system.



## 2 FEATURES

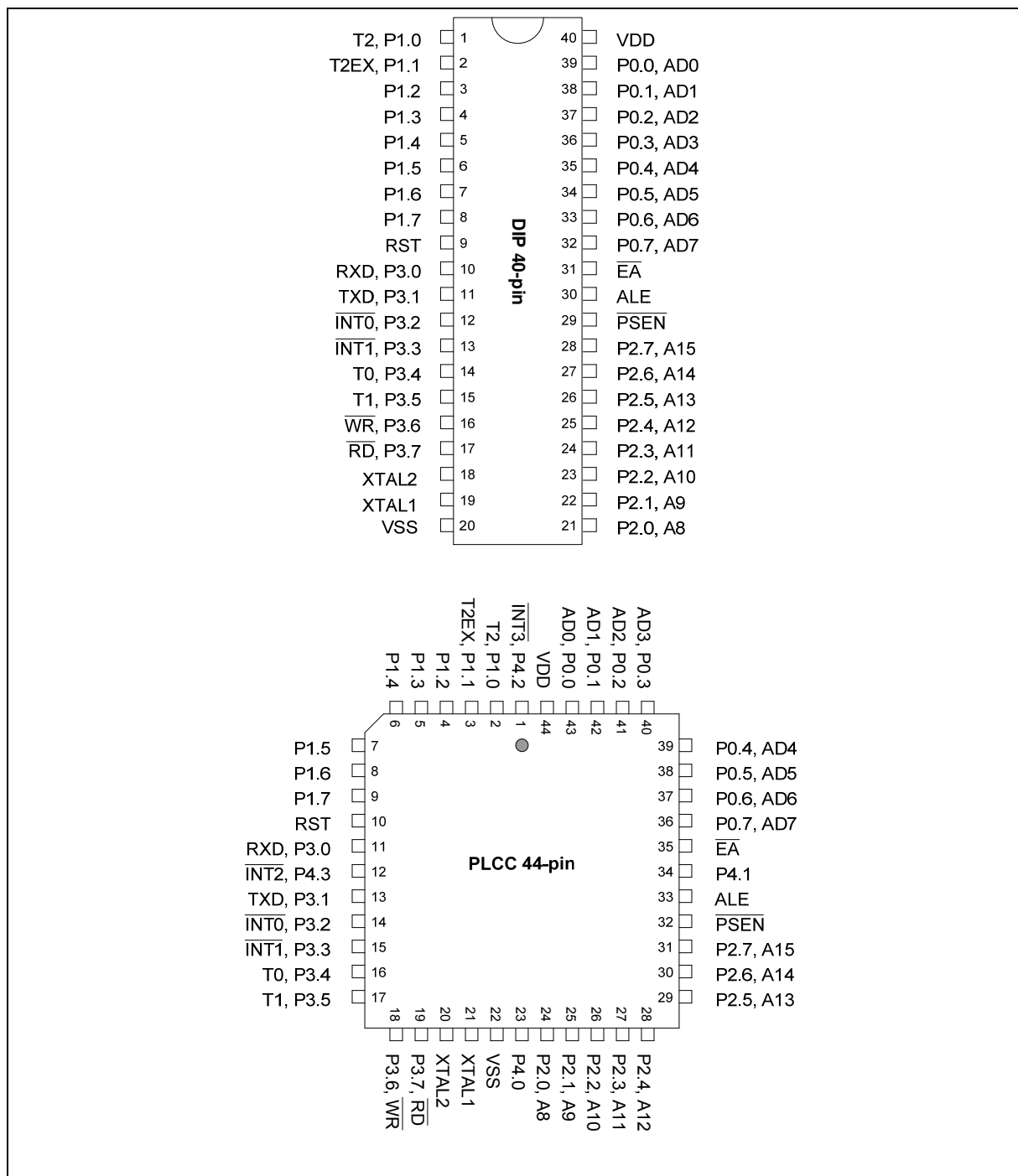
- Fully static design 8-bit CMOS microcontroller
- Optional 12T or 6T mode
  - 12T Mode, 12 clocks per machine cycle operation (default), Speed up to 40 MHz/5V
  - 6T Mode, 6 clocks per machine cycle operation set by the writer, Speed up to 20 MHz/5V
- Wide supply voltage of 2.4V to 5.5V
- Temperature grade is (-40°C~85°C)
- Pin and Instruction-sets compatible with MCS-51
- 256 bytes of on-chip scratchpad RAM
- 16K/8K/4K bytes electrically erasable/programmable Flash EPROM
- 2K bytes LDRAM support ISP function (Reference Application Note)
- 64KB program memory address space
- 64KB data memory address space
- Four 8-bit bi-directional ports
- 8-sources, 4-level interrupt capability
- One extra 4-bit bit-addressable I/O port, additional  $\overline{\text{INT2}} / \overline{\text{INT3}}$  (available on PQFP, PLCC and LQFP package)
- Three 16-bit timer/counters
- One full duplex serial port
- Watchdog Timer
- EMI reduction mode
- Software Reset
- Built-in power management with idle mode and power down mode
- Code protection
- Packages: DIP40, PLCC44, PQFP44, LQFP48

### 3 PARTS INFORMATION LIST

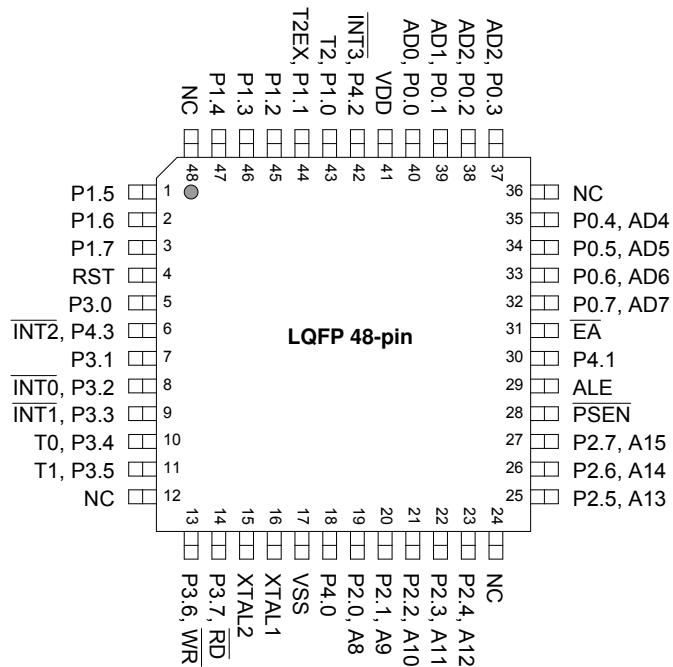
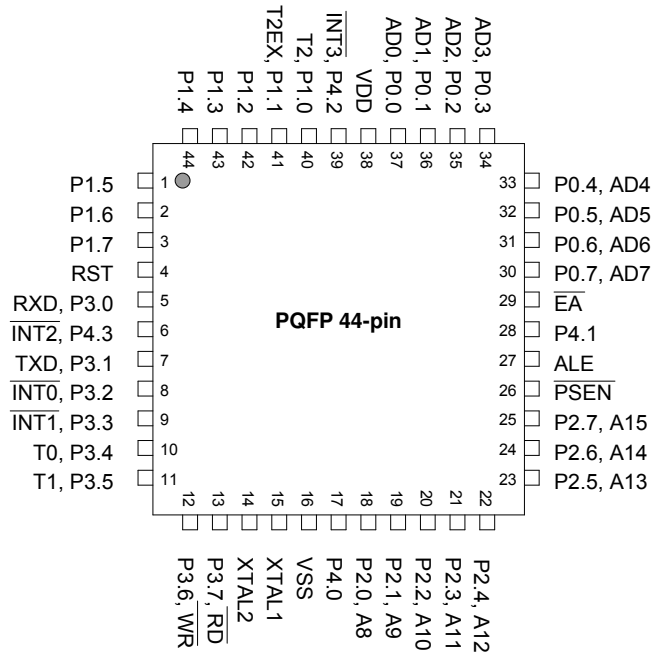
| PART NO.   | RAM          | LDROM<br>SIZE | APROM<br>SIZE | PACKAGE     | Temperature<br>grade |
|------------|--------------|---------------|---------------|-------------|----------------------|
| W78E054DDG | 256<br>Bytes | 2K Bytes      | 14K Bytes     | DIP-40 Pin  | -40°C~85°C           |
|            |              | 0             | 16K Bytes     |             |                      |
| W78E054DPG |              | 2K Bytes      | 14K Bytes     | PLCC-44 Pin | -40°C~85°C           |
|            |              | 0             | 16K Bytes     |             |                      |
| W78E054DFG |              | 2K Bytes      | 14K Bytes     | PQFP-44 Pin | -40°C~85°C           |
|            |              | 0             | 16K Bytes     |             |                      |
| W78E054DLG |              | 2K Bytes      | 14K Bytes     | LQFP-48 Pin | -40°C~85°C           |
|            |              | 0             | 16K Bytes     |             |                      |
| W78E052DDG |              | 2K Bytes      | 8K Bytes      | DIP-40 Pin  | -40°C~85°C           |
| W78E052DPG |              |               |               | PLCC-44 Pin | -40°C~85°C           |
| W78E052DFG |              |               |               | PQFP-44 Pin | -40°C~85°C           |
| W78E052DLG |              |               |               | LQFP-48 Pin | -40°C~85°C           |
| W78E051DDG |              | 2K Bytes      | 4K Bytes      | DIP-40 Pin  | -40°C~85°C           |
| W78E051DPG |              |               |               | PLCC-44 Pin | -40°C~85°C           |
| W78E051DFG |              |               |               | PQFP-44 Pin | -40°C~85°C           |
| W78E051DLG |              |               |               | LQFP-48 Pin | -40°C~85°C           |

Table 3-1: Lead Free (RoHS) Parts information list

#### 4 PIN CONFIGURATIONS









## 5 PIN DESCRIPTIONS

| SYMBOL            | TYPE  | DESCRIPTIONS                                                                                                                                                                                                                                                                                                                |
|-------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $\overline{EA}$   | I     | EXTERNAL ACCESS ENABLE: This pin forces the processor to execute out of external ROM. It should be kept high to access internal ROM. The ROM address and data will not be present on the bus if $\overline{EA}$ pin is high and the program counter is within internal ROM area. Otherwise they will be present on the bus. |
| $\overline{PSEN}$ | O H   | PROGRAM STORE ENABLE: $\overline{PSEN}$ enables the external ROM data onto the Port 0 address/data bus during fetch and MOVC operations. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs from this pin.                                                                                   |
| ALE               | O H   | ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0.                                                                                                                                                                                                           |
| RST               | I L   | RESET: A high on this pin for two machine cycles while the oscillator is running resets the device.                                                                                                                                                                                                                         |
| XTAL1             | I     | CRYSTAL1: This is the crystal oscillator input. This pin may be driven by an external clock.                                                                                                                                                                                                                                |
| XTAL2             | O     | CRYSTAL2: This is the crystal oscillator output. It is the inversion of XTAL1.                                                                                                                                                                                                                                              |
| VSS               | I     | GROUND: Ground potential                                                                                                                                                                                                                                                                                                    |
| VDD               | I     | POWER SUPPLY: Supply voltage for operation.                                                                                                                                                                                                                                                                                 |
| P0.0–P0.7         | I/O D | PORT 0: Port 0 is an open-drain bi-directional I/O port. This port also provides a multiplexed low order address/data bus during accesses to external memory.                                                                                                                                                               |
| P1.0–P1.7         | I/O H | PORT 1: Port 1 is a bi-directional I/O port with internal pull-ups. The bits have alternate functions which are described below:<br>T2 (P1.0): Timer/Counter 2 external count input<br>T2EX (P1.1): Timer/Counter 2 Reload/Capture control                                                                                  |
| P2.0–P2.7         | I/O H | PORT 2: Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.                                                                                                                                                                         |

## Pin Description, continued

| SYMBOL    | TYPE  | DESCRIPTIONS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-----------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| P3.0–P3.7 | I/O H | PORT 3: Port 3 is a bi-directional I/O port with internal pull-ups. All bits have alternate functions, which are described below:<br>RXD (P3.0): Serial Port 0 input<br>TXD (P3.1): Serial Port 0 output<br>$\overline{\text{INT0}}$ (P3.2) : External Interrupt 0<br>$\overline{\text{INT1}}$ (P3.3) : External Interrupt 1<br>T0 (P3.4) : Timer 0 External Input<br>T1 (P3.5) : Timer 1 External Input<br>$\overline{\text{WR}}$ (P3.6) : External Data Memory Write Strobe<br>$\overline{\text{RD}}$ (P3.7) : External Data Memory Read Strobe |
| P4.0–P4.3 | I/O H | PORT 4: Another bit-addressable bidirectional I/O port P4. P4.3 and P4.2 are alternative function pins. It can be used as general I/O port or external interrupt input sources ( $\overline{\text{INT2}}$ / $\overline{\text{INT3}}$ ).                                                                                                                                                                                                                                                                                                           |

\* Note: TYPE I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain.

**In application if MCU pins need external pull-up, it is recommended to add a pull-up resistor (10K $\Omega$ ) between pin and power ( $V_{DD}$ ) instead of directly wiring pin to  $V_{DD}$  for enhancing EMC.**

## 6 BLOCK DIAGRAM

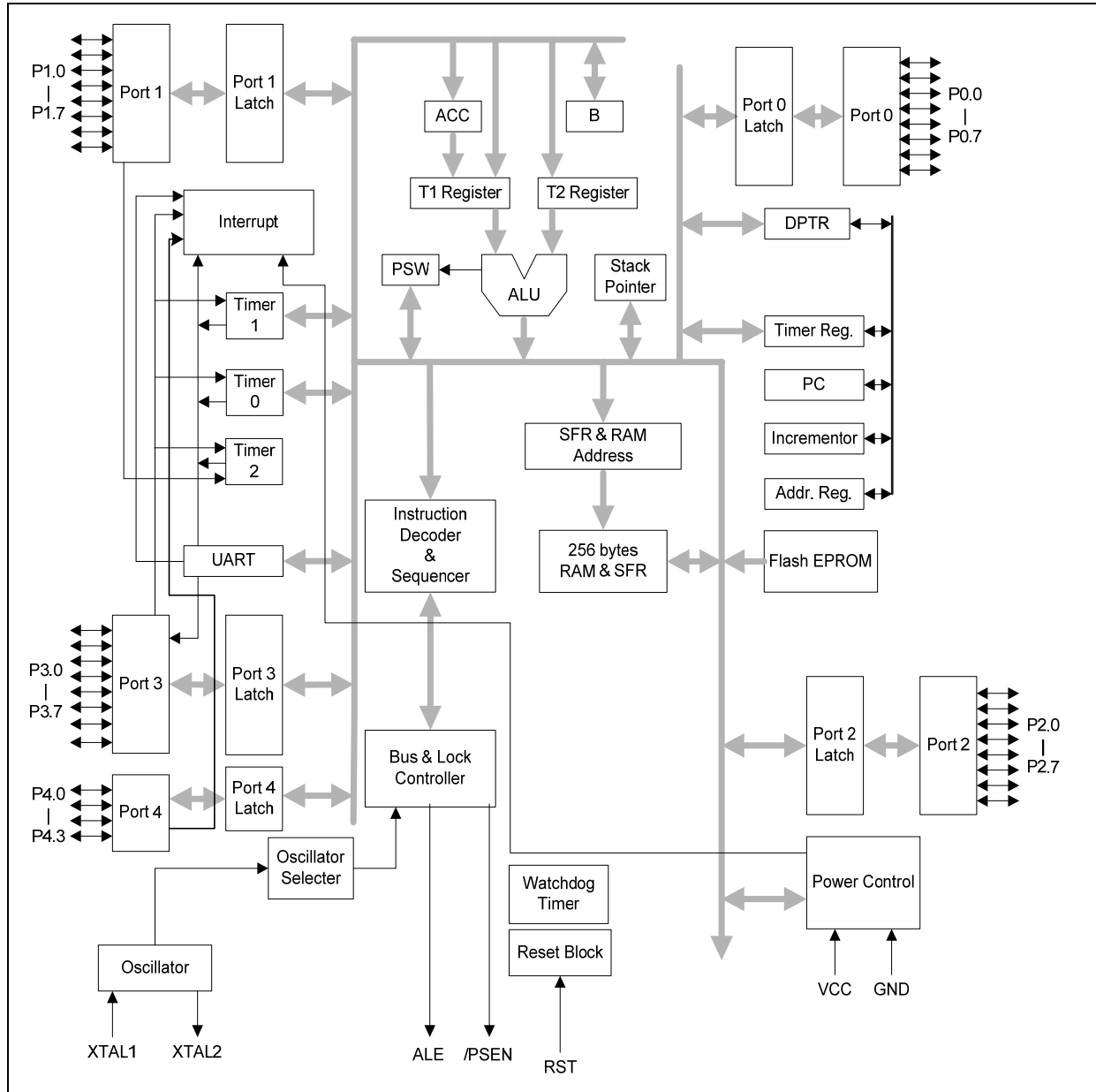


Figure 6-1 W78E054D/W78E052D/W78E051D Block Diagram



## 7 FUNCTIONAL DESCRIPTION

The W78E054D/W78E052D/W78E051D series architecture consists of a core controller surrounded by various registers, five general purpose I/O ports, 16K/8K/4K flash EPROM, 2K FLASH EPROM for ISP function, 256 bytes of RAM, three timer/counters, and a serial port. The processor supports 111 different op-codes and references both a 64K program address space and a 64K data storage space.

### 7.1 On-Chip Flash EPROM

The W78E054D/W78E052D/W78E051D series include one 16K/8K/4K bytes of main Flash EPROM for application program.

### 7.2 I/O Ports

The W78E054D/W78E052D/W78E051D series has four 8-bit ports and one extra 4-bit port. Port 0 can be used as an Address/Data bus when external program is running or external memory/device is accessed by MOVC or MOVX instruction. In these cases, it has strong pull-ups and pull-downs, and does not need any external pull-ups. Otherwise it can be used as a general I/O port with open-drain circuit. Port 2 is used chiefly as the upper 8-bits of the Address bus when port 0 is used as an address/data bus. It also has strong pull-ups and pull-downs when it serves as an address bus. Port 1 and 3 act as I/O ports with alternate functions. Port 4 is only available on PLCC/PQFP/LQFP package type. It serves as a general purpose I/O port as Port 1 and Port 3. Another bit-addressable bidirectional I/O port P4. P4.3 and P4.2 are alternative function pins. It can be used as general I/O port or external interrupt input sources (INT2 / INT3 ).

### 7.3 Serial I/O

The W78E054D/W78E052D/W78E051D series have one serial port that is functionally similar to the serial port of the original 8032 family. However the serial port on the W78E054D/ W78E052D/ W78E051D series can operate in different modes in order to obtain timing similarity as well.

### 7.4 Timers

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for timers 0 and 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as reload/capture registers for Timer 2.

The operations of Timer 0 and Timer 1 are the same as in the 8051 CPU. Timer 2 is a special feature of the W78E054D/W78E052D/W78E051D: it is a 16-bit timer/counter that is configured and controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed at capture or auto-reload mode is the same as that of Timers 0 and 1.

### 7.5 Interrupts

The Interrupt structure in the W78E054D/W78E052D/W78E051D is slightly different from that of the standard 8052. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased. The W78E054D/W78E052D/W78E051D provides 8 interrupt resources with four priority level, including four external interrupt sources, three timer interrupts, serial I/O interrupts.



## **7.6 Data Pointers**

The data pointer of W78E054D/W78E052D/W78E051D series is same as standard 8052 that have one 16-bit Data Pointer (DPTR).

## **7.7 Architecture**

The W78E054D/W78E052D/W78E051D series are based on the standard 8052 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard 8052 instruction set.

### **7.7.1 ALU**

The ALU is the heart of the W78E054D/W78E052D/W78E051D series. It is responsible for the arithmetic and logical functions. It is also used in decision making, in case of jump instructions, and is also used in calculating jump addresses. The user cannot directly use the ALU, but the Instruction Decoder reads the op-code, decodes it, and sequences the data through the ALU and its associated registers to generate the required result. The ALU mainly uses the ACC which is a special function register (SFR) on the chip. Another SFR, namely B register is also used Multiply and Divide instructions. The ALU generates several status signals which are stored in the Program Status Word register (PSW).

### **7.7.2 Accumulator**

The Accumulator (ACC) is the primary register used in arithmetic, logical and data transfer operations in the W78E054D/W78E052D/W78E051D series. Since the Accumulator is directly accessible by the CPU, most of the high speed instructions make use of the ACC as one argument.

### **7.7.3 B Register**

This is an 8-bit register that is used as the second argument in the MUL and DIV instructions. For all other instructions it can be used simply as a general purpose register.

### **7.7.4 Program Status Word**

This is an 8-bit SFR that is used to store the status bits of the ALU. It holds the Carry flag, the Auxiliary Carry flag, General purpose flags, the Register Bank Select, the Overflow flag, and the Parity flag.

### **7.7.5 Scratch-pad RAM**

The W78E054D/W78E052D/W78E051D series has a 256 byte on-chip scratch-pad RAM. This can be used by the user for temporary storage during program execution. A certain section of this RAM is bit addressable, and can be directly addressed for this purpose.

### **7.7.6 Stack Pointer**

The W78E054D/W78E052D/W78E051D series has an 8-bit Stack Pointer which points to the top of the Stack. This stack resides in the Scratch Pad RAM in the W78E054D/W78E052D/W78E051D. Hence the size of the stack is limited by the size of this RAM.



## 8 MEMORY ORGANIZATION

The W78E054D/W78E052D/W78E051D series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

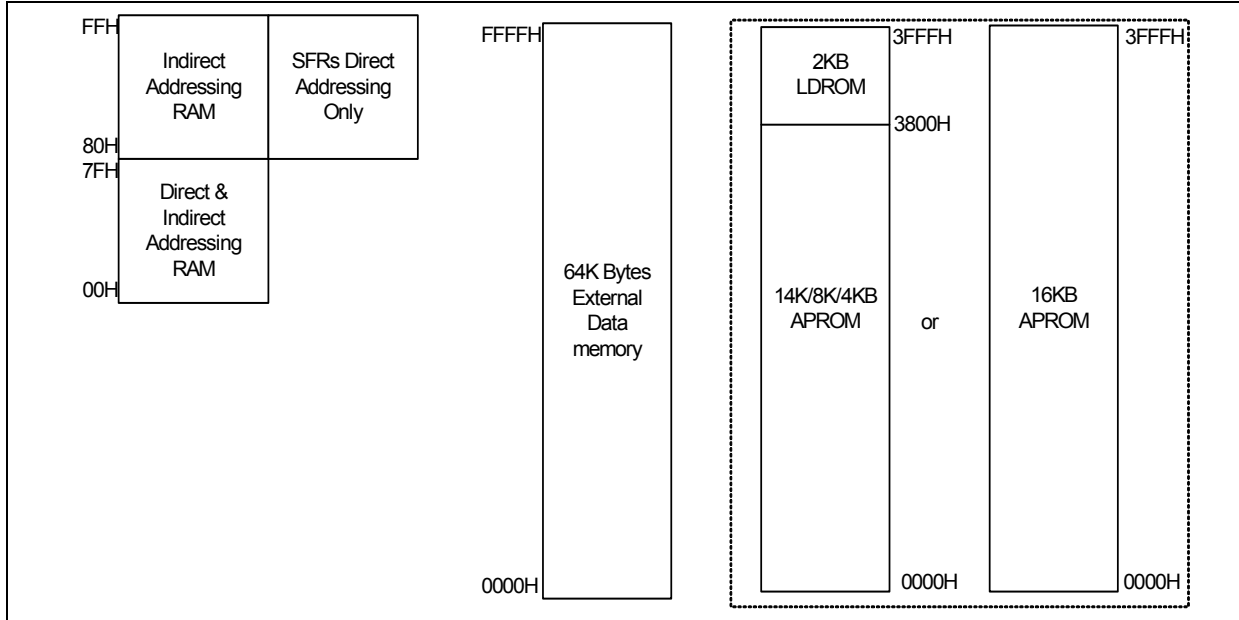


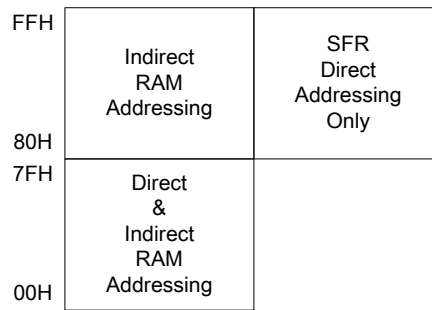
Figure 8-1 Memory Map

### 8.1 Program Memory (on-chip Flash)

The Program Memory on the W78E054D/W78E052D/W78E051D series can be up to 16K/8K/4K bytes (2K bytes for ISP F/W, share with the W78E054D) long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

### 8.2 Scratch-pad RAM and Register Map

As mentioned before the W78E054D/W78E052D/W78E051D series have separate Program and Data Memory areas. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.



256 bytes RAM and SFR Data Memory Space

Figure 8–2 W78E054D/W78E052D/W78E051D RAM and SFR Memory Map

Since the scratch-pad RAM is only 256bytes it can be used only when data contents are small. There are several other special purpose areas within the scratch-pad RAM. These are illustrated in next figure.

|            |              |    |    |    |    |    |    |    |
|------------|--------------|----|----|----|----|----|----|----|
| FFH        | Indirect RAM |    |    |    |    |    |    |    |
| 80H<br>7FH |              |    |    |    |    |    |    |    |
|            | Direct RAM   |    |    |    |    |    |    |    |
| 30H<br>2FH |              |    |    |    |    |    |    |    |
|            | 7F           | 7E | 7D | 7C | 7B | 7A | 79 | 78 |
| 2EH        | 77           | 76 | 75 | 74 | 73 | 72 | 71 | 70 |
| 2DH        | 6F           | 6E | 6D | 6C | 6B | 6A | 69 | 68 |
| 2CH        | 67           | 66 | 65 | 64 | 63 | 62 | 61 | 60 |
| 2BH        | 5F           | 5E | 5D | 5C | 5B | 5A | 59 | 58 |
| 2AH        | 57           | 56 | 55 | 54 | 53 | 52 | 51 | 50 |
| 29H        | 4F           | 4E | 4D | 4C | 4B | 4A | 49 | 48 |
| 28H        | 47           | 46 | 45 | 44 | 43 | 42 | 41 | 40 |
| 27H        | 3F           | 3E | 3D | 3C | 3B | 3A | 39 | 38 |
| 26H        | 37           | 36 | 35 | 34 | 33 | 32 | 31 | 30 |
| 25H        | 2F           | 2E | 2D | 2C | 2B | 2A | 29 | 28 |
| 24H        | 27           | 26 | 25 | 24 | 23 | 22 | 21 | 20 |
| 23H        | 1F           | 1E | 1D | 1C | 1B | 1A | 19 | 18 |
| 22H        | 17           | 16 | 15 | 14 | 13 | 12 | 11 | 10 |
| 21H        | 0F           | 0E | 0D | 0C | 0B | 0A | 09 | 08 |
| 20H        | 07           | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
| 1FH        | Bank 3       |    |    |    |    |    |    |    |
| 18H<br>17H |              |    |    |    |    |    |    |    |
|            | Bank 2       |    |    |    |    |    |    |    |
| 10H<br>0FH |              |    |    |    |    |    |    |    |
|            | Bank 1       |    |    |    |    |    |    |    |
| 08H<br>07H |              |    |    |    |    |    |    |    |
|            | Bank 0       |    |    |    |    |    |    |    |
| 00H        |              |    |    |    |    |    |    |    |

Figure 8–3 Scratch-pad RAM

### 8.2.1 Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed as Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at one time the W78E054D/W78E052D/W78E051D series can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.



### 8.2.2 Bit addressable Locations

The Scratch-pad RAM area from location 20h to 2Fh is byte as well as bit addressable. This means that a bit in this area can be individually addressed. In addition some of the SFRs are also bit addressable. The instruction decoder is able to distinguish a bit access from a byte access by the type of the instruction itself. In the SFR area, any existing SFR whose address ends in a 0 or 8 is bit addressable.

### 8.2.3 Stack

The scratch-pad RAM can be used for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a jump, call or interrupt is invoked the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07h at reset. The user can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, and then the SP is decreased.

## 9 SPECIAL FUNCTION REGISTERS

The W78E054D/W78E052D/W78E051D series uses Special Function Registers (SFRs) to control and monitor peripherals and their Modes. The SFRs reside in the register locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where users wish to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. The W78E054D/W78E052D/W78E051D series contain all the SFRs present in the standard 8052. However some additional SFRs are added. In some cases the unused bits in the original 8052, have been given new functions. The list of the SFRs is as follows.

|    |       |       |        |        |       |       |        |        |    |
|----|-------|-------|--------|--------|-------|-------|--------|--------|----|
| F8 |       |       |        |        |       |       |        |        | FF |
| F0 | B     |       |        |        |       |       |        |        | F7 |
| E8 |       |       |        |        |       |       |        |        | EF |
| E0 | ACC   |       |        |        |       |       |        |        | E7 |
| D8 | P4    |       |        |        |       |       |        |        | DF |
| D0 | PSW   |       |        |        |       |       |        |        | D7 |
| C8 | T2CON | T2MOD | RCAP2L | RCAP2H | TL2   | TH2   |        |        | CF |
| C0 | XICON |       |        |        | SFRAL | SFRAH | SFRRD  | SFRCN  | C7 |
| B8 | IP    |       |        |        |       |       | EAPAGE | CHPCON | BF |
| B0 | P3    |       |        |        |       |       |        | IPH    | B7 |
| A8 | IE    |       |        |        |       |       |        |        | AF |
| A0 | P2    |       |        |        |       |       |        |        | A7 |
| 98 | SCON  | SBUF  |        |        |       |       |        |        | 9F |
| 90 | P1    |       |        |        |       |       |        |        | 97 |
| 88 | TCON  | TMOD  | TL0    | TL1    | TH0   | TH1   | AUXR   | WDTC   | 8F |
| 80 | P0    | SP    | DPL    | DPH    |       |       | P0UPR  | PCON   | 87 |

Table 9–1: Special Function Register Location Table

Note:

1. The SFRs in the column with dark borders are bit-addressable
2. The table is condensed with eight locations per row. Empty locations indicate that these are no registers at these addresses. When a bit or register is not implemented, it will read high.



Special Function Registers:

| SYMBOL | DEFINITION                       | ADDRESS | MSB            | BIT ADDRESS, SYMBOL |              |              |               |              |              |                | LSB  | RESET      |
|--------|----------------------------------|---------|----------------|---------------------|--------------|--------------|---------------|--------------|--------------|----------------|------|------------|
| B      | B register                       | F0H     | (F7)           | (F6)                | (F5)         | (F4)         | (F3)          | (F2)         | (F1)         | (F0)           |      | 0000 0000B |
| ACC    | Accumulator                      | E0H     | (E7)           | (E6)                | (E5)         | (E4)         | (E3)          | (E2)         | (E1)         | (E0)           |      | 0000 0000B |
| P4     | Port 4                           | D8H     |                |                     |              |              | INT2          | INT3         |              |                |      | 0000 1111B |
| PSW    | Program status word              | D0H     | (D7)<br>CY     | (D6)<br>AC          | (D5)<br>F0   | (D4)<br>RS1  | (D3)<br>RS0   | (D2)<br>OV   | (D1)<br>F1   | (D0)<br>P      |      | 0000 0000B |
| TH2    | T2 reg. high                     | CDH     |                |                     |              |              |               |              |              |                |      | 0000 0000B |
| TL2    | T2 reg. low                      | CCH     |                |                     |              |              |               |              |              |                |      | 0000 0000B |
| RCAP2H | T2 capture low                   | CBH     |                |                     |              |              |               |              |              |                |      | 0000 0000B |
| RCAP2L | T2 capture high                  | CAH     |                |                     |              |              |               |              |              |                |      | 0000 0000B |
| T2MOD  | Timer 2 Mode                     | C9      |                |                     |              |              |               |              |              |                | DCEN | 0000 0000B |
| T2CON  | Timer 2 control                  | C8H     | (CF)<br>TF2    | (CE)<br>EXF2        | (CD)<br>RCLK | (CC)<br>TCLK | (CB)<br>EXEN2 | (CA)<br>TR2  | (C9)<br>C/T2 | (C8)<br>CP/RL2 |      | 0000 0000B |
| SFRCN  | SFR program of control           | C7H     |                |                     | NOE          | NCE          | CTRL3         | CTRL2        | CTRL1        | CTRL0          |      | 0000 0000B |
| SFRRD  | SFR program of data register     | C6H     |                |                     |              |              |               |              |              |                |      | 0000 0000B |
| SFRAH  | SFR program of address high byte | C5H     |                |                     |              |              |               |              |              |                |      | 0000 0000B |
| SFRAL  | SFR program of address low byte  | C4H     |                |                     |              |              |               |              |              |                |      | 0000 0000B |
| XICON  | External interrupt control       | C0H     | PX3            | EX3                 | IE3          | IT3          | PX2           | EX2          | IE2          | IT2            |      | 0000 0000B |
| CHPCON | Chip control                     | BFH     | SWRST          | -                   |              | -            | -             | -            | FBOOTS<br>L  | ENP            |      | 0000 0000B |
| EAPAGE | Erase page operation modes       | BEH     |                |                     |              |              |               |              | EAPG1        | EAPG0          |      | 0000 0000B |
| IP     | Interrupt priority               | B8H     | (BF)<br>-      | (BE)<br>-           | (BD)<br>PT2  | (BC)<br>PS   | (BB)<br>PT1   | (BA)<br>PX1  | (B9)<br>PT0  | (B8)<br>PX0    |      | 1100 0000B |
| IPH    | Interrupt priority High          | B7H     |                |                     |              |              |               |              |              |                |      | 0000 0000B |
| P3     | Port 3                           | B0H     | (B7)<br>RD     | (B6)<br>WR          | (B5)<br>T1   | (B4)<br>T0   | (B3)<br>INT1  | (B2)<br>INT0 | (B1)<br>TXD  | (B0)<br>RXD    |      | 1111 1111B |
| IE     | Interrupt enable                 | A8H     | (AF)<br>EA     | (AE)<br>-           | (AD)<br>ET2  | (AC)<br>ES   | (AB)<br>ET1   | (AA)<br>EX1  | (A9)<br>ET0  | (A8)<br>EX0    |      | 0100 0000B |
| P2     | Port 2                           | A0H     | (A7)<br>A15    | (A6)<br>A14         | (A5)<br>A13  | (A4)<br>A12  | (A3)<br>A11   | (A2)<br>A10  | (A1)<br>A9   | (A0)<br>A8     |      | 1111 1111B |
| SBUF   | Serial buffer                    | 99H     |                |                     |              |              |               |              |              |                |      | 0000 0000B |
| SCON   | Serial control                   | 98H     | (9F)<br>SM0/FE | (9E)<br>SM1         | (9D)<br>SM2  | (9C)<br>REN  | (9B)<br>TB8   | (9A)<br>RB8  | (99)<br>TI   | (98)<br>RI     |      | 0000 0000B |
| P1     | Port 1                           | 90H     | (97)           | (96)                | (95)         | (94)         | (93)          | (92)         | (91)<br>T2EX | (90)<br>T2     |      | 1111 1111B |
| WDTC   | Watchdog control                 | 8FH     | ENW            | CLRW                | WIDL         | -            | -             | PS2          | PS1          | PS0            |      | 0000 0000B |
| AUXR   | Auxiliary                        | 8EH     | -              | -                   | -            | -            |               |              |              | ALEOFF         |      | 0000 0110B |
| TH1    | Timer high 1                     | 8DH     |                |                     |              |              |               |              |              |                |      | 0000 0000B |
| TH0    | Timer high 0                     | 8CH     |                |                     |              |              |               |              |              |                |      | 0000 0000B |
| TL1    | Timer low 1                      | 8BH     |                |                     |              |              |               |              |              |                |      | 0000 0000B |
| TL0    | Timer low 0                      | 8AH     |                |                     |              |              |               |              |              |                |      | 0000 0000B |
| TMOD   | Timer mode                       | 89H     | GATE           | C/T                 | M1           | M0           | GATE          | C/T          | M1           | M0             |      | 0000 0000B |
| TCON   | Timer control                    | 88H     | (8F)<br>TF1    | (8E)<br>TR1         | (8D)<br>TF0  | (8C)<br>TR0  | (8B)<br>IE1   | (8A)<br>IT1  | (89)<br>IE0  | (88)<br>IT0    |      | 0000 0000B |
| PCON   | Power control                    | 87H     | SMOD           | SMOD0               | -            | POR          | GF1           | GF0          | PD           | IDL            |      | 0011 0000B |
| P0UPR  | Port 0 pull up option Register   | 86H     | -              | -                   | -            | -            | -             | -            | -            | P0UP           |      | 0000 0001B |
| DPH    | Data pointer high                | 83H     |                |                     |              |              |               |              |              |                |      | 0000 0000B |





|     |                  |     |      |      |      |      |      |      |      |      |            |
|-----|------------------|-----|------|------|------|------|------|------|------|------|------------|
| DPL | Data pointer low | 82H |      |      |      |      |      |      |      |      | 0000 0000B |
| SP  | Stack pointer    | 81H |      |      |      |      |      |      |      |      | 0000 0111B |
| P0  | Port 0           | 80H | (87) | (86) | (85) | (84) | (83) | (82) | (81) | (80) | 1111 1111B |

## 9.1 SFR Detail Bit Descriptions

### Port 0

|      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|
| Bit: | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|      | P0.7 | P0.6 | P0.5 | P0.4 | P0.3 | P0.2 | P0.1 | P0.0 |

Mnemonic: P0

Address: 80h

| BIT | NAME     | FUNCTION                                                                                                                                                                                                                                                                          |
|-----|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-0 | P0.[7:0] | Port 0 is an open-drain bi-directional I/O port if SFR P0UPR.0 (bit P0UP) clear to "0", and when SFR P0UPR.0 (bit P0UP) set to "1", Port 0 pins are internally pulled-up.<br>This port also provides a multiplexed low order address/data bus during accesses to external memory. |

### STACK POINTER

|      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|
| Bit: | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|      | SP.7 | SP.6 | SP.5 | SP.4 | SP.3 | SP.2 | SP.1 | SP.0 |

Mnemonic: SP

Address: 81h

| BIT | NAME     | FUNCTION                                                                                                                              |
|-----|----------|---------------------------------------------------------------------------------------------------------------------------------------|
| 7-0 | SP.[7:0] | The Stack Pointer stores the Scratch-pad RAM address where the stack begins. In other words it always points to the top of the stack. |

### DATA POINTER LOW

|      |       |       |       |       |       |       |       |       |
|------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit: | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|      | DPL.7 | DPL.6 | DPL.5 | DPL.4 | DPL.3 | DPL.2 | DPL.1 | DPL.0 |

Mnemonic: DPL

Address: 82h

| BIT | NAME      | FUNCTION                                                       |
|-----|-----------|----------------------------------------------------------------|
| 7-0 | DPL.[7:0] | This is the low byte of the standard 8052 16-bit data pointer. |

### DATA POINTER HIGH

|      |       |       |       |       |       |       |       |       |
|------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit: | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|      | DPH.7 | DPH.6 | DPH.5 | DPH.4 | DPH.3 | DPH.2 | DPH.1 | DPH.0 |

Mnemonic: DPH

Address: 83h

| BIT | NAME      | FUNCTION                                                        |
|-----|-----------|-----------------------------------------------------------------|
| 7-0 | DPH.[7:0] | This is the high byte of the standard 8052 16-bit data pointer. |

### Port 0 Pull Up Option Register

|      |   |   |   |   |   |   |   |   |
|------|---|---|---|---|---|---|---|---|
| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|---|---|



|   |   |   |   |   |   |   |      |
|---|---|---|---|---|---|---|------|
| - | - | - | - | - | - | - | P0UP |
|---|---|---|---|---|---|---|------|

Mnemonic: P0UPR

Address: 86h

| BIT | NAME | FUNCTION                                                                                                              |
|-----|------|-----------------------------------------------------------------------------------------------------------------------|
| 0   | P0UP | 0: Port 0 pins are open-drain.<br>1: Port 0 pins are internally pulled-up. Port 0 is structurally the same as Port 2. |

**Power Control**

|      |      |       |   |     |     |     |    |     |
|------|------|-------|---|-----|-----|-----|----|-----|
| Bit: | 7    | 6     | 5 | 4   | 3   | 2   | 1  | 0   |
|      | SMOD | SMOD0 | - | POR | GF1 | GF0 | PD | IDL |

Mnemonic: PCON

Address: 87h

| BIT | NAME  | FUNCTION                                                                                                                                                                                                                     |
|-----|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | SMOD  | 1: This bit doubles the serial port baud rate in mode 1, 2, and 3 when set to 1.                                                                                                                                             |
| 6   | SMOD0 | 0: Framing Error Detection Disable. SCON.7 (SM0/FE) bit is used as SM0 (standard 8052 function).<br>1: Framing Error Detection Enable. SCON.7 (SM0/FE) bit is used to reflect as Frame Error (FE) status flag.               |
| 5   | -     | Reserved                                                                                                                                                                                                                     |
| 4   | POR   | 0: Cleared by software.<br>1: Set automatically when a power-on reset has occurred.                                                                                                                                          |
| 3   | GF1   | General purpose user flags.                                                                                                                                                                                                  |
| 2   | GF0   | General purpose user flags.                                                                                                                                                                                                  |
| 1   | PD    | 1: The CPU goes into the POWER DOWN mode. In this mode, all the clocks are stopped and program execution is frozen.                                                                                                          |
| 0   | IDL   | 1: The CPU goes into the IDLE mode. In this mode, the clocks CPU clock stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating. |

**Timer Control**

|      |     |     |     |     |     |     |     |     |
|------|-----|-----|-----|-----|-----|-----|-----|-----|
| Bit: | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|      | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 |

Mnemonic: TCON

Address: 88h

| BIT | NAME | FUNCTION                                                                                                                                                                                       |
|-----|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | TF1  | Timer 1 Overflow Flag. This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit. |
| 6   | TR1  | Timer 1 Run Control. This bit is set or cleared by software to turn timer/counter on or off.                                                                                                   |
| 5   | TF0  | Timer 0 Overflow Flag. This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit. |



|   |     |                                                                                                                                                                                                                                                                           |
|---|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4 | TR0 | Timer 0 Run Control. This bit is set or cleared by software to turn timer/counter on or off.                                                                                                                                                                              |
| 3 | IE1 | Interrupt 1 Edge Detect Flag: Set by hardware when an edge/level is detected on $\overline{\text{INT1}}$ . This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin. |
| 2 | IT1 | Interrupt 1 Type Control. Set/cleared by software to specify falling edge/ low level triggered external inputs.                                                                                                                                                           |
| 1 | IE0 | Interrupt 0 Edge Detect Flag. Set by hardware when an edge/level is detected on $\overline{\text{INT0}}$ . This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin. |
| 0 | IT0 | Interrupt 0 Type Control: Set/cleared by software to specify falling edge/ low level triggered external inputs.                                                                                                                                                           |

### Timer Mode Control

|      |        |                          |    |    |        |                          |    |    |
|------|--------|--------------------------|----|----|--------|--------------------------|----|----|
| Bit: | 7      | 6                        | 5  | 4  | 3      | 2                        | 1  | 0  |
|      | GATE   | C/ $\overline{\text{T}}$ | M1 | M0 | GATE   | C/ $\overline{\text{T}}$ | M1 | M0 |
|      | TIMER1 |                          |    |    | TIMER0 |                          |    |    |

Mnemonic: TMOD

Address: 89h

| BIT | NAME                     | FUNCTION                                                                                                                                                                                                                                                                   |
|-----|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | GATE                     | Gating control: When this bit is set, Timer/counter 1 is enabled only while the $\overline{\text{INT1}}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{\text{INT1}}$ pin has no effect, and Timer 1 is enabled whenever TR1 control bit is set. |
| 6   | C/ $\overline{\text{T}}$ | Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.                                                                                                                                 |
| 5   | M1                       | Timer 1 mode select bit 1. See table below.                                                                                                                                                                                                                                |
| 4   | M0                       | Timer 1 mode select bit 0. See table below.                                                                                                                                                                                                                                |
| 3   | GATE                     | Gating control: When this bit is set, Timer/counter 0 is enabled only while the $\overline{\text{INT0}}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{\text{INT0}}$ pin has no effect, and Timer 0 is enabled whenever TR0 control bit is set. |
| 2   | C/ $\overline{\text{T}}$ | Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the T0 pin.                                                                                                                                 |
| 1   | M1                       | Timer 0 mode select bit 1. See table below.                                                                                                                                                                                                                                |
| 0   | M0                       | Timer 0 mode select bit 0. See table below.                                                                                                                                                                                                                                |

### M1, M0: Mode Select bits:

| M1 | M0 | MODE                                                                                                                                                                    |
|----|----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0  | 0  | Mode 0: 13-bit timer/counter TLx serves as 5-bit pre-scale.                                                                                                             |
| 0  | 1  | Mode 1: 16-bit timer/counter, no pre-scale.                                                                                                                             |
| 1  | 0  | Mode 2: 8-bit timer/counter with auto-reload from THx.                                                                                                                  |
| 1  | 1  | Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer0 control bits. TH0 is an 8-bit timer only controlled by Timer1 control bits. (Timer 1) |



|  |  |                             |
|--|--|-----------------------------|
|  |  | Timer/Counter 1 is stopped. |
|--|--|-----------------------------|

**Timer 0 LSB**

|      |       |       |       |       |       |       |       |       |
|------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit: | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|      | TL0.7 | TL0.6 | TL0.5 | TL0.4 | TL0.3 | TL0.2 | TL0.1 | TL0.0 |

Mnemonic: TL0

Address: 8Ah

| BIT | NAME      | FUNCTION     |
|-----|-----------|--------------|
| 7-0 | TL0.[7:0] | Timer 0 LSB. |

**Timer 1 LSB**

|      |       |       |       |       |       |       |       |       |
|------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit: | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|      | TL1.7 | TL1.6 | TL1.5 | TL1.4 | TL1.3 | TL1.2 | TL1.1 | TL1.0 |

Mnemonic: TL1

Address: 8Bh

| BIT | NAME      | FUNCTION     |
|-----|-----------|--------------|
| 7-0 | TL1.[7:0] | Timer 1 LSB. |

**Timer 0 MSB**

|      |       |       |       |       |       |       |       |       |
|------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit: | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|      | TH0.7 | TH0.6 | TH0.5 | TH0.4 | TH0.3 | TH0.2 | TH0.1 | TH0.0 |

Mnemonic: TH0

Address: 8Ch

| BIT | NAME      | FUNCTION     |
|-----|-----------|--------------|
| 7-0 | TH0.[7:0] | Timer 0 MSB. |

**Timer 1 MSB**

|      |       |       |       |       |       |       |       |       |
|------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit: | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|      | TH1.7 | TH1.6 | TH1.5 | TH1.4 | TH1.3 | TH1.2 | TH1.1 | TH1.0 |

Mnemonic: TH1

Address: 8Dh

| BIT | NAME      | FUNCTION     |
|-----|-----------|--------------|
| 7-0 | TH1.[7:0] | Timer 1 MSB. |

**AUXR**

|      |   |   |   |   |   |   |   |         |
|------|---|---|---|---|---|---|---|---------|
| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0       |
|      | - | - | - | - | - | - | - | ALE_OFF |

Mnemonic: AUXR

Address: 8Eh



| BIT | NAME    | FUNCTION                                        |
|-----|---------|-------------------------------------------------|
| 0   | ALE_OFF | 1: Disenable ALE output<br>0: Enable ALE output |

**Watchdog Timer Control Register**

|      |     |      |      |   |   |     |     |     |
|------|-----|------|------|---|---|-----|-----|-----|
| Bit: | 7   | 6    | 5    | 4 | 3 | 2   | 1   | 0   |
|      | ENW | CLRW | WIDL | - | - | PS2 | PS1 | PS0 |

Mnemonic: WDTC

Address: 8FH

| BIT | NAME  | FUNCTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                   |     |     |                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |   |   |   |    |   |   |   |    |   |   |   |     |   |   |   |     |
|-----|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|-----|-----|-------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|---|---|---|----|---|---|---|----|---|---|---|-----|---|---|---|-----|
| 7   | ENW   | Enable watch-dog if set.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                   |     |     |                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |   |   |   |    |   |   |   |    |   |   |   |     |   |   |   |     |
| 6   | CLRW  | Clear watch-dog timer and Pre-scalar if set. This flag will be cleared automatically.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                   |     |     |                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |   |   |   |    |   |   |   |    |   |   |   |     |   |   |   |     |
| 5   | WIDL  | If this bit is set, watch-dog is enabled under IDLE mode. If cleared, watch-dog is disabled under IDLE mode. Default is cleared.                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                   |     |     |                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |   |   |   |    |   |   |   |    |   |   |   |     |   |   |   |     |
| 2-0 | PS2-0 | Watch-dog Pre-scalar timer select. Pre-scalar is selected when set PS2-0 as follows: <table><tr><th>PS2</th><th>PS1</th><th>PS0</th><th>PRE-SCALAR SELECT</th></tr><tr><td>0</td><td>0</td><td>0</td><td>2</td></tr><tr><td>0</td><td>0</td><td>1</td><td>8</td></tr><tr><td>0</td><td>1</td><td>0</td><td>4</td></tr><tr><td>0</td><td>1</td><td>1</td><td>16</td></tr><tr><td>1</td><td>0</td><td>0</td><td>32</td></tr><tr><td>1</td><td>0</td><td>1</td><td>64</td></tr><tr><td>1</td><td>1</td><td>0</td><td>128</td></tr><tr><td>1</td><td>1</td><td>1</td><td>256</td></tr></table> | PS2               | PS1 | PS0 | PRE-SCALAR SELECT | 0 | 0 | 0 | 2 | 0 | 0 | 1 | 8 | 0 | 1 | 0 | 4 | 0 | 1 | 1 | 16 | 1 | 0 | 0 | 32 | 1 | 0 | 1 | 64 | 1 | 1 | 0 | 128 | 1 | 1 | 1 | 256 |
| PS2 | PS1   | PS0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | PRE-SCALAR SELECT |     |     |                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |   |   |   |    |   |   |   |    |   |   |   |     |   |   |   |     |
| 0   | 0     | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 2                 |     |     |                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |   |   |   |    |   |   |   |    |   |   |   |     |   |   |   |     |
| 0   | 0     | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 8                 |     |     |                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |   |   |   |    |   |   |   |    |   |   |   |     |   |   |   |     |
| 0   | 1     | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 4                 |     |     |                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |   |   |   |    |   |   |   |    |   |   |   |     |   |   |   |     |
| 0   | 1     | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 16                |     |     |                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |   |   |   |    |   |   |   |    |   |   |   |     |   |   |   |     |
| 1   | 0     | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 32                |     |     |                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |   |   |   |    |   |   |   |    |   |   |   |     |   |   |   |     |
| 1   | 0     | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 64                |     |     |                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |   |   |   |    |   |   |   |    |   |   |   |     |   |   |   |     |
| 1   | 1     | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 128               |     |     |                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |   |   |   |    |   |   |   |    |   |   |   |     |   |   |   |     |
| 1   | 1     | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 256               |     |     |                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |   |   |   |    |   |   |   |    |   |   |   |     |   |   |   |     |

**Port 1**

|      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|
| Bit: | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|      | P1.7 | P1.6 | P1.5 | P1.4 | P1.3 | P1.2 | P1.1 | P1.0 |

Mnemonic: P1

Address: 90h

| BIT | NAME     | FUNCTION                                                                                                                                                                      |
|-----|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-0 | P1.[7:0] | General purpose I/O port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. |

**Serial Port Control**

|      |        |     |     |     |     |     |    |    |
|------|--------|-----|-----|-----|-----|-----|----|----|
| Bit: | 7      | 6   | 5   | 4   | 3   | 2   | 1  | 0  |
|      | SM0/FE | SM1 | SM2 | REN | TB8 | RB8 | TI | RI |



Mnemonic: SCON

Address: 98h

| BIT | NAME   | FUNCTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-----|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | SM0/FE | Serial port mode select bit 0 or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.                                                                                                                                                                                                                                                                                                                                       |
| 6   | SM1    | Serial Port mode select bit 1. See table below.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 5   | SM2    | Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1, then RI will not be activated if a valid stop bit was not received. In mode 0, the SM2 bit controls the serial port clock. If set to 0, then the serial port runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052. When set to 1, the serial clock become divide by 4 of the oscillator clock. This results in faster synchronous serial communication. |
| 4   | REN    | Receive enable:<br>0: Disable serial reception.<br>1: Enable serial reception.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 3   | TB8    | This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 2   | RB8    | In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 1   | TI     | Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 0   | RI     | Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2 apply to this bit. This bit can be cleared only by software.                                                                                                                                                                                                                                                                                                                                                                                   |

SM1, SM0: Mode Select bits:

| Mode | SM0 | SM1 | Description  | Length | Baud Rate                |
|------|-----|-----|--------------|--------|--------------------------|
| 0    | 0   | 0   | Synchronous  | 8      | Tclk divided by 4 or 12  |
| 1    | 0   | 1   | Asynchronous | 10     | Variable                 |
| 2    | 1   | 0   | Asynchronous | 11     | Tclk divided by 32 or 64 |
| 3    | 1   | 1   | Asynchronous | 11     | Variable                 |

## Serial Data Buffer

|      |        |        |        |        |        |        |        |        |
|------|--------|--------|--------|--------|--------|--------|--------|--------|
| Bit: | 7      | 6      | 5      | 4      | 3      | 2      | 1      | 0      |
|      | SBUF.7 | SBUF.6 | SBUF.5 | SBUF.4 | SBUF.3 | SBUF.2 | SBUF.1 | SBUF.0 |

Mnemonic: SBUF

Address: 99h