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8-BIT MICROCONTROLLER

Table of Contents-

1 GENERAL DESCRIPTION

The W78E516D/W78E058D series is an 8-bit microcontroller which has an in-system programmable Flash EPROM for on-chip firmware updating.

The instruction sets of the W78E516D/W78E058D are fully compatible with the standard 8052. The W78E516D/W78E058D series contains a 64K/32K bytes of main Flash EPROM and a 4K bytes of auxiliary Flash EPROM which allows the contents of the 64K/32K bytes main Flash EPROM to be updated by the loader program located in the 4K bytes Flash EPROM; a 256 bytes of SRAM; 256 bytes of AUXRAM; four 8-bit bi-directional and bit-addressable I/O ports; an additional 4-bit port P4; three 16-bit timer/counters; a serial port. These peripherals are supported by an 8 sources 2-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W78E516D/W78E058D series allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

The W78E516D/W78E058D series microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

2 FEATURES

- Fully static design 8-bit CMOS microcontroller
- Optional 12T or 6T mode
  - 12T Mode, 12 clocks per machine cycle operation (default), Speed up to 40 MHz/5V
  - 6T Mode, 6 clocks per machine cycle operation set by the writer, Speed up to 20 MHz/5V
- Wide supply voltage of 2.4 to 5.5V
- Temperature grade is (-40°C~85°C)
- 64K/32K bytes of in-system programmable FLASH EPROM for Application Program (APROM)
- 4K bytes of auxiliary FLASH EPROM for Loader Program (LDROM)
- Low standby current at full supply voltage
- 512 bytes of on-chip RAM. (include 256 bytes of AUX-RAM, software selectable)
- 64K bytes program memory address space and 64K bytes data memory address space
- One 4-bit multipurpose programmable port, additional $\overline{INT2}$ / $\overline{INT3}$
- Support Watch Dog Timer
- Three 16-bit timer/counters
- One full duplex serial port
- 8-sources, 2-level interrupt capability
- Software Reset
- Built-in power management with idle mode and power down mode
- Code protection
- Packages:
  - Lead Free (RoHS) DIP 40: W78E516DDG
  - Lead Free (RoHS) PLCC 44: W78E516DPG
  - Lead Free (RoHS) PQFP 44: W78E516DFG
  - Lead Free (RoHS) LQFP 48: W78E516DLG
  - Lead Free (RoHS) DIP 40: W78E058DDG
  - Lead Free (RoHS) PLCC 44: W78E058DPG
  - Lead Free (RoHS) PQFP 44: W78E058DFG
  - Lead Free (RoHS) LQFP 48: W78E058DLG

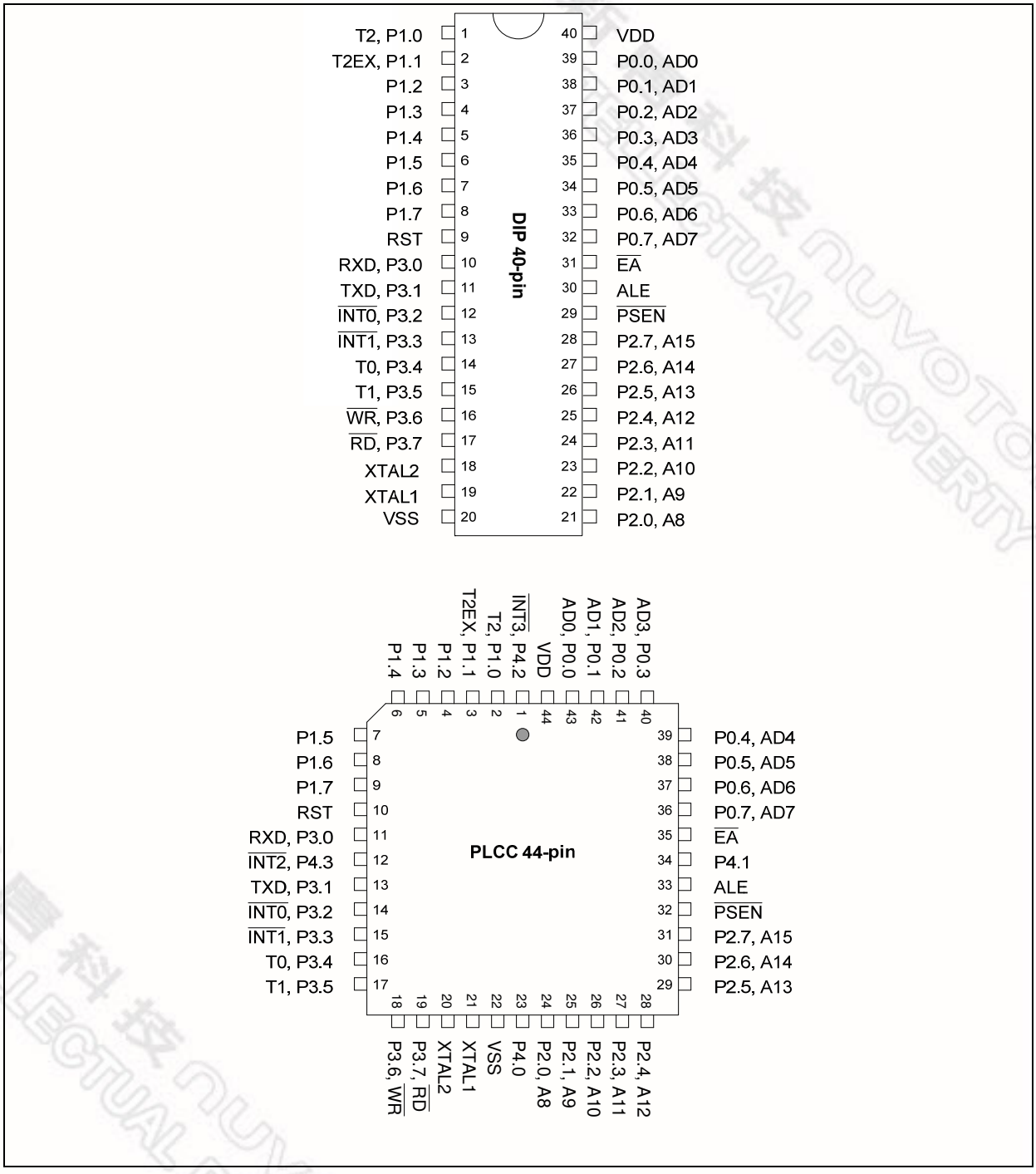
3 PARTS INFORMATION LIST

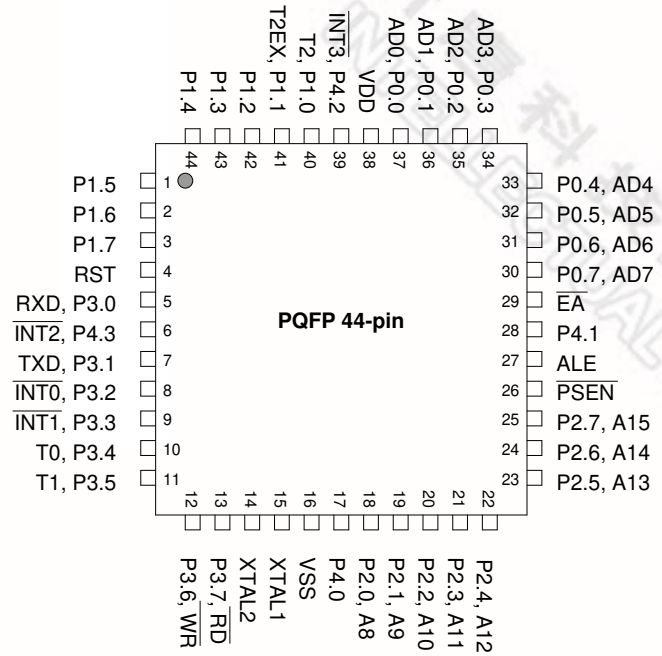
3.1 Lead Free (RoHS) Parts information list

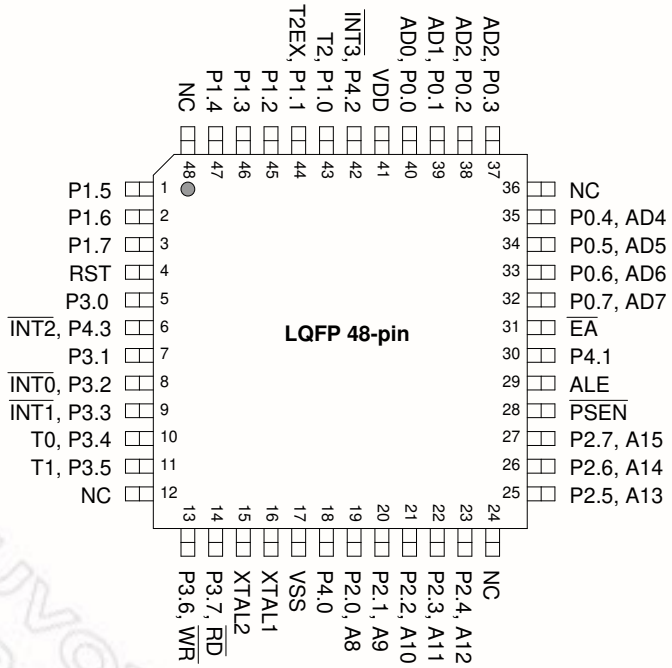
Table 3-1: Lead Free (RoHS) Parts information list

PART NO.	APROM FLASH SIZE	LDROM FLASH SIZE	RAM	PACKAGE	Temperature grade
W78E516DDG	64K Bytes	4K Bytes	512 Bytes	DIP-40 Pin	-40°C~85°C
W78E516DPG			512 Bytes	PLCC-44 Pin	
W78E516DFG			512 Bytes	PQFP-44 Pin	
W78E516DLG			512 Bytes	LQFP-48 Pin	
W78E058DDG	32K Bytes	4K Bytes	512 Bytes	DIP-40 Pin	-40°C~85°C
W78E058DPG			512 Bytes	PLCC-44 Pin	
W78E058DFG			512 Bytes	PQFP-44 Pin	
W78E058DLG			512 Bytes	LQFP-48 Pin	

4 PIN CONFIGURATIONS




PQFP 44-pin
1 P1.5
2 P1.6
3 P1.7
4 RST
5 RXD, P3.0
6 INT2, P4.3
7 TXD, P3.1
8 INT0, P3.2
9 INT1, P3.3
10 T0, P3.4
11 T1, P3.5
12 P3.6, WR
13 P3.7, RD
14 XTAL2
15 XTAL1
16 VSS
17 P4.0
18 P2.0, A8
19 P2.1, A9
20 P2.2, A10
21 P2.3, A11
22 P2.4, A12
23 P2.5, A13
24 P2.6, A14
25 P2.7, A15
26 PSEN
27 ALE
28 P4.1
29 EA
30 P0.7, AD7
31 P0.6, AD6
32 P0.5, AD5
33 P0.4, AD4
34 AD3, P0.3
35 AD2, P0.2
36 AD1, P0.1
37 AD0, P0.0
38 VDD
39 INT3, P4.2
40 T2, P1.0
41 T2EX, P1.1
42 P1.2
43 P1.3
44 P1.4


LQFP 48-pin
1 P1.5
2 P1.6
3 P1.7
4 RST
5 P3.0
6 INT2, P4.3
7 P3.1
8 INT0, P3.2
9 INT1, P3.3
10 T0, P3.4
11 T1, P3.5
12 NC
13 P3.6, WR
14 P3.7, RD
15 XTAL2
16 XTAL1
17 VSS
18 P4.0
19 P2.0, A8
20 P2.1, A9
21 P2.2, A10
22 P2.3, A11
23 P2.4, A12
24 NC
25 P2.5, A13
26 P2.6, A14
27 P2.7, A15
28 PSEN
29 ALE
30 P4.1
31 EA
32 P0.7, AD7
33 P0.6, AD6
34 P0.5, AD5
35 P0.4, AD4
36 NC
37 AD2, P0.3
38 AD2, P0.2
39 AD1, P0.1
40 AD0, P0.0
41 VDD
42 INT3, P4.2
43 T2, P1.0
44 T2EX, P1.1
45 P1.2
46 P1.3
47 P1.4
48 NC

5 PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTIONS
$\overline{EA}$	I	**EXTERNAL ACCESS ENABLE:** This pin forces the processor to execute the external ROM. The ROM address and data will not be present on the bus if the $\overline{EA}$ pin is high and the program counter is within the internal ROM area. Otherwise they will be present on the bus.
$\overline{PSEN}$	O H	**PROGRAM STORE ENABLE:** $\overline{PSEN}$ enables the external ROM data in the Port 0 address/data bus. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs originate from this pin.
ALE	O H	**ADDRESS LATCH ENABLE:** ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6th of the oscillator frequency. An ALE pulse is omitted during external data memory accesses.
RST	I L	**RESET:** A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	I	**CRYSTAL 1:** This is the crystal oscillator input. This pin may be driven by an external clock.
XTAL2	O	**CRYSTAL 2:** This is the crystal oscillator output. It is the inversion of XTAL1.
VSS	I	**GROUND:** ground potential.
VDD	I	**POWER SUPPLY:** Supply voltage for operation.
P0.0–P0.7	I/O D	**PORT 0:** Port 0 is an **open-drain bi-directional I/O port**. This port also provides a multiplexed low order address/data bus during accesses to external memory.
P1.0–P1.7	I/O H	**PORT 1**: Port 1 is a bi-directional I/O port with internal pull-ups. The bits have alternate functions which are described below: T2(P1.0): Timer/Counter 2 external count input T2EX(P1.1): Timer/Counter 2 Reload/Capture/Direction control
P2.0–P2.7	I/O H	**PORT 2:** Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.
P3.0–P3.7	I/O H	**PORT 3:** Port 3 is a bi-directional I/O port with internal pull-ups. All bits have alternate functions, which are described below: RXD(P3.0): Serial Port 0 input TXD(P3.1): Serial Port 0 output $\overline{INT0}$ (P3.2) : External Interrupt 0 $\overline{INT1}$ (P3.3) : External Interrupt 1 T0(P3.4) : Timer 0 External Input T1(P3.5) : Timer 1 External Input $\overline{WR}$ (P3.6) : External Data Memory Write Strobe $\overline{RD}$ (P3.7) : External Data Memory Read Strobe
P4.0–P4.3	I/O H	**PORT 4:** Another bit-addressable bidirectional I/O port P4. P4.3 and P4.2 are alternative function pins. It can be used as general I/O port or external interrupt input sources ($\overline{INT2}$ / $\overline{INT3}$).

* Note : **TYPE** I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain

6 BLOCK DIAGRAM

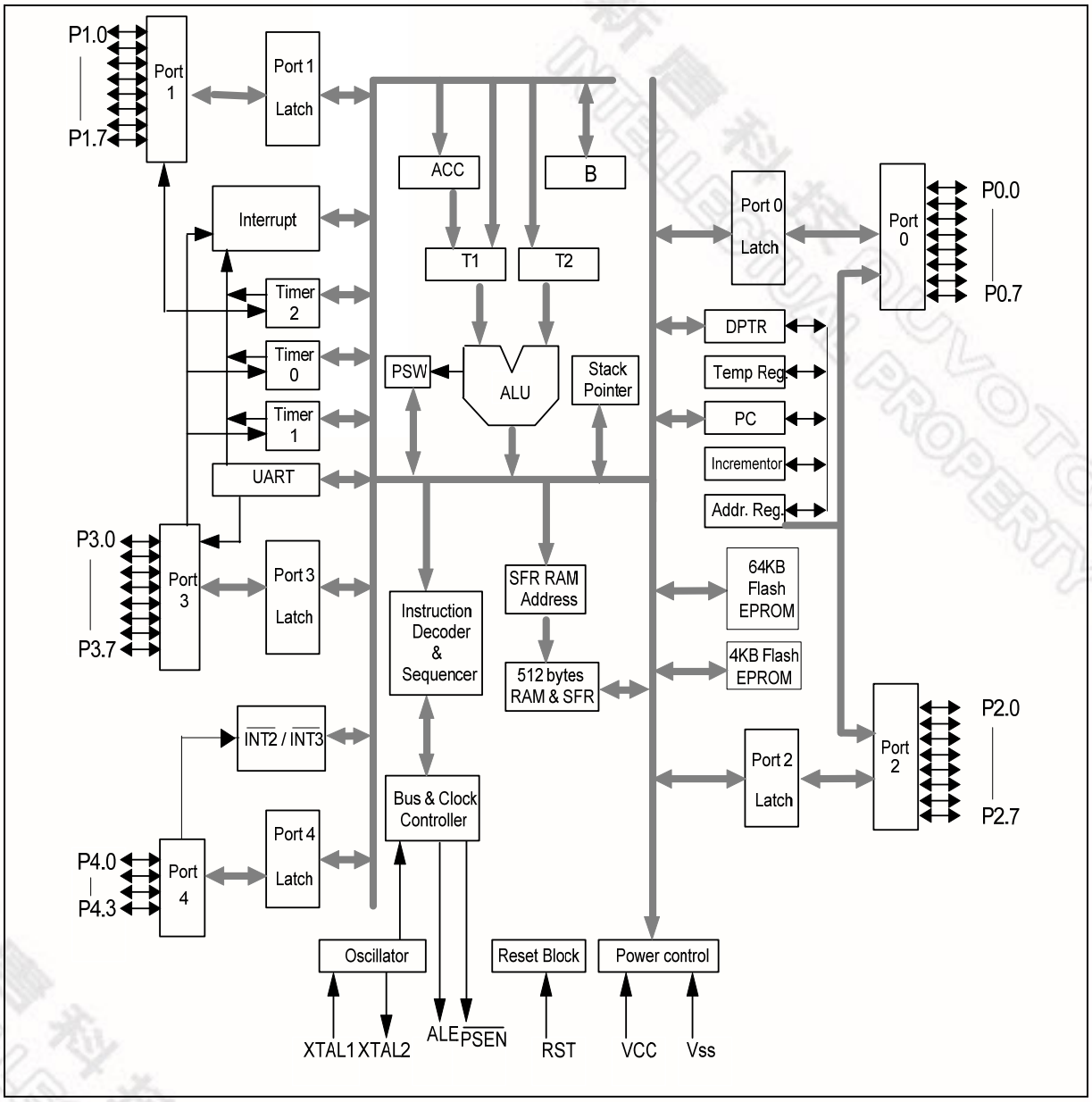


Figure 6- 1 W78E516D/W78E058D Block Diagram

7 FUNCTIONAL DESCRIPTION

The W78E516D/W78E058D series architecture consists of a core controller surrounded by various registers, four general purpose I/O ports, one special purpose programmable 4-bits I/O port, 512 bytes of RAM, three timer/counters, a serial port. The processor supports 111 different op-codes and references both a 64K program address space and a 64 K data storage space.

7.1 On-Chip Flash EPROM

The W78E516D/W78E058D series includes one 64K/32K bytes of main FLASH EPROM for application program (APROM) and one 4K bytes of FLASH EPROM for loader program (LDROM) when operating the in-system programming feature. In normal operation, the microcontroller will execute the code from the 64K/32K bytes of main FLASH EPROM. By setting program registers, user can force microcontroller to switch to the programming mode which microcontroller will execute the code (loader program) from the 4K bytes of auxiliary FLASH EPROM, and this loader program is going to update the contents of the 64K/32K bytes of main FLASH EPROM. After reset, the microcontroller executes the new application program in the main FLASH EPROM. This in-system programming feature makes the job easy and efficient in which the application needs to update firmware frequently. In some applications, the in-system programming feature make it possible that the end-user is able to easily update the system firmware by the them without opening the chassis.

7.2 I/O Ports

The W78E516D/W78E058D series has four 8-bit ports and one extra 4-bit port. Port 0 can be used as an Address/Data bus when external program is running or external memory/device is accessed by MOVC or MOVX instruction. In these cases, it has strong pull-ups and pull-downs, and does not need any external pull-ups. Otherwise it can be used as a general I/O port with open-drain circuit. Port 2 is used chiefly as the upper 8-bits of the Address bus when port 0 is used as an address/data bus. It also has strong pull-ups and pull-downs when it serves as an address bus. Port1 and 3 act as I/O ports with alternate functions. Port 4 is only available on PLCC/QFP/LQFP package type. It serves as a general purpose I/O port as Port 1 and Port 3. Another bit-addressable bidirectional I/O port P4. P4.3 and P4.2 are alternative function pins. It can be used as general I/O port or external interrupt input sources ($\overline{INT2}$ / $\overline{INT3}$).

7.3 Serial I/O

The W78E516D/W78E058D series have one serial port that is functionally similar to the serial port of the original 8032 family. However the serial port on the W78E516D/W78E058D series can operate in different modes in order to obtain timing similarity as well.

7.4 Timers

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for timers 0 and 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as reload/capture registers for Timer 2.

The operations of Timer 0 and Timer 1 are the same as in the 8051 CPU. Timer 2 is a special feature of the W78E516D/W78E058D series: it is a 16-bit timer/counter that is configured and controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or

as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed at capture or auto-reload mode is the same as that of Timers 0 and 1.

7.4.1 Clock

The W78E516D/W78E058D series are designed to be used with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used by default. This makes the W78E516D/W78E058D series relatively insensitive to duty cycle variations in the clock.

7.5 Interrupts

The Interrupt structure in the W78E516D/W78E058D series is slightly different from that of the standard 8052. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased. The W78E516D/W78E058D series provides 8 interrupt resources with two priority level, including four external interrupt sources, three timer interrupts, serial I/O interrupts.

7.6 Data Pointers

The data pointer of W78E516D/W78E058D series is same as standard 8052 that have one 16-bit Data Pointer (DPTR).

7.7 Architecture

The W78E516D/W78E058D series are based on the standard 8052 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard 8052 instruction set.

7.7.1 ALU

The ALU is the heart of the W78E516D/W78E058D series. It is responsible for the arithmetic and logical functions. It is also used in decision making, in case of jump instructions, and is also used in calculating jump addresses. The user cannot directly use the ALU, but the Instruction Decoder reads the op-code, decodes it, and sequences the data through the ALU and its associated registers to generate the required result. The ALU mainly uses the ACC which is a special function register (SFR) on the chip. Another SFR, namely B register is also used Multiply and Divide instructions. The ALU generates several status signals which are stored in the Program Status Word register (PSW).

7.7.2 Accumulator

The Accumulator (ACC) is the primary register used in arithmetic, logical and data transfer operations in the W78E516D/W78E058D series. Since the Accumulator is directly accessible by the CPU, most of the high speed instructions make use of the ACC as one argument.

7.7.3 B Register

This is an 8-bit register that is used as the second argument in the MUL and DIV instructions. For all other instructions it can be used simply as a general purpose register.

7.7.4 Program Status Word

This is an 8-bit SFR that is used to store the status bits of the ALU. It holds the Carry flag, the Auxiliary Carry flag, General purpose flags, the Register Bank Select, the Overflow flag, and the Parity flag.

7.7.5 Stack Pointer

The W78E516D/W78E058D series has an 8-bit Stack Pointer which points to the top of the Stack. This stack resides in the Scratch Pad RAM in the W78E516D/W78E058D series. Hence the size of the stack is limited by the size of this RAM.

7.7.6 Scratch-pad RAM

The W78E516D/W78E058D series has a 256 bytes on-chip scratch-pad RAM. This can be used by the user for temporary storage during program execution. A certain section of this RAM is bit addressable, and can be directly addressed for this purpose.

7.7.7 AUX-RAM

AUX-RAM 0H~255H is addressed indirectly as the same way to access external data memory with the MOVX instruction. The data memory region is from 0000H to 00FFH. Memory MAP shows the memory map for this product series. W78E516D/W78E058D series can read/write 256 bytes AUX RAM by the MOVX instruction.

8 MEMORY ORGANIZATION

The W78E516D/W78E058D series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

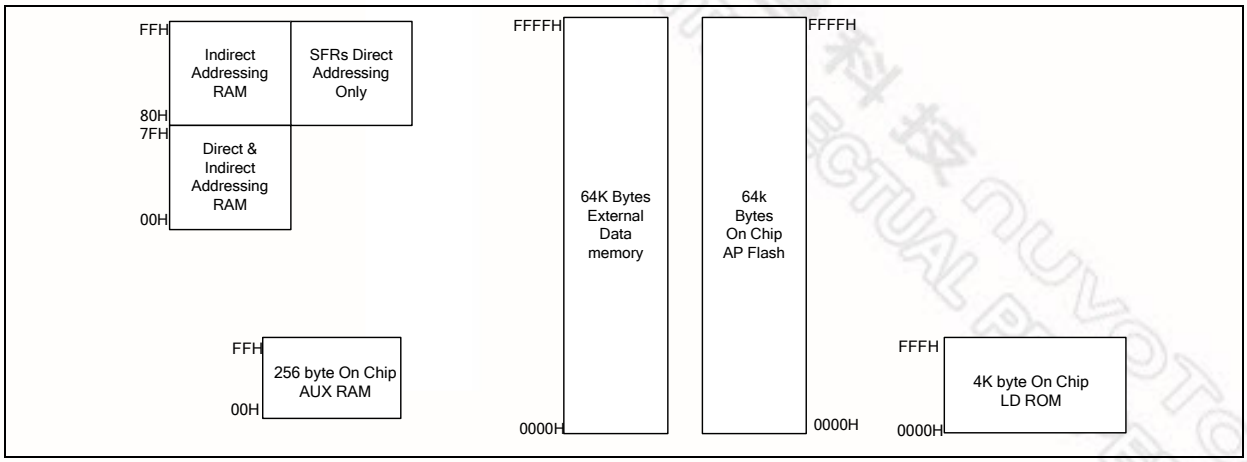


Figure 8- 1 Memory Map

8.1 Program Memory (on-chip Flash)

The Program Memory on the W78E516D/W78E058D series can be up to 64K/32K bytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

8.2 Scratch-pad RAM and Register Map

As mentioned before the W78E516D/W78E058D series have separate Program and Data Memory areas. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.

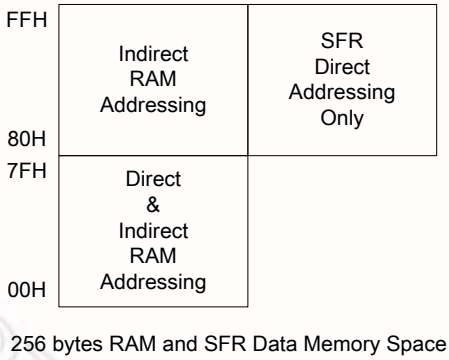


Figure 8- 2 W78E516D/W78E058D RAM and SFR Memory Map

Since the scratch-pad RAM is only 256bytes it can be used only when data contents are small. There are several other special purpose areas within the scratch-pad RAM. These are illustrated in next figure.

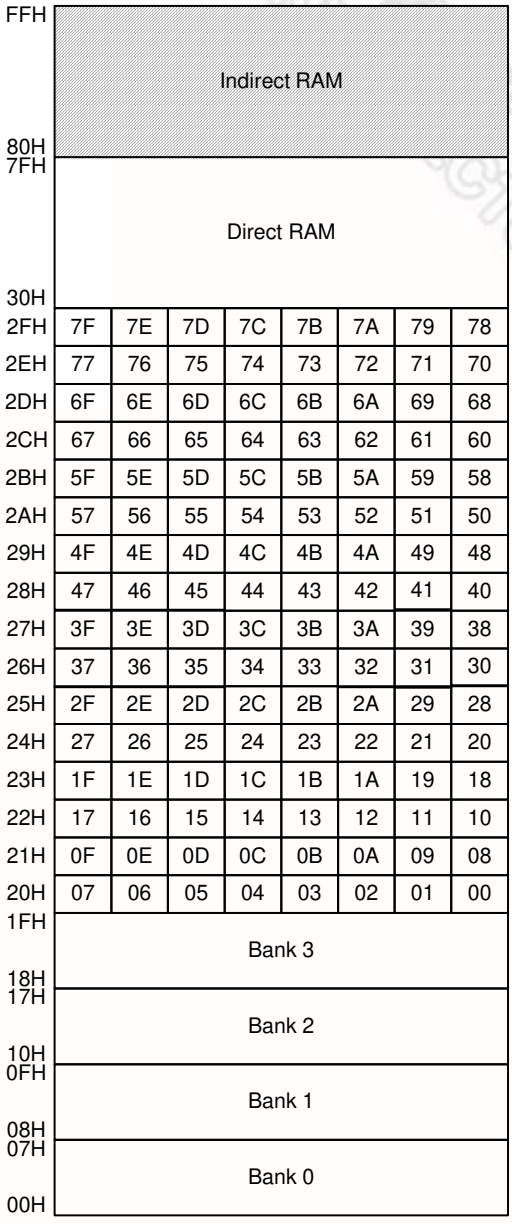


Figure 8- 3 Scratch-pad RAM

8.2.1 Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed as Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at one time the W78E516D/W78E058D series can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

8.2.2 Bit addressable Locations

The Scratch-pad RAM area from location 20h to 2Fh is byte as well as bit addressable. This means that a bit in this area can be individually addressed. In addition some of the SFRs are also bit addressable. The instruction decoder is able to distinguish a bit access from a byte access by the type of the instruction itself. In the SFR area, any existing SFR whose address ends in a 0 or 8 is bit addressable.

8.2.3 Stack

The scratch-pad RAM can be used for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a jump, call or interrupt is invoked the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07h at reset. The user can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, and then the SP is decreased.

8.2.4 AUX-RAM

AUX-RAM 0H~255H is addressed indirectly as the same way to access external data memory with the MOVX instruction. Address pointer are R0 and R1 of the selected register bank and DPTR register. A access to external data memory locations higher than 255 will be performed with the MOVX instruction in the same way as in the 8051. The AUX-RAM is disabled after power-on reset. Setting the bit 4 in CHPCON register will enable the access to AUX-RAM.

9 SPECIAL FUNCTION REGISTERS

The W78E516D/W78E058D series uses Special Function Registers (SFRs) to control and monitor peripherals and their Modes. The SFRs reside in the register locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where users wish to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. The W78E516D/W78E058D series contain all the SFRs present in the standard 8052. However some additional SFRs are added. In some cases the unused bits in the original 8052, have been given new functions. The list of the SFRs is as follows.

W78E516D/W78E058D Special Function Registers (SFRs) and Reset Values

F8									FF
F0	+B						CHPENR		F7
E8									EF
E0	+ACC								E7
D8	+P4								DF
D0	+PSW								D7
C8	+T2CON		RCAP2L	RCAP2H	TL2	TH2			CF
C0	+XICON		P4CONA	P4CONB	**SFRAL**	**SFRAH**	SFRFD	SFRCN	C7
B8	+IP							CHPCON	BF
B0	+P3				**P43AL**	**P43AH**			B7
A8	+IE				**P42AL**	**P42AH**	P2ECON		AF
A0	+P2								A7
98	+SCON	SBUF							9F
90	+P1				**P41AL**	**P41AH**			97
88	+TCON	TMOD	TL0	TL1	TH0	TH1	AUXR	WDTC	8F
80	+P0	SP	DPL	DPH	**P40AL**	**P40AH**	P0UPR	PCON	87

Figure 9-1: Special Function Register Location Table

Note: 1.The SFRs marked with a plus sign(+) are both byte- and bit-addressable.
2. The text of SFR with bold type characters are extension function registers.

Special Function Registers:

SYMBOL	DEFINITION	ADDRESS	MSB	BIT ADDRESS, SYMBOL						LSB	RESET
CHPENR	Chip enable register	F6H									1111 0110B
B	B register	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	0000 0000B
ACC	Accumulator	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	0000 0000B
P4	Port 4	D8H					P43	P42	P41	P40	0000 1111B
PSW	Program status word	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P	0000 0000B
TH2	T2 reg. high	CDH									0000 0000B
TL2	T2 reg. low	CCH									0000 0000B
RCAP2H	T2 capture low	CBH									0000 0000B
RCAP2L	T2 capture high	CAH									0000 0000B
T2CON	Timer 2 control	C8H	(CF) TF2	(CE) EXF2	(CD) RCLK	(CC) TCLK	(CB) EXEN2	(CA) TR2	(C9) C/T2	(C8) CP/RL2	0000 0000B
SFRCN	SFR for program control	C7H									0000 0000B
SFRFD	SFR for program data	C6H									0000 0000B
SFRAH	Port4 base address high register	C5H									0000 0000B
SFRAL	Port4 base address low register	C4H									0000 0000B
P4CONB	Port 4 control B	C3H	P43FUN1	P43FUN0	P43CMP1	P43COM0	P42FUN1	P42FUN0	P42CMP1	P42CMP2	0000 0000B
P4CONA	Port 4 control A	C2H	P41UN1	P41FUN0	P41CMP1	P41COM0	P40FUN1	P40FUN0	P40CMP1	P40CMP2	0000 0000B
XICON	External interrupt control	C0H	PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2	0000 0000B
CHPCON	Chip Control	BFH	SWRESET			ENAUXRAM			FBOOTSL	FPROGEN	XXX0 0000B[1]
IP	Interrupt priority	B8H	(BF) -	(BE) -	(BD) PT2	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	x000 0000B
P43AH	Port 4.3 comparator high address	B5H									0000 0000B
P43AL	Port 4.3 comparator low address	B4H									0000 0000B
P3	Port 3	B0H	(B7) RD	(B6) WR	(B5) T1	(B4) T0	(B3) INT1	(B2) INT0	(B1) TXD	(B0) RXD	1111 1111B
P2ECON	Port 2 expanded control	AEH	P43CSINV	P42CSINV	P41CSINV	P40CSINV	-	-			0000 0000B
P42AH	Port 4.2 comparator high address	ADH									0000 0000B
P42AL	Port 4.3 comparator low address	ACH									0000 0000B
IE	Interrupt enable	A8H	(AF) EA	(AE) -	(AD) ET2	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	0000 0000B
P2	Port 2	A0H	(A7) A15	(A6) A14	(A5) A13	(A4) A12	(A3) A11	(A2) A10	(A1) A9	(A0) A8	1111 1111B
SBUF	Serial buffer	99H									xxxx xxxxB
SCON	Serial control	98H	(9F) SM0/FE	(9E) SM1	(9D) SM2	(9C) REN	(9B) TB8	(9A) RB8	(99) TI	(98) RI	0000 0000B
P41AH	Port 4.1 comparator high address	95H									0000 0000B
P41AL	Port 4.1 comparator low address	94H									0000 0000B
P1	Port 1	90H	(97)	(96)	(95)	(94)	(93)	(92)	(91) T2EX	(90) T2	1111 1111B
WDTC	Watchdog control	8FH	ENW	CLRW	WIDL	-	-	PS2	PS1	PS0	0000 0000B
AUXR	Auxiliary	8EH								ALE_OFF	0000 0110B
TH1	Timer high 1	8DH									0000 0000B
TH0	Timer high 0	8CH									0000 0000B
TL1	Timer low 1	8BH									0000 0000B
TL0	Timer low 0	8AH									0000 0000B
TMOD	Timer mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	0000 0000B

TCON	Timer control	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	0000 0000B
PCON	Power control	87H	SMOD	SMOD0	-	POR	GF1	GF0	PD	IDL	00x1 0000B
P0UPR	Port 0 pull up option register	86H								P0UP	0000 0000B
P40AH	HI address comparator of P4.0	85H									0000 0000B
P40AL	LO address comparator of P4.0	84H									0000 0000B
DPH	Data pointer high	83H									0000 0000B
DPL	Data pointer low	82H									0000 0000B
SP	Stack pointer	81H									0000 0111B
P0	Port 0	80H	(87)	(86)	(85)	(84)	(83)	(82)	(81)	(80)	1111 1111B

[1]: When CPU in F04KBOOT mode (Ref. P65), CHPCON=1xx0 0000B, other mode the CHPCON=0xx0 0000B

9.1 SFR Detail Bit Descriptions

Port 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

BIT	NAME	FUNCTION
7-0	P0.[7:0]	Port 0 is an open-drain bi-directional I/O port. This port also provides a multiplexed low order address/data bus during accesses to external memory.

STACK POINTER

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

BIT	NAME	FUNCTION
7-0	SP.[7:0]	The Stack Pointer stores the Scratch-pad RAM address where the stack begins. In other words it always points to the top of the stack.

DATA POINTER LOW

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

BIT	NAME	FUNCTION
7-0	DPL.[7:0]	This is the low byte of the standard 8052 16-bit data pointer.

DATA POINTER HIGH

Bit:	7	6	5	4	3	2	1	0

DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

BIT	NAME	FUNCTION
7-0	DPH.[7:0]	This is the high byte of the standard 8052 16-bit data pointer.

P4.0 Base Address Low Byte Register

Bit:	7	6	5	4	3	2	1	0
	P40AL.7	P40AL.6	P40AL.5	P40AL.4	P40AL.3	P40AL.2	P40AL.1	P40AL.0

Mnemonic: P40AL Address: 84h

BIT	NAME	FUNCTION
7-0	P40AL.[7:0]	The Base address register for comparator of P4.0. P40AL contains the low-order byte of address.

P4.0 Base Address High Byte Register

Bit:	7	6	5	4	3	2	1	0
	P40AH.7	P40AH.6	P40AH.5	P40AH.4	P40AH.3	P40AH.2	P40AH.1	P40AH.0

Mnemonic:P40AH Address: 85h

BIT	NAME	FUNCTION
7-0	P40AH.[7:0]	The Base address register for comparator of P4.0. P40AH contains the High-order byte of address.

Port 0 Pull up Option Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	P0UP

Mnemonic: P0UPR Address: 86h

BIT	NAME	FUNCTION
0	P0UP	0: Port 0 pins are open-drain. 1: Port 0 pins are internally pulled-up. Port 0 is structurally the same as Port 2.

Power Control

Bit:	7	6	5	4	3	2	1	0
	SMOD	SMOD0	-	-	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: This bit doubles the serial port baud rate in mode 1, 2, and 3 when set to 1.
6	SMOD 0	0: Framing Error Detection Disable. SCON.7 (SM0/FE) bit is used as SM0 (standard 8052 function). 1: Framing Error Detection Enable. SCON.7 (SM0/FE) bit is used to reflect as

		Frame Error (FE) status flag.
5	-	Reserved
4	POR	0: Cleared by software. 1: Set automatically when a power-on reset has occurred.
3	GF1	General purpose user flags.
2	GF0	General purpose user flags.
1	PD	1: The CPU goes into the POWER DOWN mode. In this mode, all the clocks are stopped and program execution is frozen.
0	IDL	1: The CPU goes into the IDLE mode. In this mode, the clocks CPU clock stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating.

Timer Control

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 Overflow Flag. This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
5	TF0	Timer 0 Overflow Flag. This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
3	IE1	Interrupt 1 Edge Detect Flag: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
2	IT1	Interrupt 1 Type Control. Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect Flag. Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
0	IT0	Interrupt 0 Type Control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

Timer Mode Control

Bit:	7	6	5	4	3	2	1	0

GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
TIMER1				TIMER0			

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.
5	M1	Timer 1 mode select bit 1. See table below.
4	M0	Timer 1 mode select bit 0. See table below.
3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 control bit is set.
2	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the T0 pin.
1	M1	Timer 0 mode select bit 1. See table below.
0	M0	Timer 0 mode select bit 0. See table below.

M1, M0: Mode Select bits:

M1	M0	MODE
0	0	Mode 0: 8-bit timer/counter TLx serves as 5-bit pre-scale.
0	1	Mode 1: 16-bit timer/counter, no pre-scale.
1	0	Mode 2: 8-bit timer/counter with auto-reload from THx.
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer0 control bits. TH0 is an 8-bit timer only controlled by Timer1 control bits. (Timer 1) Timer/Counter 1 is stopped.

Timer 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

BIT	NAME	FUNCTION
7-0	TL0.[7:0]	Timer 0 LSB.

Timer 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

BIT	NAME	FUNCTION
7-0	TL1.[7:0]	Timer 1 LSB.

Timer 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

BIT	NAME	FUNCTION
7-0	TH0.[7:0]	Timer 0 MSB.

Timer 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

BIT	NAME	FUNCTION
7-0	TH1.[7:0]	Timer 1 MSB.

AUXR

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	ALE_OFF

Mnemonic: AUXR Address: 8Eh

BIT	NAME	FUNCTION
0	ALE_OFF	1: Disable ALE output 0: Enable ALE output

Watchdog Timer Control Register

Bit:	7	6	5	4	3	2	1	0
	ENW	CLRW	WIDL	-	-	PS2	PS1	PS0

Mnemonic: WDTC Address: 8FH

BIT	NAME	FUNCTION
7	ENW	Enable watch-dog if set.
6	CLRW	Clear watch-dog timer and Pre-scalar if set. This flag will be cleared automatically.
5	WIDL	If this bit is set, watch-dog is enabled under IDLE mode. If cleared, watch-dog is

		disabled under IDLE mode. Default is cleared.
2-0	PS2-0	Watch-dog Pre-scalar timer select. Pre-scalar is selected when set PS2–0 as follows: **PS2 PS1 PS0 — PRE-SCALAR SELECT** 0 0 0 — 2 0 0 1 — 4 0 1 0 — 8 0 1 1 — 16 1 0 0 — 32 1 0 1 — 64 1 1 0 — 128 1 1 1 — 256

Port 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

BIT	NAME	FUNCTION
7-0	P1.[7:0]	General purpose I/O port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read.

P4.1 Base Address Low Byte Register

Bit:	7	6	5	4	3	2	1	0
	P41AL.7	P41AL.6	P41AL.5	P41AL.4	P41AL.3	P41AL.2	P41AL.1	P41AL.0

Mnemonic: P41AL Address: 94h

BIT	NAME	FUNCTION
7-0	P41AL.[7:0]	The Base address register for comparator of P4.1. P41AL contains the low-order byte of address.

P4.1 Base Address High Byte Register

Bit:	7	6	5	4	3	2	1	0
	P41AH.7	P41AH.6	P41AH.5	P41AH.4	P41AH.3	P41AH.2	P41AH.1	P41AH.0

Mnemonic: P41AH Address: 95h

BIT	NAME	FUNCTION
7-0	P41AH.[7:0]	The Base address register for comparator of P4.1. P41AH contains the High-order byte of address.

Serial Port Control

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial port mode select bit 0 or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.
6	SM1	Serial Port mode select bit 1. See table below.
5	SM2	Multiprocessor communication mode enable. The function of this bit is dependent on the serial port mode. Mode 0: No effect. Mode 1: Checking valid stop bit. 0 = Reception is always valid no matter the logic level of stop bit. 1 = Reception is ignored if the received stop bit is not logic 1. Mode 2 or 3: For multiprocessor communication. 0 = Reception is always valid no matter the logic level of the 9th bit. 1 = Reception is ignored if the received 9th bit is not logic 1.
4	REN	Receive enable: 0: Disable serial reception. 1: Enable serial reception.
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2 apply to this bit. This bit can be cleared only by software.

SM1, SM0: Mode Select bits:

Mode	SM0	SM1	Description	Length	Baud Rate
0	0	0	Synchronous	8	Tclk divided by 4 or 12
1	0	1	Asynchronous	10	Variable
2	1	0	Asynchronous	11	Tclk divided by 32 or 64
3	1	1	Asynchronous	11	Variable