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8-BIT MICROCONTROLLER

Table of Contents-

1. GENERAL DESCRIPTION

The W78ERD2 is an 8-bit microcontroller which is pin- and instruction-set-compatible with the standard 80C52. The W78ERD2 contains a 64-KB Flash EPROM whose contents may be updated in-system by a loader program stored in an auxiliary, 4-KB Flash EPROM. Once the contents are confirmed, it can be protected for security.

The W78ERD2 also contains 256 bytes of on-chip RAM; 1 KB of auxiliary RAM; four 8-bit, bi-directional and bit-addressable I/O ports; an additional 4-bit port P4; three 16-bit timer/counters; and a serial port. These peripherals are all supported by nine interrupt sources with 4 levels of priority.

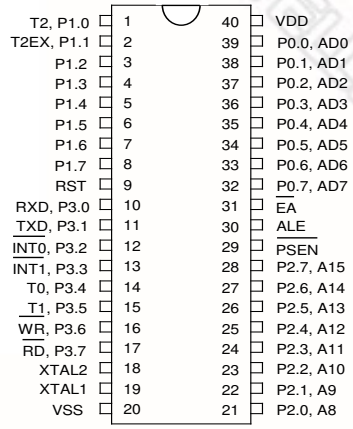
The W78ERD2 has two power-reduction modes: idle mode and power-down mode, both of which are software-selectable. Idle mode turns off the processor clock but allows peripherals to continue operating, while power-down mode stops the crystal oscillator for minimum power consumption. Power-down mode can be activated at any time and in any state without affecting the processor.

2. FEATURES

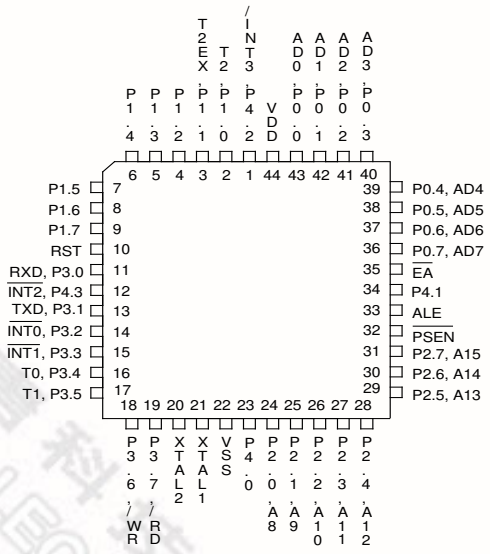
- 8-bit CMOS microcontroller
- Pin-compatible with standard 80C52
- Instruction-set compatible with 80C52
- Four 8-bit I/O ports; Port 0 has internal pull-up resisters enabled by software.
- One extra 4-bit I/O port with interrupt and chip-select functions
- Three 16-bit timers
- Programmable clock out
- Programmable Counter Array (PCA) with PWM, Capture, Compare and Watchdog functions
- 9 interrupt sources with 4 levels of priority
- Full-duplex serial port with framing-error detection and automatic address recognition
- 64-KB, in-system-programmable, Flash EPROM (AP Flash EPRAOM)
- 4-KB auxiliary Flash EPROM for loader program (LD Flash EPROM)
- 256-byte on-chip RAM
- 1-KB auxiliary RAM, software-selectable
- Software Reset
- 12 clocks per machine cycle operation (default). Speed up to 40 MHz.
- 6 clocks per machine cycle operation set by the writer. Speed up to 20 MHz.
- 2 DPTR registers
- Low EMI (inhibit ALE)
- Built-in power management with idle mode and power down mode
- Code protection
- Packages:
  - Lead Free (RoHS) DIP 40: W78ERD2A40DL
  - Lead Free (RoHS) PLCC 44: W78ERD2A40PL
  - Lead Free (RoHS) PQFP 44: W78ERD2A40FL

3. PIN CONFIGURATIONS

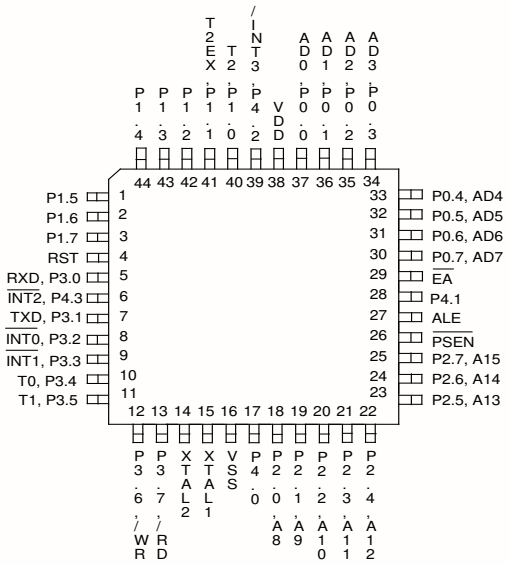
40-Pin DIP



44-Pin PLCC



44-Pin QFP



Publication Release Date: March 2, 2009
Revision A12

4. PIN DESCRIPTION

SYMBOL	TYPE*	DESCRIPTIONS
$\overline{EA}$	I	EXTERNAL ACCESS ENABLE: This pin forces the processor to execute instructions in external ROM. The ROM address and data are not presented on the bus if the $\overline{EA}$ pin is high.
$\overline{PSEN}$	O H	PROGRAM STORE ENABLE: $\overline{PSEN}$ indicates external ROM data is on the Port 0 address/data bus. If internal ROM is accessed, no $\overline{PSEN}$ strobe signal is present on this pin.
ALE	O H	ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6th of the oscillator frequency.
RST	I L	RESET: If this pin is set high for two machine cycles while the oscillator is running, the W78ERD2 is reset.
XTAL1	I	CRYSTAL 1: Crystal oscillator input or external clock input.
XTAL2	O	CRYSTAL 2: Crystal oscillator output.
V_{SS}	I	GROUND: ground potential.
V_{DD}	I	POWER SUPPLY: Supply voltage for operation.
P0.0 – P0.7	I/O D	PORT 0: 8-bit, bi-directional I/O port, the same as that of the standard 80C52. Port 0 has internal pull-up resisters enabled by software.
P1.0 – P1.7	I/O H	PORT 1: 8-bit, bi-directional I/O port, the same as that of the standard 80C52.
P2.0 – P2.7	I/O H	PORT 2: 8-bit, bi-directional I/O port with internal pull-ups. This port also provides the upper address bits when accessing external memory.
P3.0 – P3.7	I/O H	PORT 3: 8-bit, bi-directional I/O port, the same as that of the standard 80C52.
P4.0 – P4.3	I/O H	PORT 4: 4-bit, bi-directional I/O port with chip-select functions.

* **Note: TYPE** I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain

5. FUNCTIONAL DESCRIPTION

The W78ERD2 architecture consists of a core processor that supports 111 different op-codes and references 64 KB of program space and 64 KB of data space. It is surrounded by various registers; four general-purpose I/O ports; one special-purpose, programmable, 4-bit I/O port; 256 bytes of RAM; 1 KB of auxiliary RAM (AUX-RAM); three timer/counters; a serial port; and an internal 74373 latch and 74244 buffer which can be switched to port 2.

This section introduces the RAM, Timers/Counters, Clock, Power Management, Reduce EMI Emission, and Reset.

5.1 RAM

The W78ERD2 has two banks of RAM: 256 bytes of RAM and 1 KB of AUX-RAM. AUX-RAM is enabled by clearing bit 1 in the AUXR register, and it is enabled after reset. Different addresses in RAM are addressed in different ways.

- RAM 00H – 7FH can be addressed directly or indirectly, as in the 8051. The address pointers are R0 and R1 of the selected bank.
- RAM 80H – FFH can only be addressed indirectly, as in the 8051. The address pointers are R0 and R1 of the selected bank.
- AUX-RAM 00H –3FFH is addressed indirectly in the same way external data memory is accessed with the MOVX instruction. The address pointers are R0 and R1 of the selected bank and the DPTR register.
- Addresses higher than 3FFH are stored in external memory and are accessed indirectly with the MOVX instruction, as in the 8051.

When AUX-RAM is enabled, the instruction "MOVX @Ri" always accesses AUX-RAM. When the W78ERD2 is executing instructions from internal program memory, accessing AUX-RAM does not affect ports P0, P2, $\overline{WR}$ or $\overline{RD}$.

For example,

```
ANL   AUXR,#11111101B  ; Enable AUX-RAM
MOV   DPTR,#1234H
MOV   A,#56H
MOVX  @DPTR,A          ; Write 56h to address 1234H in external memory
MOV   XRAMAH,#02H      ; Only 2 LSB effective
MOV   R0,#34H
MOV   A,@R0            ; Read AUX-RAM data at address 0234H
```

5.2 Timers/Counters

The W78ERD2 has three timers/counters called Timer 0, Timer 1, and Timer 2. Each timer/counter consists of two 8-bit data registers: TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2.

The operations of Timer 0 and Timer 1 are similar to those in the W78C52, and these timers are controlled by the TCON and TMOD registers.

Timer 2 is controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. In capture or auto-reload mode, RCAP2H and RCAP2L are the reload / capture registers and the clock speed is the same as that of Timers 0 and 1.

5.3 Clock

The W78ERD2 is designed for either a crystal oscillator or an external clock.

The W78ERD2 incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2, and a load capacitor may be connected from each pin to ground. In addition, if the crystal frequency is higher than 24 MHz, a resistor should be connected between XTAL1 and XTAL2 to provide a DC bias.

An external clock is connected to pin XTAL1, while pin XTAL2 should be left disconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator. As a result, the logic-1 voltage should be higher than 3.5 V.

5.4 Power Management

The W78ERD2 provides two modes, idle mode and power-down mode, to reduce power consumption. Both modes are entered by software.

The W78ERD2 enters Idle mode when the IDL bit in the PCON register is set. In Idle mode, the internal clock for the processor stops while the internal clock for the peripherals and interrupt logic continues to run. The W78ERD2 leaves Idle mode when an interrupt or a reset occurs.

The W78ERD2 enters Power-Down mode when the PD bit in the PCON register is set. In Power-Down mode, all of the clocks are stopped, including the oscillator. The W78ERD2 leaves Power-Down mode when there is a hardware reset or by external interrupts $\overline{INT0}$ or $\overline{INT1}$, if enabled.

5.5 Reduce EMI Emission

If the crystal frequency is less than 25 MHz, set bit 7 in the option register to 0 to reduce EMI emissions. Please see Option Bits for more information.

5.6 Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running, as the W78ERD2 has a special glitch-removal circuit that ignores glitches on the reset line.

During reset, the ports are initialized to FFH, the stack pointer to 07H, and all of the other SFR to 00H, with two exceptions—SBUF does not change, and bit 4 in PCON is not cleared.

6. SPECIAL FUNCTION REGISTER

The following table identifies the Special Function Registers (SFRs) in the W78ERD2, as well as each of their addresses and reset values.

F8		CH 00000000	CCAP0H 00000000	CCAP1H 00000000	CCAP2H 00000000	CCAP3H 00000000	CCAP4H 00000000		FF
F0	+B 00000000						CHPENR 00000000		F7
E8	+P4 xxxx1111	CL 00000000	CCAP0L 00000000	CCAP1L 00000000	CCAP2L 00000000	CCAP3L 00000000	CCAP4L 00000000		EF
E0	+ACC 00000000								E7
D8	CCON x0000000	CMOD 00xxx000	CCAPM0 x0000000	CCAPM1 x0000000	CCAPM2 x0000000	CCAPM3 x0000000	CCAPM4 x0000000	CKCON xx000xx1	DF
D0	+PSW 00000000								D7
C8	+T2CON 00000000	T2MOD xxxxxx00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			CF
C0	XICON 00000000	XICONH 0xxx0xxx	P4CONA 00000000	P4CONB 00000000	SFRAL 00000000	SFRAH 00000000	SFRFD 00000000	SFRCN 00000000	C7
B8	+IP x0000000	SADEN 00000000						CHPCON 000xx000	BF
B0	+P3 11111111				P43AL 00000000	P43AH 00000000		IPH x0000000	B7
A8	+IE 00000000	SADDR 00000000			P42AL 00000000	P42AH 00000000	P4CSIN 00000000		AF
A0	+P2 11111111	XRAMAH 00000000	AUXR1 xxxxx0x0				WDTRST 00000000		A7
98	+SCON 00000000	SBUF xxxxxxxx					P2EAL 00000000	P2EAH 00000000	9F
90	+P1 11111111				P41AL 00000000	P41AH 00000000			97
88	+TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR 00000000		8F
80	+P0 11111111	SP 00000111	DPL 00000000	DPH 00000000	P40AL 00000000	P40AH 00000000	PORT 00000000	PCON 00110000	87

Notes:

1. SFRs marked with a plus sign (+) are both byte- and bit-addressable.
2. The text of SFR with bold type characters are extension function registers.

The rest of this section explains each SFR, starting with the lowest address.

Port 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

Port 0 is an open-drain, bi-directional I/O port after chip is reset. Besides, it has internal pull-up resisters enabled by setting P0UP of POPT (86H) to high. This port also provides a multiplexed, low-order address/data bus when the W78IRD2 accesses external memory.

Stack Pointer

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

The Stack Pointer stores the RAM address (scratchpad RAM, not AUX-RAM) where the stack begins. It always points to the top of the stack.

Data Pointer Low

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

This is the low byte of the standard-8052 16-bit data pointer.

Data Pointer High

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

This is the high byte of the standard-8052 16-bit data pointer.

Port 4.0 Low-Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P40AL.7	P40AL.6	P40AL.5	P40AL.4	P40AL.3	P40AL.2	P40AL.1	P40AL.0

Mnemonic: P40AL Address: 84h

Port 4.0 High-Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P40AH.7	P40AH.6	P40AH.5	P40AH.4	P40AH.3	P40AH.2	P40AH.1	P40AH.0

Mnemonic: P40AH Address: 85h

Port Option Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	P0UP

Mnemonic: POPT Address: 86h

BIT	NAME	FUNCTION
1 – 7	-	Reserve
0	P0UP	0: Port 0 pins are open-drain. 1: Port 0 pins are internally pulled-up. Port 0 is structurally the same as Port 2.

Power Control

Bit:	7	6	5	4	3	2	1	0
	SMOD	SMOD0	-	POR	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: Double the serial-port baud rate in serial port modes 1, 2, and 3.
6	SMOD0	0: Framing Error Detection Disable. SCON.7 acts as per the standard 8052 function. 1: Framing Error Detection Enable. SCON.7 indicates a Frame Error and acts as the FE (FE_1) flag.
5	-	Reserved
4	POF	This bit is set to 1 when a power-on reset has occurred. It can be cleared by software.
3	GF1	General-purpose flag.
2	GF0	General-purpose flag.
1	PD	Set this bit to 1 to go into POWER DOWN mode.
0	IDL	Set this bit to 1 to go into IDLE mode.

Timer Control

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 overflow flag: This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. It can also be set or cleared by software.
6	TR1	1: Turn on Timer 1. 0: Turn off Timer 1.
5	TF0	Timer 0 overflow flag: This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. It can also be set or cleared by software.
4	TR0	1: Turn on Timer 0. 0: Turn off Timer 0.
3	IE1	Interrupt 1 Edge Detect: This bit is set by the hardware when a falling-edge / low-level is detected on $\overline{INT1}$. If $\overline{INT1}$ is edge-triggered, this bit is cleared by the hardware when the interrupt service routine begins. Otherwise, it follows the pin.
2	IT1	Interrupt 1 type control 1: Interrupt 1 is triggered by a falling-edge on $\overline{INT1}$. 0: Interrupt 1 is triggered by a low-level on $\overline{INT1}$.
1	IE0	Interrupt 0 Edge Detect: This bit is set by the hardware when a falling-edge / low-level is detected on $\overline{INT0}$. If $\overline{INT0}$ is edge-triggered, this bit is cleared by the hardware when the interrupt service routine begins. Otherwise, it follows the pin.
0	IT0	Interrupt 0 type control 1: Interrupt 0 is triggered by a falling-edge on $\overline{INT0}$. 0: Interrupt 0 is triggered by a low-level on $\overline{INT0}$.

Timer Mode Control

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/Counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 is set.
6	C/$\overline{T}$	Timer or Counter Select: When cleared, Timer 1 is incremented by the internal clock. When set, Timer 1 counts falling edges on the T1 pin.
5	M1	Timer 1 Mode Select bits: See below.
4	M0	Timer 1 Mode Select bits: See below.

Continued

BIT	NAME	FUNCTION
3	GATE	Gating control: When this bit is set, Timer/Counter 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 is set.
2	C/$\overline{T}$	Timer or Counter Select: When cleared, Timer 0 is incremented by the internal clock. When set, Timer 0 counts falling edges on the T0 pin.
1	M1	Timer 0 Mode Select bits: See below.
0	M0	Timer 0 Mode Select bits: See below.

M1, M0: Mode Select bits:

M1	M0	Mode
0	0	Mode 0: 8048 timer, TLx serves as 5-bit pre-scale.
0	1	Mode 1: 16-bit timer/counter, no pre-scale.
1	0	Mode 2: 8-bit timer/counter with auto-reload from THx
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer-0 control bits. TH0 is an 8-bit timer only controlled by Timer-1 control bits. (Timer 1) Timer/Counter 1 is stopped.

Timer 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

TL0.7-0: Timer 0 Low byte

Timer 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

TL1.7-0: Timer 1 Low byte

Timer 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

TH0.7-0: Timer 0 High byte

Timer 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

TH1.7-0: Timer 1 High byte

Auxiliary Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	EXTRAM	ALEOFF

Mnemonic: AUXR Address: 8Eh

BIT	NAME	FUNCTION
7~2	-	Reserve
1	EXTRAM	0 = Enable AUX-RAM 1 = Disable AUX-RAM
0	ALEOFF	0: ALE expression is enabled. 1: ALE expression is disabled.

Port 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7-0: General-purpose input/output port. Port-read instructions read the port pins, while read-modify-write instructions read the port latch.

Port 4.1 Low Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P41AL.7	P41AL.6	P41AL.5	P41AL.4	P41AL.3	P41AL.2	P41AL.1	P41AL.0

Mnemonic: P41AL Address: 94h

Port 4.1 High Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P41AH.7	P41AH.6	P41AH.5	P41AH.4	P41AH.3	P41AH.2	P41AH.1	P41AH.0

Mnemonic: P41AH Address: 95h

Serial Port Control

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial port, Mode 0 (SM0) bit or Framing-Error (FE) Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. SM0 is described with SMI1 below. When used as FE, this bit indicates whether the stop bit is invalid (FE=1) or valid (FE=0). This bit must be manually cleared by software.
6	SM1	Serial port, Mode 1 (SM1) bit: Mode: SM0 SM1 Description Length Baud rate 0 0 0 Synchronous 8 6(6T mode)/12(12T mode) T_{clk} 1 0 1 Asynchronous 10 Variable 2 1 0 Asynchronous 11 32/16(6T mode) or 64/32(12T mode) T_{clk} 3 1 1 Asynchronous 11 Variable
5	SM2	Multi-processor communication. (Modes 2 and 3) Set this bit to enable the multi-processor communication feature. With this feature, RI is not activated if the ninth data bit received (RB8) is 0. (Mode 1) Set this bit to 1 to keep RI de-activated if a valid stop bit is not received. (Mode 0) SM2 controls the serial port clock. If clear, the serial port runs at 1/12 the oscillator. This is compatible with the standard 8052.
4	REN	Receive enable: 1 = Serial reception is enabled 0 = Serial reception is disabled
3	TB8	(Modes 2 and 3) This is the ninth bit to be transmitted. This bit is set and cleared by software as desired.
2	RB8	(Modes 2 and 3) This is the ninth data bit that was received. (Mode 1) If SM2 is 0, RB8 is the stop bit that was received. (Mode 0) No function.
1	TI	Transmit interrupt flag: This flag is set by the hardware at the end of the eighth bit in mode 0 or at the beginning of the stop bit in modes 1 – 3 during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by the hardware at the end of the eighth bit in mode 0 or halfway through the stop bit in modes 1 – 3 during serial reception. However, SM2 restricts this bit. This bit can be cleared only by software.

Serial Data Buffer

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

BIT	NAME	FUNCTION
7~0	SBUF	Serial port data is read from or written to this location. It actually consists of two separate, internal 8-bit registers, the receive register and the transmit buffer. Any read access reads data from the receive register, while write access writes to the transmit buffer.

Port 2

Bit:	7	6	5	4	3	2	1	0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

Mnemonic: P2 Address: A0h

Ram High Byte Address

Bit:	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	XRAMAH.1	XRAMAH.0

Mnemonic: XRAMAH Address: A1h

The AUX-RAM high byte address

Auxiliary 1 Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	GF2	0	-	DPS

Mnemonic: AUXR1 Address: A2h

BIT	NAME	FUNCTION
7~4	-	Reserved
3	GF2	General purpose, user–defined flag.
2	0	The bit cannot be written and is always read as 0.
1	-	Reserved
0	DPS	0 = switch to DPTR0 1 = switch to DPTR1

Watchdog Timer Reset Register

Bit:	7	6	5	4	3	2	1	0
	WDTRST.7	WDTRST.6	WDTRST.5	WDTRST.4	WDTRST.3	WDTRST.2	WDTRST.1	WDTRST.0

Mnemonic: WDTRST Address: A6h

Interrupt Enable

Bit:	7	6	5	4	3	2	1	0
	EA	EC	ET2	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

BIT	NAME	FUNCTION
7	EA	Global interrupt enable. Enable/disable all interrupts except for PFI.
6	EC	Enable PCA interrupt.
5	ET2	Enable Timer 2 interrupt.
4	ES	Enable Serial port interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt $\overline{INT1}$.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt $\overline{INT0}$.

SLAVE ADDRESS

Bit:	7	6	5	4	3	2	1	0

Mnemonic: SADDR Address: A9h

BIT	NAME	FUNCTION
7~0	SADDR	The SADDR should be programmed to the given or broadcast address for serial port to which the slave processor is designated.

Port 4.2 Low Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P42AL.7	P42AL.6	P42AL.5	P42AL.4	P42AL.3	P42AL.2	P42AL.1	P42AL.0

Mnemonic: P42AL Address: Ach

Port 4.2 High Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P42AH.7	P42AH.6	P42AH.5	P42AH.4	P42AH.3	P42AH.2	P42AH.1	P42AH.0

Mnemonic: P42AH Address: ADh

Port 4 CS Inverse

Bit:	7	6	5	4	3	2	1	0
	P43INV	P42INV	P41INV	P40INV	0	0	0	0

Mnemonic: P4CSIN Address: AEh

BIT	NAME	FUNCTION
7~4	P4xINV	The active polarity of P4.x which functions chip-select signal. 1: Active high 0: Active low
3~0	-	Reserved and must be set zero.

Port 3

Bit:	7	6	5	4	3	2	1	0
	P3.7	P32.6	P3.5	P32.4	P3.3	P3.2	P3.1	P3.0

Mnemonic: P3 Address: B0h

Port 4.3 Low Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P43AL.7	P43AL.6	P43AL.5	P43AL.4	P43AL.3	P43AL.2	P43AL.1	P43AL.0

Mnemonic: P43AL Address: B4h

Port 4.3 High Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P43AH.7	P43AH.6	P43AH.5	P43AH.4	P43AH.3	P43AH.2	P43AH.1	P43AH.0

Mnemonic: P43AH Address: B5h

Interrupt Priority High

Bit:	7	6	5	4	3	2	1	0
	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Mnemonic: IPH Address: B8h

BIT	NAME	FUNCTION
7	-	This bit is not implemented and is always read high.
6	PPCH	1: Set the priority of the PCA interrupt to the highest level.

5	PT2H	1: Set the priority of the Timer 2 interrupt to the highest level.
4	PSH	1: Set the priority of the Serial Port interrupt to the highest level.
3	PT1H	1: Set the priority of the Timer 1 interrupt to the highest level.
2	PX1H	1: Set the priority of external interrupt $\overline{INT1}$ to the highest level.
1	PT0H	1: Set the priority of the Timer 0 interrupt to the highest level.
0	PX0H	1: Set the priority of external interrupt $\overline{INT0}$ to the highest level.

Interrupt Priority

Bit:	7	6	5	4	3	2	1	0
	-	PPC	PT2	PS	PT1	PX1	PT0	PX0

Mnemonic: IP Address: B8h

BIT	NAME	FUNCTION
7	-	This bit is not implemented and is always read high.
6	PPC	1: Set the priority of the PCA interrupt one level higher.
5	PT2	1: Set the priority of the Timer 2 interrupt one level higher.
4	PS	1: Set the priority of the Serial Port interrupt one level higher.
3	PT1	1: Set the priority of the Timer 1 interrupt one level higher.
2	PX1	1: Set the priority of external interrupt $\overline{INT1}$ one level higher.
1	PT0	1: Set the priority of the Timer 0 interrupt one level higher.
0	PX0	1: Set the priority of external interrupt $\overline{INT0}$ one level higher.

Slave Address Mask Enable

Bit:	7	6	5	4	3	2	1	0

Mnemonic: SADEN Address: B9h

BIT	NAME	FUNCTION
7~0	SADEN	This register enables the Automatic Address Recognition feature of the serial port. When a bit in SADEN is set to 1, the same bit in SADDR is compared to the incoming serial data. When a bit in SADEN is set to 0, the same bit in SADDR is a "don't care" value in the comparison. The serial port interrupt occurs only if all the SADDR bits where SADEN is set to 1 match the incoming serial data.

On-Chip Programming Control

Bit:	7	6	5	4	3	2	1	0
	SWRST/ REBOOT	-	-	-	-	0	FBOOTSL	FPROGEN

Mnemonic: CHPCON Address: BFh

BIT	NAME	FUNCTION
7	W: SWRESET R: REBOOT	When FBOOTSL and FPROGEN are set to 1, set this bit to 1 to force the microcontroller to reset to the initial condition, just like power-on reset. This action re-boots the microcontroller and starts normal operation. Read this bit to determine whether or not a hardware reboot is in progress.
6 – 2	-	Reserved
1	FBOOTSL	Program Location Selection. This bit should be set before entering ISP mode. 0: The Loader Program is in the 64-KB AP Flash EPROM. The 4-KB LD Flash EPROM is the destination for re-programming. 1: The Loader Program is in the 4-KB memory bank. The 64-KB AP Flash EPROM is the destination for re-programming.
0	FPROGEN	FLASH EPROM Programming Enable. 1: Enable in-system programming mode. In this mode, erase, program and read operations are achieved during device enters idle state. 0: Disable in-system programming mode. The on-chip flash memory is read-only.

CHPCON has an unrestricted read access, however, the write access is protected by timed-access protection. See the section of timed-access protection for more information.

External Interrupt Control

Bit:	7	6	5	4	3	2	1	0
	PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

Mnemonic: XICON Address: C0h

BIT	NAME	FUNCTION
7	PX3	1: Set the priority of external interrupt $\overline{INT3}$ one level higher.
6	EX3	1: Enable external interrupt $\overline{INT3}$.
5	IE3	Interrupt $\overline{INT3}$ flag. This bit is set and cleared automatically by the hardware when the interrupt is detected and processed.
4	IT3	1: $\overline{INT3}$ is falling-edge triggered 0: $\overline{INT3}$ is low-level triggered
3	PX2	1: Set the priority of external interrupt $\overline{INT2}$ one level higher.
2	EX2	1: Enable external interrupt $\overline{INT2}$.
1	IE2	Interrupt $\overline{INT2}$ flag. This bit is set and cleared automatically by the hardware when the interrupt is detected and processed.
0	IT2	1: $\overline{INT2}$ is falling-edge triggered 0: $\overline{INT2}$ is low-level triggered

External Interrupt High Control

Bit:	7	6	5	4	3	2	1	0
	PXH3	-	-	-	PXH2	-	-	-

Mnemonic: XICONH Address: C1h

BIT	NAME	FUNCTION
7	PXH3	1: Set the priority of external interrupt $\overline{INT3}$ to the highest level.
6 - 4	-	Reserved
3	PXH2	1: Set the priority of external interrupt $\overline{INT2}$ to the highest level.
2 - 0	-	Reserved

Port 4 Control Register A

Bit:	7	6	5	4	3	2	1	0
	P41FUN1	P41FUN0	P41CMP1	P41CMP0	P40FUN1	P40FUN0	P40CMP1	P40CMP0

Mnemonic: P4CONA Address: C2h

BIT	NAME	FUNCTION
7, 6	P41FUN1 P41FUN0	P4.1 function control bits, similar to P43FUN1 and P43FUN0 below.
5, 4	P41CMP1 P41CMP0	P4.1 address-comparator length control bits, similar to P43CMP1 and P43CMP0 below.
3, 2	P40FUN1 P40FUN0	P4.0 function control bits, similar to P43FUN1 and P43FUN0 below.
1, 0	P40CMP1 P40CMP0	P4.0 address-comparator length control bits, similar to P43CMP1 and P43CMP0 below.

Port 4 Control Register B

Bit:	7	6	5	4	3	2	1	0
	P43FUN1	P43FUN0	P43CMP1	P43CMP0	P42FUN1	P42FUN0	P42CMP1	P42CMP0

Mnemonic: P4CONB Address: C3h

BIT	NAME	FUNCTION
7, 6	P43FUN1 P43FUN0	00: Mode 0. P4.3 is a general purpose I/O port, like Port 1. 01: Mode 1. P4.3 is a read-strobe signal for chip-select purposes. The address range depends on SFR P43AH, P43AL, P43CMP1 and P43CMP0. 10: Mode 2. P4.3 is a write-strobe signal for chip-select purposes. The address range depends on SFR P43AH, P43AL, P43CMP1 and P43CMP0. 11: Mode 3. P4.3 is a read/write-strobe signal for chip-select purposes. The address range depends on SFR P43AH, P43AL, P43CMP1, and P43CMP0.
5, 4	P43CMP1 P43CMP0	Chip-select signal address comparison: 00: Compare the full 16-bit address with P43AH and P43AL. 01: Compare the 15 MSB of the 16-bit address with P43AH and P43AL. 10: Compare the 14 MSB of the 16-bit address with P43AH and P43AL. 11: Compare the 8 MSB of the 16-bit address with P43AH.
3, 2	P42FUN1 P42FUN0	P4.2 function control bits, similar to P43FUN1 and P43FUN0 above.
1, 0	P42CMP1 P42CMP0	P4.2 address-comparator length control bits, similar to P43CMP1 and P43CMP0 above.

F/W Flash Low Address

Bit:	7	6	5	4	3	2	1	0

Mnemonic: SFRAL Address: C4h

F/W flash low byte address

F/W Flash High Address

Bit:	7	6	5	4	3	2	1	0

Mnemonic: SFRAH Address: C5h

F/W flash high byte address

F/W Flash Data

Bit:	7	6	5	4	3	2	1	0

Mnemonic: SFRFD Address: C6h

F/W flash data

F/W Flash Control

Bit:	7	6	5	4	3	2	1	0
	0	WFWIN	OEN	CEN	CTRL3	CTRL2	CTRL1	CTRL0

Mnemonic: SFRCN Address: C7h

BIT	NAME	FUNCTION
7	-	Reserved
6	WFWIN	On-chip Flash EPROM bank select for in-system programming. This bit should be defined by the loader program in ISP mode. 0: 64-KB Flash EPROM is the destination for re-programming. 1: 4-KB Flash EPROM is the destination for re-programming.
5	OEN	Flash EPROM output enable.
4	CEN	Flash EPROM chip enable.
3 - 0	CTRL[3:0]	Flash control signals

Timer 2 Control

Bit:	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2

Mnemonic: T2CON Address: C8h

BIT	NAME	FUNCTION
7	TF2	Timer 2 overflow flag: If RCLK and TCLK are 0, this bit is set when Timer 2 overflows or when the count is equal to the value in the capture register in down-count mode. This bit can also be set by software, and it can only be cleared by software.
6	EXF2	Timer 2 External Flag: When Timer 2 is in either capture or auto-reload mode and DCEN is 0, a negative transition on the T2EX pin (P1.1) and EXEN2=1 sets this flag. This flag can also be set by software. Once set, this flag generates a Timer-2 interrupt, if enabled, and it must be cleared by software.
5	RCLK	Receive Clock Flag: Set this bit to force Timer 2 into baud-rate generator mode when receiving data on the serial port in modes 1 or 3. 1 = Timer 2 overflow is the time base. 0 = Timer 1 overflow is the time base.
4	TCLK	Transmit clock Flag: Set this bit to force Timer 2 into baud-rate generator mode when transmitting data on the serial port in modes 1 or 3. 1 = Timer 2 overflow is the time base. 0 = Timer 1 overflow is the time base.

Continued

BIT	NAME	FUNCTION
3	EXEN2	Timer 2 External Enable: If Timer 2 is not in baud-rate generator mode (see RCLK and TCLK above), set this bit to allow a negative transition on the T2EX pin to capture/reload Timer 2 counter.
2	TR2	Timer 2 Run Control: 1 = Enable Timer 2. 0 = Disable Timer 2, which preserves the current value in TH2 and TL2.
1	C/T2	Counter/Timer select: 0 = Timer 2 operates as a timer at a speed controlled by T2M (CKCON.5) 1 = Timer 2 counts negative edges on the T2EX pin.
0	CP/RL2	Capture/Reload Select: If EXEN2 is set to 1, this bit determines whether the capture or auto-reload function is activated. 0 = auto-reload when timer 2 overflows or a falling edge is detected on T2EX 1 = capture each falling edge is detected on T2EX If either RCLK or TCLK is set, this bit has no function, as Timer 2 runs in auto-reload mode.

Timer 2 Mode

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	T2OE	DCEN

Mnemonic: T2MOD Address: C9h

BIT	NAME	FUNCTION
7~2	-	Reserved
1	T2OE	Timer 2 Output Enable. This bit enables/disables the Timer 2 clock-out function.
0	DCEN	Down Count Enable: Setting DCEN to 1 allows T2EX pin to control the direction that Timer 2 counts in 16-bit auto-reload mode.

Timer 2 Capture Low

Bit:	7	6	5	4	3	2	1	0
	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0

Mnemonic: RCAP2L Address: CAh

RCAP2L Timer 2 Capture LSB: In capture mode, RCAP2L is used to capture the TL2 value. In auto-reload mode, RCAP2L is used as the LSB of the 16-bit reload value.

Timer 2 Capture High

Bit:	7	6	5	4	3	2	1	0
	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0

Mnemonic: RCAP2H Address: CBh

RCAP2H Timer 2 Capture HSB: In capture mode, RCAP2H is used to capture the TH2 value. In auto-reload mode, RCAP2H is used as the MSB of the 16-bit reload value.

Timer 2 Register Low

Bit:	7	6	5	4	3	2	1	0
	TL2.7	TL2.6	TLH2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0

Mnemonic: TL2 Address: CCh

TL2 Timer 2 LSB

Timer 2 Register High

Bit:	7	6	5	4	3	2	1	0
	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0

Mnemonic: TH2 Address: CDh

TL2 Timer 2 MSB

Program Status Word

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

Mnemonic: PSW Address: D0h

BIT	NAME	FUNCTION
7	CY	Carry flag: Set when an arithmetic operation results in a carry being generated from the ALU. It is also used as the accumulator for bit operations.
6	AC	Auxiliary carry: Set when the previous operation resulted in a carry from the high order nibble.
5	F0	General–purpose, user-defined flag 0.
4	RS1	Register bank select bits: See below.
3	RS0	Register bank select bits: See below.
2	OV	Overflow flag: Set when a carry was generated from the seventh bit but not from the eighth bit as a result of the previous operation, or vice-versa.
1	F1	General–purpose, user-defined flag 1.
0	P	Parity flag: Set and cleared by the hardware to indicate an odd or even number, respectively, of 1's in the accumulator.

RS.1-0: Register bank select bits:

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

PCA Counter Control Register

Bit:	7	6	5	4	3	2	1	0
	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0

Mnemonic: CCON Address: D8h

PCA Counter Mode Register

Bit:	7	6	5	4	3	2	1	0
	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF

Mnemonic: CMOD Address: D9h

PCA Module 0 Register

Bit:	7	6	5	4	3	2	1	0
	-	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0

Mnemonic: CCAPM0 Address: DAh

PCA Module 1 Register

Bit:	7	6	5	4	3	2	1	0
	-	ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1

Mnemonic: CCAPM1 Address: DBh

PCA Module 2 Register

Bit:	7	6	5	4	3	2	1	0
	-	ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2

Mnemonic: CCAPM2 Address: DCh

PCA Module 3 Register

Bit:	7	6	5	4	3	2	1	0
	-	ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3

Mnemonic: CCAPM3 Address: DDh