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8-BIT MICROCONTROLLER

Table of Contents-

1.	GENERAL DESCRIPTION.....	3
2.	FEATURES	3
3.	PIN CONFIGURATION	4
4.	PIN DESCRIPTION.....	5
5.	FUNCTIONAL DESCRIPTION.....	6
5.1	I/O Ports	6
5.2	Serial I/O	6
5.3	Timers	6
5.4	Interrupts.....	6
5.5	Power Management.....	7
5.6	Memory Organization.....	7
6.	SPECIAL FUNCTION REGISTERS.....	8
7.	INSTRUCTION.....	30
7.1	Instruction Timing.....	30
8.	POWER MANAGEMENT	36
8.1	Idle Mode	36
8.2	Power Down Mode.....	36
8.3	Reset Conditions.....	37
9.	INTERRUPTS	39
10.	PROGRAMMABLE TIMERS/COUNTERS.....	40
10.1	Timer/Counters 0 and 1	40
10.2	Timer/Counter 2.....	42
11.	WATCHDOG TIMER	45
12.	SERIAL PORT.....	48
12.1	Mode 0	48
12.2	Mode 1	49
12.3	Mode 2	50
12.4	Mode 3	51
12.5	Framing Error Detection.....	53
12.6	Multiprocessor Communications.....	53
13.	PULSE-WIDTH-MODULATED (PWM) OUTPUTS.....	55
14.	ANALOG-TO-DIGITAL CONVERTER (ADC)	57
15.	TIMED-ACCESS PROTECTION	59

16.	H/W REBOOT MODE (BOOT FROM 4K BYTES OF LD FLASH EPROM)	61
17.	IN-SYSTEM PROGRAMMING	62
18.	SECURITY BITS	63
19.	THE PERFORMANCE CHARACTERISTIC OF ADC	64
20.	ELECTRICAL CHARACTERISTICS	65
20.1	Absolute Maximum Ratings	65
20.2	DC Characteristics	65
20.3	ADC DC Electrical Characteristics	67
20.4	AC Characteristics	67
21.	TYPICAL APPLICATION CIRCUITS	73
22.	PACKAGE DIMENSIONS	75
23.	IN-SYSTEM PROGRAMMING SOFTWARE EXAMPLES	77
24.	REVISION HISTORY	83

1. GENERAL DESCRIPTION

The W79E201 is a fast, 8051/52-compatible microcontroller with a redesigned processor core that eliminates wasted clock and memory cycles. Typically, the W79E201 executes instructions 1.5 to 3 times faster than that of the traditional 8051/52, depending on the type of instruction, and the overall performance is about 2.5 times better at the same crystal speed. As a result, with the fully-static CMOS design, the W79E201 can accomplish the same throughput with a lower clock speed, reducing power consumption.

The W79E201 provides one eight-bit digital/analog input port (Port 1) that includes a ten-bit ADC; three eight-bit, bi-directional and bit-addressable I/O ports; a one-bit port P4.0 for external ISP reboot; three 16-bit timers / counters; and one serial port. These peripherals are supported by an eight-source, two-level interrupt capability.

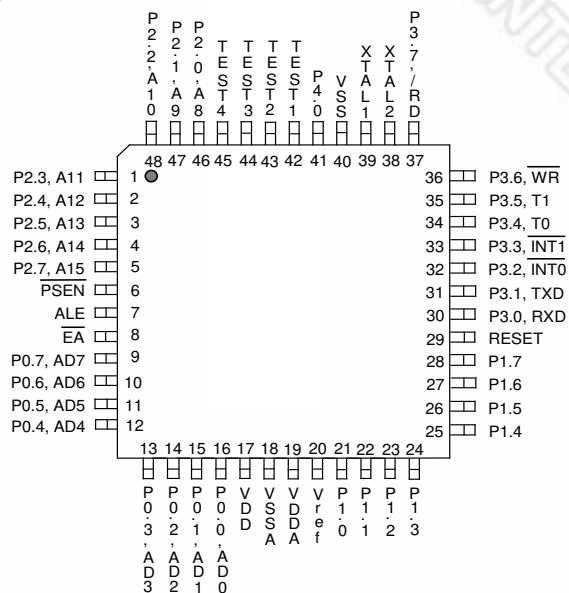
To facilitate programming and verification, the W79E201 contains In-System Programmable (ISP) 16-KB AP Flash EPROM; 4-KB LD Flash EPROM for the loader program in ISP mode; and 256 bytes of RAM. The Flash EPROM allows the program memory to be read and programmed electronically. Once the code is confirmed, it can be protected for security.

2. FEATURES

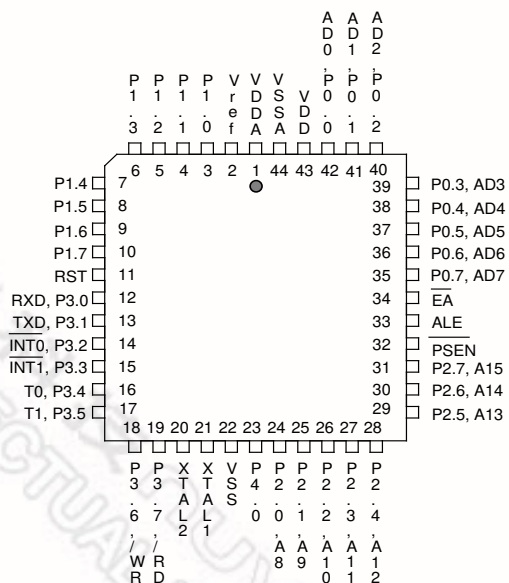
- Fully-static-design 8-bit Turbo 51 CMOS microcontroller up to 16MHz
- 16KB of in-system-programmable Flash EPROM (AP Flash EPROM)
- 4 KB of Auxiliary Flash EPROM for the loader program (LD Flash EPROM)
- 256 bytes of on-chip RAM
- Instruction-set compatible with MSC-51
- Three 8-bit bi-directional ports
- Three 16-bit timers / counters
- 8 interrupt sources with two levels of priority
- One enhanced full-duplex serial port with framing-error detection and automatic address recognition
- Port 0 internal pull-up resistor optional
- Programmable Watchdog Timer
- 6-channel PWM
- Software-programmable access cycle to external RAM/peripherals
- 10-bit ADC with eight-channel analog input or digital input port
- Development Tools:
 - JTAG ICE(In Circuit Emulation) tool
- Packages:
 - Lead Free (RoHS) PLCC 44: W79E201A16PL
 - Lead Free (RoHS) QFP 44: W79E201A16FL
 - Lead Free (RoHS) LQFP 48: W79E201A16LL

3. PIN CONFIGURATION

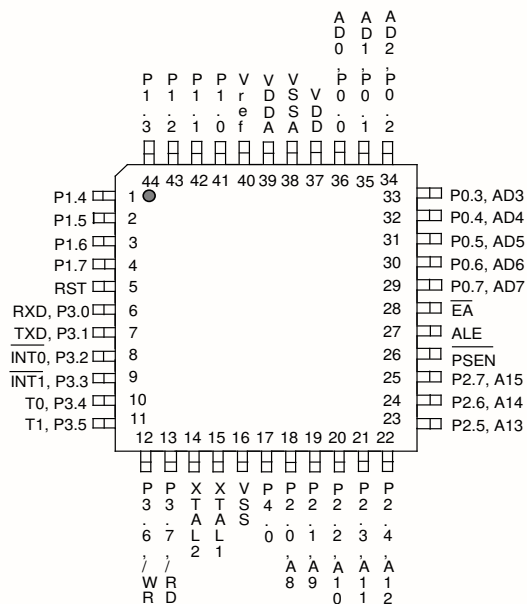
48-Pin LQFP



44-Pin PLCC



44-Pin QFP



4. PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTIONS
\overline{EA}	I H	EXTERNAL ACCESS ENABLE: This pin forces the processor to execute from external ROM. It should be kept high to access internal ROM. Note: The ROM address and data are present on the bus, unless the \overline{EA} pin is high and the program counter is within the 16-KB area for internal ROM.
\overline{PSEN}	O H	PROGRAM STORE ENABLE: \overline{PSEN} enables external ROM devices when data is on the Port-0 address / data bus during fetch and MOVC operations. When internal ROM is accessed, \overline{PSEN} is driven high.
ALE	O H	ADDRESS LATCH ENABLE: ALE enables the address latch that separates the address from the data on Port 0.
RST	I L	RESET: Set this pin high for two machine cycles while the oscillator is running to reset the device.
XTAL1	I	CRYSTAL1: Crystal oscillator input. It may be driven by an external clock.
XTAL2	O	CRYSTAL2: Crystal oscillator output. It is the inversion of XTAL1.
V_{SS}	P	Digital GROUND: Ground potential
V_{DD}	P	Digital POWER SUPPLY: Supply voltage for digital operations.
AV_{DD}	P	Analog POWER SUPPLY: Supply voltage for analog operations.
AV_{SS}	P	Analog GROUND.
Vref	P	Vref: Maximum ADC voltage of analog reference input.
P0.0–P0.7	I/O D(H)	PORT 0: Port 0 is an open-drain, bi-directional I/O port. There is an internal pull-up resistor option that is enabled by bit 0 of P0R (8Fh). This port also provides a multiplexed, low-order address / data bus during accesses to external memory.
P1.0–P1.7	I	PORT 1: Port 1 is an input port only. This port is also used for 8 channels of analog inputs from ADC0 to ADC7. Furthermore, P1.1 and P1.0 serves T2 and T2EX functions.
P2.0–P2.7	I/O	PORT 2: Port 2 is a bi-directional I/O port with weak internal pull-up resistors. This port also provides the upper address bits during accesses to external memory.
P3.0–P3.7	I/O	PORT 3: Port 3 is a bi-directional I/O port with weak internal pull-up resistors. Its function is the same as that in the standard 8051/52.
P4.0	I/O	PORT 4: A bi-directional I/O port with weak internal pull-up resistors.
TEST1~4	I L	TEST1~4: The TEST pins

* **TYPE:** P: power, I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open-drain.

5. FUNCTIONAL DESCRIPTION

The W79E201 is instruction-set-compatible, though not pin-compatible, with the 8051/52. It includes most of the standard features of the 8051/52, such as three eight-bit I/O ports, one eight-bit digital or analog input port, three 16-bit timers / counters, one full-duplex serial port and interrupt sources, and it has a few extra peripherals and features as well.

The W79E201 features a redesigned, eight-bit core processor that eliminates wasted clock and memory cycles. It improves the speed and performance not just by running at high frequency but also by reducing the machine-cycle duration from the standard-8051/52 period of twelve clock cycles to four clock cycles for the majority of instructions. This improves the performance by an average of 1.5 to 3 times. The W79E201 can also adjust the duration of the MOVX instruction, anywhere from two machine cycles to nine machine cycles, to work efficiently with fast and slow external RAM and peripheral devices.

5.1 I/O Ports

The W79E201 has one eight-bit digital or analog input port, three eight-bit I/O ports and one extra, one-bit port at P4.0.

Port 0 can also be used as an address / data bus when a program is running in external memory or when external memory or devices are accessed by MOVC or MOVX instructions. In these cases, it has strong pull-up and pull-down resistors and does not need any external resistors. Otherwise, it can be used as a general I/O port with open-drain circuits.

Port 1 is the only input port that can be connected to the ADC. Port 2 is used chiefly as the upper eight bits of the address bus when port 0 is used as an address / data bus, and, as an address bus, it also has strong pull-up and pull-down resistors. Port 3 acts as an I/O port with additional, alternative functions, and Port 4.0 is a general-purpose I/O port similar to Port 3.

5.2 Serial I/O

The W79E201 has one enhanced serial port that is functionally similar to the original 8051/52 serial port. However, the W79E201 serial port can operate in different modes to obtain timing similarity as well. It also has two enhancements, Automatic Address Recognition and Frame Error Detection.

5.3 Timers

The W79E201 has three 16-bit timers that are functionally similar to the timers of the 8051/52 family. When used as timers, they can run at either four clocks or twelve clocks per count, thus providing the user with the option of emulating the timing of the original 8051/52. The W79E201 also has a Watchdog Timer that acts as a system monitor or a long-period timer.

5.4 Interrupts

The Interrupt structure in the W79E201 is slightly different from that of the standard 8051/52. Because of additional features and peripherals, the number of interrupt sources and vectors is higher. The W79E201 provides eight interrupt resources—two external interrupt sources, three timer interrupts, one serial I/O interrupt, one ADC interrupt and one watchdog timer interrupt—with two priority levels.

5.5 Power Management

Like the standard 8051/52, the W79E201 has IDLE and POWER DOWN modes of operation. In POWER DOWN mode, all of the peripheral clocks are stopped, and chip operation stops completely. This mode consumes the least amount of power.

5.6 Memory Organization

The W79E201 separates memory into two sections, Program Memory and Data Memory. Program Memory stores instruction op-codes, while Data Memory stores data or memory-mapped devices.

Program Memory

On the standard 8051/52, only 64 KB of Program Memory can be addressed, and, in the W79E201, this area is the 16-KB Flash EPROM (AP Flash EPROM). All instructions are fetched from this area, and the MOVC instruction can also access this region. There is an auxiliary 4-KB Flash EPROM (LD Flash EPROM), where the loader program for In-System Programming (ISP) resides. The AP Flash EPROM is re-programmed by serial or parallel download according to this loader program.

Data Memory

The W79E201 can access up to 64 KB of external Data Memory. This memory is accessed by MOVX instructions, and any MOVX instructions to 0000H through FFFFH go to the expanded bus on Ports 0 and 2. This is the default condition.

The W79E201 also has the standard 256 bytes of on-chip Scratchpad RAM. This can be accessed either by direct addressing or by indirect addressing. There are also some Special Function Registers (SFRs), which can only be accessed by direct addressing. Since the Scratchpad RAM is only 256 bytes, it can be used only when data contents are small.

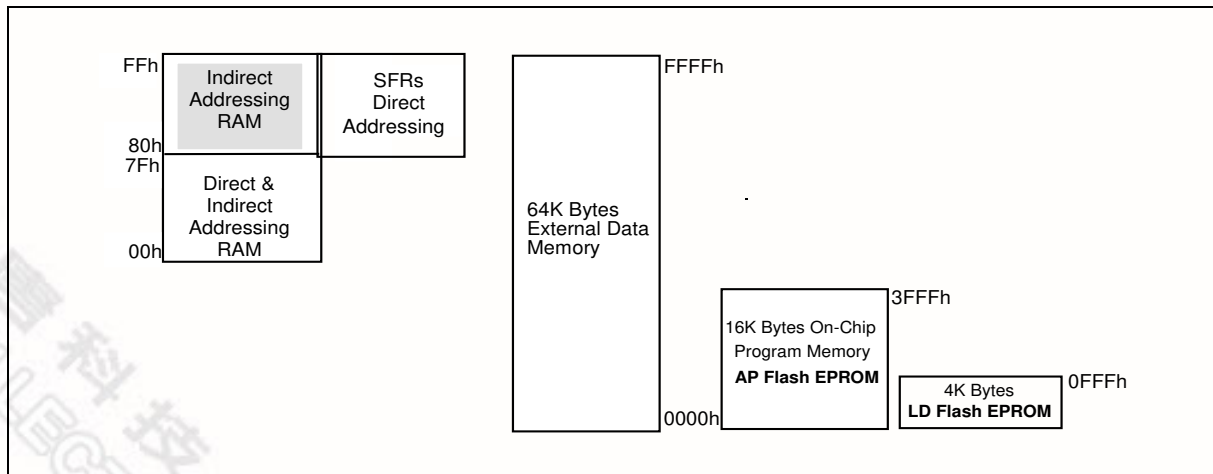


Figure 5-1 Memory Map

6. SPECIAL FUNCTION REGISTERS

The W79E201 uses Special Function Registers (SFR) to control and monitor peripherals. The SFR reside in register locations 80-FFh and are only accessed by direct addressing. The W79E201 contains all the SFR present in the standard 8051/52, as well as some additional SFR, and, in some cases, unused bits in the standard 8051/52 have new functions. SFR whose addresses end in 0 or 8 (hex) are bit-addressable. The following table of SFR is condensed, with eight locations per row. Empty locations indicate that there are no registers at these addresses. When a bit or register is not implemented, it reads high.

Table 1 Special Function Register Location Table

F8	EIP							
F0	B							
E8	EIE							
E0	ACC	ADCCON	ADCH		ADCCEN			
D8	WDCON	PWMP	PWM0	PWM1	PWMCON1	PWM2	PWM3	
D0	PSW							
C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	PWMCON2	PWM4
C0				PWM5	PMR	Status		TA
B8	IP	SADEN						
B0	P3							
A8	IE	SADDR			SFRAL	SFRAH	SFRFD	SFRCN
A0	P2					P4		
98	SCON	SBUF						CHPCON
90	P1							
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	P0R
80	P0	SP	DPL	DPH				PCON

Note: The SFRs in the column with dark borders are bit-addressable.

Port 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0

Address: 80h

Port 0 is an open-drain, bi-directional I/O port after chip is reset. Besides, it has internal pull-up resistors enabled by setting P0UP of P0R (8FH) to high. This port also provides a multiplexed, low-order address/data bus when the W79E201 accesses external memory.

Stack Pointer

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP

Address: 81h

The Stack Pointer stores the address in Scratchpad RAM where the stack begins. It always points to the top of the stack.

Data Pointer Low

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL

Address: 82h

This is the low byte of the standard-8051/52, 16-bit data pointer.

Data Pointer High

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH

Address: 83h

This is the high byte of the standard-8051/52, 16-bit data pointer.

Power Control

Bit:	7	6	5	4	3	2	1	0
	SMOD	SMOD0	-	-	GF1	GF0	PD	IDL

Mnemonic: PCON

Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: This bit doubles the serial-port baud rate in modes 1, 2 and 3.
6	SMOD0	0: Disable Framing Error Detection. SCON.7 acts as per the standard 8051/52 function. 1: Enable Framing Error Detection. SCON.7 indicates a Frame Error and acts as the FE flag.
5-4	-	Reserved
3	GF1	General-purpose user flag.
2	GF0	General-purpose user flag.
1	PD	1: Go into POWER DOWN mode. In this mode, all clocks and program execution are stopped.
0	IDL	1: Go into IDLE mode. In this mode, the CPU clock stops, so program execution stops too. However, the clock to the serial port, ADC, timer and interrupt blocks does not stop, so these blocks continue operating.

Timer Control

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON

Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 overflow flag: This bit is set when Timer 1 overflows. It is cleared automatically when the program executes the Timer-1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 run control: This bit turns the Timer 1 on or off.
5	TF0	Timer 0 overflow flag: This bit is set when Timer 0 overflows. It is cleared automatically when the program executes the Timer-0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 run control: This bit turns Timer 0 on or off.
3	IE1	Interrupt 1 Edge Detect: Set by hardware when an edge / level is detected on $\overline{\text{INT1}}$. This bit is cleared by the hardware when the ISR is executed only if the interrupt is edge-triggered. Otherwise, it follows the pin.
2	IT1	Interrupt 1 type control: Specify falling-edge or low-level trigger for $\overline{\text{INT1}}$.
1	IE0	Interrupt 0 Edge Detect: Set by hardware when an edge / level is detected on $\overline{\text{INT0}}$. This bit is cleared by the hardware when the ISR is executed only if the interrupt is edge-triggered. Otherwise, it follows the pin.
0	IT0	Interrupt 0 type control: Specify falling-edge or low-level trigger for $\overline{\text{INT0}}$.

Timer Mode Control

Bit:	7	6	5	4	3	2	1	0
	GATE	$\text{C}/\overline{\text{T}}$	M1	M0	GATE	$\text{C}/\overline{\text{T}}$	M1	M0

Mnemonic: TMOD

Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer 1 is enabled only while the $\overline{\text{INT1}}$ pin is high and the TR1 control bit is set. When clear, the $\overline{\text{INT1}}$ pin has no effect, and Timer 1 is enabled whenever TR1 is set.
6	$\text{C}/\overline{\text{T}}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the Tx pin.
5	M1	Timer 1 mode select bit 1. See table below.
4	M0	Timer 1 mode select bit 0. See table below.

Continued

BIT	NAME	FUNCTION
3	GATE	Gating control: When this bit is set, Timer 0 is enabled only while the $\overline{\text{INT0}}$ pin is high and the TR0 control bit is set. When clear, the $\overline{\text{INT0}}$ pin has no effect, and Timer 0 is enabled whenever TR0 is set.
2	C/ $\overline{\text{T}}$	Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the Tx pin.
1	M1	Timer 0 mode select bit 1. See table below.
0	M0	Timer 0 mode select bit 0. See table below.

M1, M0: Mode Select bits:

M1	M0	Mode
0	0	Mode 0: 8-bit timer/counter TLx serves as 5-bit pre-scale.
0	1	Mode 1: 16-bit timer/counter, no pre-scale.
1	0	Mode 2: 8-bit timer/counter with auto-reload from THx
1	1	Mode 3:

(Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer-0 control bits. TH0 is an 8-bit timer only controlled by Timer-1 control bits.

(Timer 1) Timer/Counter 1 is stopped.

Timer 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0

Address: 8Ah

TL0.7–0: Timer 0 LSB

Timer 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1

Address: 8Bh

TL1.7–0: Timer 1 LSB

Timer 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0

Address: 8Ch

TH0.7–0: Timer 0 MSB

Timer 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1

Address: 8Dh

TH1.7–0: Timer 1 MSB

Clock Control

Bit:	7	6	5	4	3	2	1	0
	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0

Mnemonic: CKCON

Address: 8Eh

BIT	NAME	FUNCTION
7	WD1	Watchdog Timer mode select bit 1. See table below.
6	WD0	Watchdog Timer mode select bit 0. See table below.
5	T2M	Timer 2 clock select: 1: divide-by-4 clock 0: divide-by-12 clock
4	T1M	Timer 1 clock select: 1: divide-by-4 clock 0: divide-by-12 clock
3	T0M	Timer 0 clock select: 1: divide-by-4 clock 0: divide-by-12 clock
2	MD2	Stretch MOVX select bit 2: MD2, MD1, and MD0 select the stretch value for the MOVX instruction. The \overline{RD} or \overline{WR} strobe is stretched by the selected interval, which enables the W79E201 to access faster or slower external memory devices or peripherals without the need for external circuits. By default, the stretch value is one. See table below. (Note: When accessing on-chip SRAM, these bits have no effect, and the MOVX instruction always takes two machine cycles.)
1	MD1	Stretch MOVX select bit 1. See MD2.
0	MD0	Stretch MOVX select bit 0. See MD2.

WD1, WD0: Mode Select bits:

These bits determine the time-out periods for the Watchdog Timer. The reset time-out period is 512 clocks more than the interrupt time-out period.

WD1	WD0	INTERRUPT TIME-OUT	RESET TIME-OUT
0	0	2^{17}	$2^{17} + 512$
0	1	2^{20}	$2^{20} + 512$
1	0	2^{23}	$2^{23} + 512$
1	1	2^{26}	$2^{26} + 512$

MD2, MD1, MD0: Stretch MOVX select bits:

MD2	MD1	MD0	STRETCH VALUE	MOVX DURATION
0	0	0	0	2 machine cycles
0	0	1	1	3 machine cycles (Default)
0	1	0	2	4 machine cycles
0	1	1	3	5 machine cycles
1	0	0	4	6 machine cycles
1	0	1	5	7 machine cycles
1	1	0	6	8 machine cycles
1	1	1	7	9 machine cycles

Port 0 pull-up resistor

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	P0UP

Mnemonic: P0R

Address: 8Fh

BIT	NAME	FUNCTION
7~1	-	Reserved
0	P0UP	Port 0 Pull-Up Resistor 0: No pull-up resistor 1: Pull-up resistor (~10 KΩ)

Port 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1

Address: 90h

P1.7–0: General-purpose digital input port or analog input port AD0~AD7. For digital input, port-read instructions read the port pins, while read-modify-write instructions read the port latch. Additional functions are described below. This port is also used for 8 channels of analog inputs from ADC0 to ADC7.

BIT	NAME	FUNCTION
1	P1.1	T2 : External Input for Timer/Counter 2
0	P1.0	T2EX : Timer/Counter 2 Capture/Reload Trigger

Serial Port Control

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON

Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial Port mode select bit 0 or Framing Error Flag: This bit is controlled by the SMOD0 bit in the PCON register. (SM0) See table below. (FE) This bit indicates an invalid stop bit. It must be manually cleared by software.
6	SM1	Serial Port mode select bit 1. See table below.
5	SM2	Serial Port Clock or Multi-Processor Communication. (Mode 0) This bit controls the serial port clock. If set to zero, the serial port runs at a divide-by-12 clock of the oscillator. This is compatible with the standard 8051/52. (Mode 1) If SM2 is set to one, RI is not activated if a valid stop bit is not received. (Modes 2 / 3) This bit enables multi-processor communication. If SM2 is set to one, RI is not activated if RB8, the ninth data bit, is zero.
4	REN	Receive enable: 1: Enable serial reception 0: Disable serial reception
3	TB8	(Modes 2 / 3) This is the 9th bit to transmit.
2	RB8	(Mode 0) No function. (Mode 1) If SM2 = 0, RB8 is the stop bit that was received. (Modes 2 / 3) This is the 9th bit that was received.
1	TI	Transmit interrupt flag: This flag is set by the hardware at the end of the 8th bit in mode 0 or at the beginning of the stop bit in the other modes during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by the hardware at the end of the 8th bit in mode 0 or halfway through the stop bits in the other modes during serial reception. However, SM2 can restrict this behavior. This bit can only be cleared by software.

SM0, SM1: Mode Select bits:

SM0	SM1	MODE	DESCRIPTION	LENGTH	BAUD RATE
0	0	0	Synchronous	8	Tclk divided by 4 or 12
0	1	1	Asynchronous	10	Variable
1	0	2	Asynchronous	11	Tclk divided by 32 or 64
1	1	3	Asynchronous	11	Variable

Serial Data Buffer

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF

Address: 99h

SBUF.7–0: Serial data in the serial port is read from or written to this location. It actually consists of two separate 8-bit registers, the receive register and the transmit buffer. Read accesses get data from the receive register, and write accesses write to the transmit buffer.

ISP Control Register

Bit:	7	6	5	4	3	2	1	0
	SWRST/ REBOOT	-	LDAP	-	-	-	FBOOTSL	FPROGEN

Mnemonic: CHPCON

Address: 9Fh

BIT	NAME	FUNCTION
7	SWRST/ REBOOT	Set this bit to reset the device. This has the same effect as asserting the RST pin. The microcontroller returns to its initial state, and this bit is cleared automatically. Reading this bit indicates whether or not the device is in ISP hardware reboot mode.
6	-	Reserved
5	LDAP	This bit is read-only. 1: Device is running the program in LD Flash EPROM 0: Device is running the program in AP Flash EPROM
4-2	-	Reserved
1	FBOOTSL	Program Location Selection. This bit should be set before entering ISP mode. 1: Run the program in LD Flash EPROM. 0: Run the program in AP Flash EPROM.
0	FPROGEN	FLASH EPROM Programming Enable. 1: Enable in-system programming mode. The erase, program and read operations are executed according to various SFR settings. In this mode, the device runs in IDLE state, so PCON.1 has no effect. 0: Disable in-system programming mode. The device returns to normal operations, and PCON.1 is functional again.

Port 2

Bit:	7	6	5	4	3	2	1	0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

Mnemonic: P2

Address: A0h

P2.7-0: Port 2 is a bi-directional I/O port with internal pull-up resistors. This port also provides the upper address bits for accesses to external memory.

Port 4

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	P4.0

Mnemonic: P4

Address: A5h

P4.0:

When security bit B3 is 0, P4.0 is the reboot pin.

When security bit B3 is 1, P4.0 is an I/O pin.

Interrupt Enable

Bit:	7	6	5	4	3	2	1	0
	EA	EADC	ET2	ES	ET1	EX1	ET0	EX0

Mnemonic: IE

Address: A8h

BIT	NAME	FUNCTION
7	EA	Global enable. Enable/disable all interrupts.
6	EADC	Enable ADC interrupt.
5	ET2	Enable Timer 2 interrupt.
4	ES	Enable Serial Port interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt 1.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt 0.

Slave Address

Bit:	7	6	5	4	3	2	1	0
	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0

Mnemonic: SADDR

Address: A9h

The SADDR should be programmed to the given or broadcast address for the serial ports to which a slave processor is designated.

ISP Address Low Byte

Bit:	7	6	5	4	3	2	1	0
	SFRAL.7	SFRAL.6	SFRAL.5	SFRAL.4	SFRAL.3	SFRAL.2	SFRAL.1	SFRAL.0

Mnemonic: SFRAL

Address: ACh

Low-byte destination address for In-System Programming operations. SFRAH and SFRAL are specific ROM locations for erase, program or read operations.

ISP Address High Byte

Bit:	7	6	5	4	3	2	1	0
	SFRAH.7	SFRAH.6	SFRAH.5	SFRAH.4	SFRAH.3	SFRAH.2	SFRAH.1	SFRAH.0

Mnemonic: SFRAH

Address: ADh

High-byte destination address for In-System Programming operations. SFRAH and SFRAL are specific ROM locations for erase, program or read operations.

ISP Data Buffer

Bit:	7	6	5	4	3	2	1	0
	SFRFD.7	SFRFD.6	SFRFD.5	SFRFD.4	SFRFD.3	SFRFD.2	SFRFD.1	SFRFD.0

Mnemonic: SFRFD

Address: AEh

In ISP mode, bytes read from ROM and bytes written to ROM go through SFRFD

ISP Operation Modes

Bit:	7	6	5	4	3	2	1	0
	-	WFWIN	OEN	CEN	CTRL3	CTRL2	CTRL1	CTRL0

Mnemonic: SFRCN

Address: AFh

BIT	NAME	FUNCTION
7	-	Reserved
6	WFWIN	On-chip Flash EPROM bank select for in-system programming. This bit should be set by the loader program in ISP mode. 0: 16-KB Flash EPROM is the destination for re-programming. 1: 4-KB Flash EPROM is the destination for re-programming.
5	OEN	Flash EPROM output is enabled.
4	CEN	Flash EPROM chip is enabled.
3~0	CTRL[3:0]	The flash control signals. See table below.

WFWIN, OEN, CEN, CTRL[3:0]: ISP Instruction select bits:

ISP MODE	WFWIN	OEN	CEN	CTRL<3:0>	SFRAH, SFRAL	SFRFD
Erase 4-KB LD FLASH PROM	1	1	0	0010	X	X
Erase 16-K AP FLASH EPROM	0	1	0	0010	X	X
Program 4-KB LD FLASH EPROM	1	1	0	0001	Address in	Data in
Program 16-KB AP FLASH EPROM	0	1	0	0001	Address in	Data in
Read 4-KB LD FLASH EPROM	1	0	0	0000	Address in	Data out
Read 16-KB AP FLASH EPROM	0	0	0	0000	Address in	Data out

Port 3

Bit:	7	6	5	4	3	2	1	0
	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0

Mnemonic: P3

Address: B0h

P3.7-0: General-purpose I/O port. Each pin also has an alternative input or output function, which is described below.

BIT	NAME	FUNCTION
7	P3.7	$\overline{\text{RD}}$ strobe for reading from external RAM
6	P3.6	$\overline{\text{WR}}$ strobe for writing to external RAM
5	P3.5	Timer 1 external count input
4	P3.4	Timer 0 external count input
3	P3.3	External interrupt 1 $\overline{\text{INT1}}$
2	P3.2	External interrupt 0 $\overline{\text{INT0}}$
1	P3.1	TxD: Serial port 0 output
0	P3.0	RxD: Serial port 0 input

Interrupt Priority

Bit:	7	6	5	4	3	2	1	0
	-	PADC	PT2	PS	PT1	PX1	PT0	PX0

Mnemonic: IP

Address: B8h

BIT	NAME	FUNCTION
7	-	Reserved. This bit reads high.
6	PADC	1: Set the priority of the ADC interrupt to the highest level.
5	PT2	1: Set the priority of the Timer 2 interrupt to the highest level.
4	PS	1: Set the priority of the Serial Port interrupt to the highest level.
3	PT1	1: Set the priority of the Timer 1 interrupt to the highest level.
2	PX1	1: Set the priority of external interrupt 1 to the highest level.
1	PT0	1: Set the priority of the Timer 0 interrupt to the highest level.
0	PX0	1: Set the priority of external interrupt 0 to the highest level.

Slave Address Mask Enable

Bit:	7	6	5	4	3	2	1	0
	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0

Mnemonic: SADEN

Address: B9h

BIT	NAME	FUNCTION
7~0	SADEN	This register enables the Automatic Address Recognition feature for the serial port. When a bit in SADEN is set to 1, the same bit in SADDR is compared to incoming serial data. When a bit in SADEN is set to 0, the same bit becomes a "don't care" condition in the comparison. Disable Automatic Address Recognition by setting all the bits in SADEN to 0.

PWM 5 Register

Bit:	7	6	5	4	3	2	1	0
	PWM5.7	PWM5.6	PWM5.5	PWM5.4	PWM5.3	PWM5.2	PWM5.1	PWM5.0

Mnemonic: PWM 5

Address: C3h

Power Management Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	ALE-OFF	-	-

Mnemonic: PMR

Address: C4h

BIT	NAME	FUNCTION
7~3	-	Reserved.
2	ALE-OFF	0: ALE expression is enabled during on-board program and data accesses. 1: ALE expression is disabled. Keep the logic in the high state. External memory accesses automatically enable ALE, regardless of ALE-OFF.
1~0	-	Reserved.

Status Register

Bit:	7	6	5	4	3	2	1	0
	-	HIP	LIP	-	-	-	SPTA0	SPRA0

Mnemonic: STATUS

Address: C5h

BIT	NAME	FUNCTION
7	-	Reserved.
6	HIP	High-Priority Interrupt Status. When set, it indicates that the software is servicing a high-priority interrupt. This bit is cleared when the program executes the corresponding RETI instruction.
5	LIP	Low-Priority Interrupt Status. When set, it indicates that the software is servicing a low-priority interrupt. This bit is cleared when the program executes the corresponding RETI instruction.
4-2	-	Reserved.
1	SPTA0	Serial-Port Transmit Activity. This bit is set when the serial port is transmitting data. It is cleared when the TI bit is set by the hardware.
0	SPRA0	Serial-Port Receive Activity. This bit is set when the serial port is receiving data. It is cleared when the RI bit is set by the hardware.

Timed Access

Bit:	7	6	5	4	3	2	1	0
	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0

Mnemonic: TA

Address: C7h

TA: This register controls the access to protected bits. To access protected bits, the program must write AAH, followed immediately by 55H, to TA. This opens a window for three machine cycles, during which the program can write to protected bits.

Timer 2 Control

Bit:	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2

Mnemonic: T2CON

Address: C8h

BIT	NAME	FUNCTION
7	TF2	Timer 2 Overflow flag: This bit is set when Timer 2 overflows. It is also set when the count is equal to the capture register in down-count mode. It can be set by the hardware only if RCLK and TCLK are both 0, and it can be set or cleared by software.
6	EXF2	Timer 2 External flag: A negative transition on the T2EX pin (P1.1) or a timer 2 underflow / overflow sets this flag according to the CP/RL2, EXEN2 and DCEN bits. This bit can also be set by the software. If set by a negative transition, this flag must be cleared by software. If set by a negative transition or by software, a Timer 2 interrupt is generated, if enabled.
5	RCLK	Receive Clock flag: This bit determines the serial-port time base when receiving data in Serial Port modes 1 or 3. 0: The Timer 1 overflow is used for baud-rate generation 1: The Timer 2 overflow is used for baud-rate generation, forcing Timer 2 into baud-rate generator mode.
4	TCLK	Transmit Clock flag: This bit determines the serial-port time base when transmitting data in Serial Port modes 1 or 3. 0: The Timer 1 overflow is used for baud-rate generation 1: The Timer 2 overflow is used for baud-rate generation, forcing Timer 2 into baud-rate generator mode.
3	EXEN2	Timer 2 External Enable: This bit enables the capture / reload function on the T2EX pin, as long as Timer 2 is not generating baud clocks for the serial port. 0: Ignore T2EX. 1: Negative transitions on T2EX result in capture or reload.
2	TR2	Timer 2 Run Control: This bit enables / disables Timer 2. When disabled, Timer 2 preserves the current values in TH2 and TL2.
1	$\overline{\text{C/T2}}$	Counter / Timer select: 0: Timer 2 operates as a timer at a speed depending on T2M bit (CKCON.5) 1: Timer 2 counts negative edges on the T2EX pin. Regardless of this bit, Timer 2 may be forced into baud-rate generator mode.
0	$\overline{\text{CP/RL2}}$	Capture / Reload select, when Timer 2 overflows or when a falling edge is detected on T2EX (and EXEN2 = 1). 0: Auto-reload Timer 2 1: Capture in Timer 2 If RCLK or TCLK is set, this bit does not function, and Timer 2 runs in auto-reload mode following each overflow.

Timer 2 Mode Control

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	T2CR	-	-	DCEN

Mnemonic: T2MOD

Address: C9h

BIT	NAME	FUNCTION
7~4	-	Reserved.
3	T2CR	Timer 2 Capture Reset. In Timer-2 Capture Mode, 1: Automatically reset Timer 2 once the Timer 2 capture registers have captured the values in Timer 2.
2~1	-	Reserved.
0	DCEN	Down Count Enable: This bit controls the direction that Timer 2 counts in 16-bit auto-reload mode.

Timer 2 Capture LSB

Bit:	7	6	5	4	3	2	1	0
	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0

Mnemonic: RCAP2L

Address: CAh

RCAP2L:

(Capture mode) This register captures the LSB of Timer 2 (TL2).

(Auto-reload mode) This register is the LSB of the 16-bit reload value.

Timer 2 Capture MSB

Bit:	7	6	5	4	3	2	1	0
	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0

Mnemonic: RCAP2H

Address: CBh

RCAP2H:

(Capture mode) This register captures the MSB of Timer 2 (TH2).

(Auto-reload mode) This register is the MSB of the 16-bit reload value.

Timer 2 LSB

Bit:	7	6	5	4	3	2	1	0
	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0

Mnemonic: TL2

Address: CCh

TL2: Timer 2 LSB

Timer 2 MSB

Bit:	7	6	5	4	3	2	1	0
	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0

Mnemonic: TH2

Address: CDh

TH2: Timer 2 MSB

PWM 4~5 Control Register 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	PWM5OE	PWM4OE	ENPWM5	ENPWM4

Mnemonic: PWMCON2

Address: CEh

BIT	NAME	FUNCTION
7~4	-	Reserved.
3	PWM5OE	Output enable for PWM5 0: Disable PWM5 Output. 1: Enable PWM5 Output.
2	PWM4OE	Output enable for PWM4 0: Disable PWM4 Output. 1: Enable PWM4 Output.
1	ENPWM5	Enable PWM5 0: Disable PWM5. 1: Enable PWM5.
0	ENPWM4	Enable PWM4 0: Disable PWM4. 1: Enable PWM4.

PWM 4 Register

Bit:	7	6	5	4	3	2	1	0
	PWM4.7	PWM4.6	PWM4.5	PWM4.4	PWM4.3	PWM4.2	PWM4.1	PWM4.0

Mnemonic: PWM 4

Address: CFh

Program Status Word

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

Mnemonic: PSW

Address: D0h

BIT	NAME	FUNCTION
7	CY	Carry flag: Set when an arithmetic operation results in a carry being generated from the ALU. It is also used as the accumulator for bit operations.
6	AC	Auxiliary carry: Set when the previous operation resulted in a carry from the high-order nibble.
5	F0	User flag 0: A general-purpose flag that can be set or cleared by the user.
4	RS1	Register Bank select bits. See table below.
3	RS0	Register Bank select bits. See table below.
2	OV	Overflow flag: Set when a carry was generated from the seventh bit but not from the eighth bit, or vice versa, as a result of the previous operation.
1	F1	User flag 1: A general-purpose flag that can be set or cleared by the user.
0	P	Parity flag: Set and cleared by the hardware to indicate an odd or even number of 1's in the accumulator.

RS1, RS0: Register Bank select bits:

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

Watchdog Control

Bit:	7	6	5	4	3	2	1	0
	-	POR	-	-	WDIF	WTRF	EWT	RWT

Mnemonic: WDCON

Address: D8h

BIT	NAME	FUNCTION
7	-	Reserved.
6	POR	Power-on reset flag. The hardware sets this flag during power-up, and it can only be cleared by software. This flag can also be written by software.
5-4	-	Reserved.
3	WDIF	Watchdog Timer Interrupt Flag. If the watchdog interrupt is enabled, the hardware sets this bit to indicate that the watchdog interrupt has occurred. If the interrupt is not enabled, this bit indicates that the time-out period has elapsed. This bit must be cleared by software.
2	WTRF	Watchdog Timer Reset Flag. If EWT is 0, the Watchdog Timer has no affect on this bit. Otherwise, the hardware sets this bit when the Watchdog Timer causes a reset. It can be cleared by software or a power-fail reset. It can be also read by software, which helps determine the cause of a reset.
1	EWT	Enable Watchdog-Timer Reset. Set this bit to enable the Watchdog Timer Reset function.
0	RWT	Reset Watchdog Timer. Set this bit to reset the Watchdog Timer before a time-out occurs. This bit is automatically cleared by the hardware.

The WDCON register is affected differently by different kinds of resets. After an external reset, the WDCON register is set to 0x0x0x0b. After a Watchdog Timer reset, WTRF is set to 1, and the other bits are unaffected. On a power-on/-down reset, WTRF and EWT are set to 0, and POR is set to 1.

All the bits in this SFR have unrestricted read access. POR, EWT, WDIF and RWT are protected bits, so programs must follow the Timed Access procedure to write them. (See the TA Register description for more information.) This is illustrated in the following example.

```

TA      EG    C7H
WDCON   REG   D8H
CKCON   REG   8EH
        MOV   TA, #AAH
        MOV   TA, #55H
        SETB  WDCON.0           ; Reset Watchdog Timer
        ORL   CKCON, #11000000B ; Select 26 bits Watchdog Timer
        MOV   TA, #AAH
        MOV   TA, #55H
        ORL   WDCON, #00000010B ; Enable watchdog
  
```

The other bits in WDCON have unrestricted write access.

PWM Prescale Register

Bit:	7	6	5	4	3	2	1	0
	PWMP.7	PWMP.6	PWMP.5	PWMP.4	PWMP.3	PWMP.2	PWMP.1	PWMP.0

Mnemonic: PWMP

Address: D9h

PWM 0 Register

Bit:	7	6	5	4	3	2	1	0
	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0

Mnemonic: PWM0

Address: DAh

PWM 1 Register

Bit:	7	6	5	4	3	2	1	0
	PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0

Mnemonic: PWM1

Address: DBh

PWM 0~3 Control Register 1

Bit:	7	6	5	4	3	2	1	0
	PWM3OE	PWM2OE	ENPWM3	ENPWM2	PWM1OE	PWM0OE	ENPWM1	ENPWM0

Mnemonic: PWMCON1

Address: DCh