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8-bit Microcontroller

Table of Contents-

1.	GENERAL DESCRIPTION	5
2.	FEATURES	6
3.	PARTS INFORMATION LIST	7
3.1	Lead Free (RoHS) Parts information list.....	7
4.	PIN CONFIGURATION	8
5.	PIN DESCRIPTION.....	9
5.1	Port 4	12
6.	MEMORY ORGANIZATION.....	13
6.1	Program Memory (on-chip Flash)	13
6.2	Data Memory	13
6.3	Auxiliary SRAM	14
6.4	2-KB NVM Data Flash Memory	14
6.4.1	Operation.....	16
7.	SPECIAL FUNCTION REGISTERS	19
8.	INSTRUCTION SET.....	73
8.1	Instruction Timing.....	81
8.1.1	External Data Memory Access Timing.....	83
9.	POWER MANAGEMENT.....	86
9.1	Idle Mode	86
9.2	Power Down Mode	86
10.	RESET CONDITIONS.....	88
10.1	Sources of reset.....	88
10.1.1	External Reset.....	88
10.1.2	Power-On Reset (POR).....	88
10.1.3	Watchdog Timer Reset.....	88
10.2	Reset State	89
11.	INTERRUPTS	90
11.1	Interrupt Sources	90
11.2	Priority Level Structure	91
11.2.1	Response Time	94
12.	PROGRAMMABLE TIMERS/COUNTERS	95
12.1	Timer/Counters 0 & 1.....	95
12.1.1	Time-Base Selection	95
12.1.2	Mode 0	95
12.1.3	Mode 1	96
12.1.4	Mode 2	96
12.1.5	Mode 3	97
12.2	Timer/Counter 2.....	97
12.2.1	Capture Mode.....	98

Preliminary W79E217A Data Sheet



12.2.2	Auto-reload Mode, Counting up.....	98
12.2.3	Auto-reload Mode, Counting Up/Down	99
12.2.4	Baud Rate Generator Mode	100
13.	WATCHDOG TIMER.....	101
14.	PULSE-WIDTH-MODULATED (PWM) OUTPUTS	104
14.1	PWM Features	104
14.2	PWM Control Registers	105
14.3	PWM Pin Structures	107
14.4	Complementary PWM with Dead-time and Override functions	110
14.5	Dead-Time Insertion	111
14.6	PWM Output Override	112
14.7	Edge Aligned PWM (up-counter).....	115
14.8	Center Aligned PWM (up/down counter)	117
14.9	Single Shot (Up-Counter)	120
14.10	Smart Fault Detector	122
14.11	PWM Power-down/Wakeup Procedures	125
15.	MOTION FEEDBACK MODULE	127
15.1	Input Capture Module (IC)	127
15.1.1	Compare Mode.....	134
15.1.2	Reload Mode	135
15.2	Quadrature Encoder Interface (QEI)	135
15.2.1	Free-counting mode	137
15.2.2	Compare-counting mode	137
15.2.3	X2/X4 Counting modes.....	137
15.2.4	Direction of Count.....	137
15.2.5	Up-Counting	139
15.2.6	Down-Counting.....	139
16.	SERIAL PORT	140
16.1	Mode 0	140
16.2	Mode 1	141
16.3	Mode 2	142
16.4	Mode 3	142
16.5	Framing Error Detection	143
16.6	Multiprocessor Communications.....	144
17.	I2C SERIAL PORTS	145
17.1	SIO Port	145
17.2	The I2C Control Registers	145
17.2.1	Slave Address Registers, I2ADDR	146
17.2.2	Data Register, I2DAT	146
17.2.3	Control Register, I2CON.....	146
17.2.4	Status Register, I2STATUS	147
17.2.5	I2C Clock Baud Rate Control, I2CLK.....	147
17.2.6	I2C Time-out Counter, I2Timer	147
17.2.7	I2C Maskable Slave Address	147
17.3	Modes of Operation	148

Preliminary W79E217A Data Sheet



17.3.1	Master Transmitter Mode	148
17.3.2	Master Receiver Mode	148
17.3.3	Slave Receiver Mode	148
17.3.4	Slave Transmitter Mode	149
17.4	Data Transfer Flow in Five Operating Modes	149
17.4.1	Master/Transmitter Mode	150
17.4.2	Master/Receiver Mode	151
17.4.3	Slave/Transmitter Mode	152
17.4.4	Slave/Receiver Mode	153
17.4.5	GC Mode	154
18.	SERIAL PERIPHERAL INTERFACE (SPI)	155
18.1	General descriptions	155
18.2	Block descriptions	155
18.3	Functional descriptions	157
18.3.1	Master mode	157
18.3.2	Slave Mode	160
18.3.3	Slave select	164
18.3.4	/SS output	164
18.3.5	SPI I/O pins mode	165
18.3.6	Programmable serial clock's phase and polarity	165
18.3.7	Receive double buffered data register	166
18.3.8	LSB first enable	166
18.3.9	Write Collision detection	167
18.3.10	Transfer complete interrupt	167
18.3.11	Mode Fault	167
19.	ANALOG-TO-DIGITAL CONVERTER	170
19.1	Operation of ADC	170
19.2	ADC Resolution and Analog Supply	171
20.	LCD DISPLAY	172
20.1	LCD Features	172
20.2	LCD Frequency	173
20.3	LCD Power Connection	178
20.4	LCD Option Bits	180
20.5	LCD Display	180
21.	TIMED ACCESS PROTECTION	183
22.	PORT 4 STRUCTURE	185
23.	IN-SYSTEM PROGRAMMING	188
23.1	The Loader Program Locates at LDFlash Memory	188
23.2	The Loader Program Locates at APFlash Memory	188
24.	OPTION BITS	189
24.1	Config0	189
24.2	Config1	190
25.	ELECTRICAL CHARACTERISTICS	191
25.1	Absolute Maximum Ratings	191

Preliminary W79E217A Data Sheet



25.2	DC Characteristics	191
25.3	AC Characteristics	194
25.3.1	External Clock Characteristics	194
25.3.2	AC Specification	194
25.3.3	MOVX Characteristics Using Stretch Memory Cycle	195
25.4	The ADC Converter DC ELECTRICAL CHARACTERISTICS	197
25.5	I2C Bus Timing Characteristics	197
25.6	Program Memory Read Cycle	198
25.7	Data Memory Read Cycle	199
25.8	Data Memory Write Cycle	199
26.	TYPICAL APPLICATION CIRCUITS	200
26.1	Crystal connections	200
26.2	Expanded External Data Memory and Oscillator	200
27.	PACKAGE DIMENSION	201
27.1	100L QFP (14x20x2.75mm footprint 3.2mm)	201
28.	APPLICATION NOTE	202
29.	REVISION HISTORY	208



1. GENERAL DESCRIPTION

The W79E217 is a fast, 8051/52-compatible microcontroller with a redesigned processor core that eliminates wasted clock and memory cycles. Typically, the W79E217 executes instructions 1.5 to 3 times faster than that of the traditional 8051/52, depending on the type of instruction, and the overall performance is about 2.5 times better at the same crystal speed. As a result, with the fully-static CMOS design, the W79E217 can accomplish the same throughput with a lower clock speed, reducing power consumption.

The W79E217 provides **256** bytes of on-chip RAM; **2**-KB of NVM memory Flash EPROM; **2**-KB of auxiliary RAM; **seven** 8-bit, bi-directional and bit-addressable I/O ports; an additional **4**-bit port P4; **three** 16-bit timer/counters; Motion Feedback Module support; **2** UART serial ports; **1** channels of I2C with master/slave capability; **1** channels of Serial Peripheral Interface (SPI), **8** channels of **12** bit PWM with configurable dead time and **8** channels of 10-bit ADC. These peripherals are all supported by **20** interrupt sources with **4** levels of priority.

The W79E217 also contains a **64**-KB Flash EPROM whose contents may be updated in-system by a loader program stored in an auxiliary, **4**-KB Flash EPROM. Once the contents are confirmed, it can be protected for security.



2. FEATURES

- Fully-static-design 8-bit 4T-8051 CMOS microcontroller up to 33MHz.
- **64**-KB of in-system-programmable Flash EPROM (AP Flash EPROM).
- **4**-KB of Auxiliary Flash EPROM for the loader program (LD Flash EPROM). User can optionally reboot from LD Flash EPROM by pull low at either P4.3 or P3.6 and P3.7, at external reset.
- **2**-KB auxiliary RAM, software-selectable, accessed by MOVX instruction.
- **2**-KB of NVM Data Flash EPROM for customer data storage used.
- 256 bytes of scratch-pad RAM.
- Seven 8-bit bi-directional ports; Port 0 has internal pull-up resistors enabled by software.
- One 4-bit multipurpose I/O port4 with Chips select (CS) and boot function.
- Three 16-bit timers.
- One 16-bit Timer 3 for Motion Feed-Back Module.
- Motion Feedback Module - QEI decoder and 3 Inputs Capture.
- Eight channels of 12-bit PWM:-
 - Complementary paired output with programmable dead-time insertion.
 - Three modes: Edge aligned, center aligned and single shot.
 - Output override control for BLDC motor application.
- 10-bit ADC with 8-channel inputs.
- Two enhanced full-duplex UART with framing-error detection and automatic address recognition.
- One channel of I2C with master/slave capability.
- One channel of SPI with master/slave capability.
- LCD driver output:-
 - 32segment X 4common.
 - 1/3 duty (1/3 bias), 1/4 duty (1/3 bias) driving mode can be selected.
 - LCD driver output pin can be used as DC output.
- Software programmable access cycle to external RAM/peripherals.
- 20 interrupt sources with four levels of priority.
- Software reset function.
- Optional H/L state of ALE/PSEN during power down mode.
- Built-in power management.
- Code protection.
- Package:
 - Lead Free (RoHS) PQFP 100: W79E217AFG

Preliminary W79E217A Data Sheet



3. PARTS INFORMATION LIST

3.1 Lead Free (RoHS) Parts information list

PART NO.	EPROM FLASH SIZE	RAM	OPERATING FREQUENCY	OPERATING VOLTAGE	NVM FLASH EPROM	PACKAGE	REMARK
W79E217AFG	64KB	256B + 2KB	up to 33MHz up to 20MHz	4.5V ~ 5.5V 2.7V ^[1] ~ 5.5V	2KB	PQFP-100 Pin	Internal memory
			up to 24MHz	4.5V ~ 5.5V			External memory

Note: 1. Minimum of 3.0V operating voltage for NVM program and erase operations.

W79E217A
PQFP-100pin



5. PIN DESCRIPTION

SYMBOL	TYPE	INITIAL STATE	DESCRIPTIONS
$\overline{EA}$	I	-	EXTERNAL ACCESS ENABLE: This pin forces the processor to execute from external ROM. The ROM address and data are not presented on the bus if the $\overline{EA}$ pin is high. Note: This pin has no internal pull-up or pull-down. The pin needs externally pull-up to execute from internal APROM. For executing from external APROM, the pin needs externally pull-down. The pin state is internally latched during all reset. User needs to take note that changes to $\overline{EA}$ pin state after reset will not be effective.
$\overline{PSEN}$	O H	High	PROGRAM STORE ENABLE: $\overline{PSEN}$ enables the external ROM data in the Port 0 address/data bus. When internal ROM access is performed, $\overline{PSEN}$ strobe signal will not be output from this pin.
ALE	O H	High	ADDRESS LATCH ENABLE: ALE enables the address latch that separates the address from the data on Port 0.
RST	I L	-	RESET: Set this pin high for two machine cycles while the oscillator is running to reset the device.
XTAL1	I	-	CRYSTAL 1: Crystal oscillator input or external clock input.
XTAL2	O	-	CRYSTAL 2: Crystal oscillator output.
V_{SS}	I	-	GROUND: Ground potential.
V_{DD}	I	-	POWER SUPPLY: Supply voltage for operation.
VLCD1, VLCD2	I	-	LCD voltage input. Positive (+) supply voltage terminal for LCD biasing.
AVDD	I	-	Analog power supply.
AVSS	I	-	Analog ground potential.
VDDPWM	I	-	PWM power supply.
VSSPWM	I	-	PWM ground potential.
P0.0–P0.7	I/O D S H	High-Z	PORT 0: Port 0 is an open-drain bi-directional I/O port. This port also provides a multiplexed low byte address/data bus during accesses to external memory. There is an embedded weakly pull-up resistor on each port 0 pin which can be enabled or disabled by setting or clearing of PUP0, bit0 in A2h. The ports have alternate functions which are described below: P0.0, MISO P0.1, MOSI P0.2, SPCLK P0.3, $\overline{SS}$ P0.4, INT2 P0.5, INT3 P0.6, INT4 P0.7, INT5

Preliminary W79E217A Data Sheet



PIN DESCRIPTION, continued

SYMBOL	TYPE	INITIAL STATE	DESCRIPTIONS
P1.0–P1.7	I/O S H	High	PORT 1: 8-bit, bi-directional I/O port with internal pull-ups. The ports have alternate functions which are described below: P1.0, ADC0, T2 P1.1, ADC1, BRAKE P1.2, ADC2, RXD1 P1.3, ADC3, TXD1 P1.4, ADC4 P1.5, ADC5 P1.6, ADC6 P1.7, ADC7
P2.0-P2.5	I/O S H	Tri-state	PORT 2: 8-bit, bi-directional I/O port. This port also provides the upper address bits for accesses to external memory. P2.6 to P2.7 can be software configured as I2C serial ports. P2.0 to P2.5 also provides PWM0 to PWM5 outputs. P2.0, A8, PWM0 P2.1, A9, PWM1 P2.2, A10, PWM2 P2.3, A11, PWM3 P2.4, A12, PWM4 P2.5, A13, PWM5 P2.6, A14, SCL P2.7, A15, SDA Note: a. P2.6 and P2.7 are permanent open drain pins. When access to external memory beyond 16K region, user requires to add external pull-up registers (up to 2Kohm) on these pins. This will result in slight increase in current consumption. b. Port 2 power source is from VDDPWM.
P2.6-P2.7	I/O S D	High-Z	
P3.0-P3.7	I/O S H	High	PORT 3: 8-bit, bi-directional I/O port with internal pull-ups. The ports have alternate functions which are described below: P3.0, RXD P3.1, TXD P3.2, /INT0 P3.3, /INT1 P3.4, T0, IC0, QEA P3.5, T1, IC1, QEB P3.6, /WR P3.7, /RD

Preliminary W79E217A Data Sheet



PIN DESCRIPTION, continued

SYMBOL	TYPE	INITIAL STATE	DESCRIPTIONS		
P4.0-P4.3	I/O S H	High	PORT 4: 4-bit multipurpose programmable I/O port with alternate functions. The Port 4 has four different operation modes. P4.0, STADC P4.1, T2EX, IC2 P4.2 P4.3		
P5.0-P5.1	I/O S H	Tri-state	PORT 5: 8-bit, bit-directional I/O port. This port is not bit addressable. The alternate functions are described below: P5.0, PWM6 P5.1, PWM7 P5[7:2] = SEG [15:10]		
P5.2-P5.7	I/O S H	High			
P6.0-P6.7	I/O D S H	High	PORT 6: 8-bit, bit-directional I/O port. This port is not bit addressable. P6[7:0] = SEG [23:16]		
P7.0-P7.7	I/O S H	High	PORT 7: 8-bit, bit-directional I/O port. This port is not bit addressable. P7[7:0] = SEG [31:24]		
SEG0-SEG9	O	Low	LCD segment outputs. Can also be used as DC output ports specified by code option.		
DH1, DH2	I	-	Capacitor input for LCD driver.		
COM0-COM3	O	Low	LCD common outputs.		
				1/3 Duty	1/4 Duty
			COM0	Used	Used
			COM1	Used	Used
			COM2	Used	Used
			COM3	Not Used	Used
			The LCD alternating frequency can be selected by code option.		

Note : TYPE I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain S: Schmitt Trigger



5.1 Port 4

Port 4, SFR P4 at address A5H, is a 4-bit multipurpose programmable I/O port which functions are I/O and chip-select function. It has four different operation modes:

- Mode 0 - P4.0 ~ P4.3 is 4-bit bi-directional I/O port which is the same as port 1. The default Port 4 is a general I/O function.
- Mode1 - P4.0 ~ P4.3 are read data strobe signals which are synchronized with $\overline{RD}$ signal at specified addresses. These read data strobe signals can be used as chip-select signals for external peripherals.
- Mode2 - P4.0 ~ P4.3 are write data strobe signals which are synchronized with $\overline{WR}$ signal at specified addresses. These write data strobe signals can be used as chip-select signals for external peripherals.
- Mode3 - P4.0 ~ P4.3 are read/write data strobe signals which are synchronized with $\overline{RD}$ or $\overline{WR}$ signal at specified addresses. These read/write data strobe signals can be used as chip-select signals for external peripherals.

When Port 4 is configured with the feature of chip-select signals, the chip-select signal address range depends on the contents of the SFR P4xAH, P4xAL, P4CONA and P4CONB. P4xAH and P4xAL contain the 16-bit base address of P4.x. P4CONA and P4CONB contain the control bits to configure the Port 4 operation mode.

6. MEMORY ORGANIZATION

The W79E217 separates the memory into two sections; Program Memory and Data Memory. Program Memory stores instruction op-codes, while Data Memory stores data or memory-mapped devices.

6.1 Program Memory (on-chip Flash)

W79E217 includes one 64K bytes of main FLASH EPROM for application program (AP FLASH EPROM) and one 4K bytes of FLASH EPROM for loader program (LD FLASH EPROM) to operate the in-system programming (ISP) feature, and one 2K bytes of NVM Flash EPROM for data storage. The 64K bytes Flash EPROM is AP0 bank. The default active bank is AP0.

In normal operation, the microcontroller will execute the code from main FLASH EPROM. By setting program registers, user can force the microcontroller to switch to programming mode which will cause it to execute the code (loader program) from the 4K bytes of auxiliary LD FLASH EPROM to update the contents of the 64K bytes of main FLASH EPROM. After reset, the microcontroller will executes the new application program in the main FLASH EPROM. This ISP feature makes the job easy and efficient in which the application needs to update firmware frequently without opening the chassis.

6.2 Data Memory

W79E217 can access up to 64Kbytes of external Data Memory. This memory region is accessed by the MOVX instructions. Unlike the 8051 derivatives, W79E217 contains on-chip 2 Kbytes of Data Memory, which only can be accessed by MOVX instructions. These 2 Kbytes of SRAM is between address 0000h and 07FFh. Access to the on-chip Data Memory is optional under software control. When enabled by DME0 bit of PMR register, a MOVX instruction that uses this area will go to the on-chip RAM. If MOVX instruction accesses the addresses greater than 07FFh CPU will automatically access external memory through Port 0 and 2. When disabled, the 2 KB memory area is transparent to the system memory map. Any MOVX directed to the space between 0000h and FFFFh goes to the expanded bus on the Port 0 and 2. This is the default condition. In addition, the device has the standard 256 bytes of on-chip RAM. This can be accessed either by direct addressing or by indirect addressing. There are also some Special Function Registers (SFRs), which can only be accessed by direct addressing.

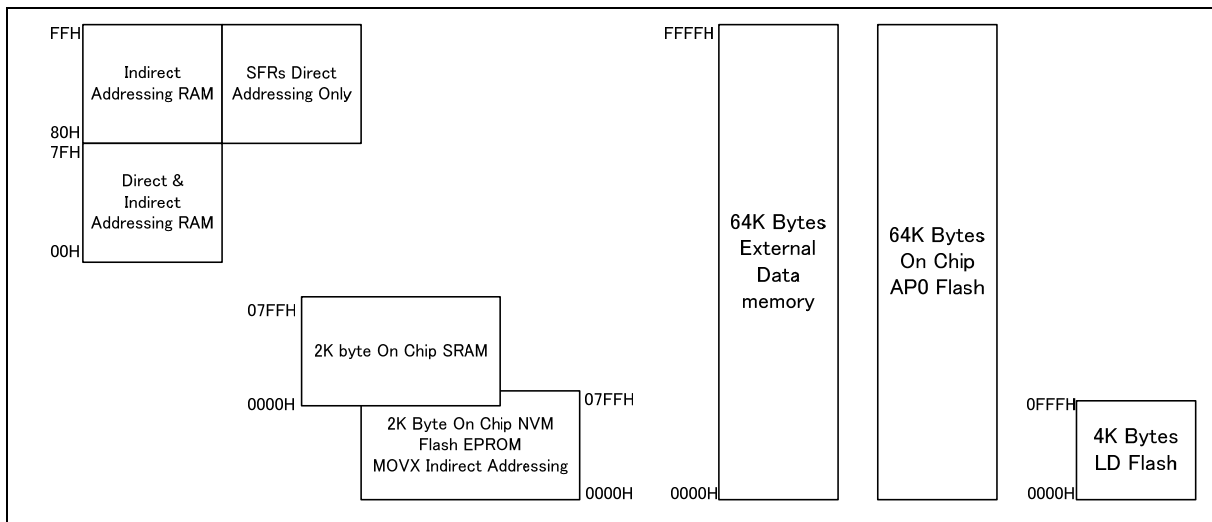


Figure 6-1: W79E217A Memory Map

6.3 Auxiliary SRAM

W79E217 has a 2 KB of data space SRAM which is read/write accessible and is memory mapped. This on-chip SRAM is accessed by the MOVX instruction. There is no conflict or overlap among the 256 bytes scratch-pad memory and the 2 KB auxiliary sram as they use different addressing modes and instructions. Access to the on-chip Data Memory is optional under software control. Set DME0 bit of PMR SFR to 1 will enable the on-chip 2 KB MOVX SRAM and at the same time EnNVM bit must be cleared as NVM memory uses the same instruction of MOVX. Refer to Table 6-3: W79E217 NVM page (n) area definition table.

6.4 2-KB NVM Data Flash Memory

W79E217 2-KB NVM memory block shown in the diagram on Figure 6-1, shares the same address as AUX-RAM address.

Due to overlapping of AUX-RAM, NVM data memory and external data memory physical address, the following table is defined. EnNVM bit (NVMCON.5) will enable read access to NVM data memory area. DME0 (PMR.0) will enable read access to AUX-RAM.

ENNVM	DME0	DATA MEMORY AREA
0	0	Enable External RAM read/write access by MOVX
0	1	Enable AUX-RAM read/write access by MOVX
1	X	Enable NVM data Memory read access by MOVX only. If EER or EWR is set and NVM flash erase or write control is busy, to set this bit read NVM data is invalid.

Table 6-1: Bits setting for MOVX access to Data Memory Area

INSTRUCTIONS		ENNVM = 1	
		NVM SIZE = SRAM (2K)	
		ADDR ≤ 2K	ADDR > 2K
Read access	MOVX A, @DPTR (Read)	NVM	Ext memory
	MOVX A, @R0 (Read)	NVM	NOP
	MOVX A, @R1 (Read)	NVM	NOP
Write access	MOVX @DPTR, A (Write)	NOP	Ext memory
	MOVX @R0, A (Write)	NOP	NOP
	MOVX @R1, A (Write)	NOP	NOP

Table 6-2: MOVX read/write access destination

Preliminary W79E217A Data Sheet



It is partition into **32** pages area and each page has 64 bytes data as below figure. The page 0 is from 0000h ~ 003Fh, page 1 is from 0040h ~ 007Fh until page 31 address located at 07C0h ~ 07FFh.

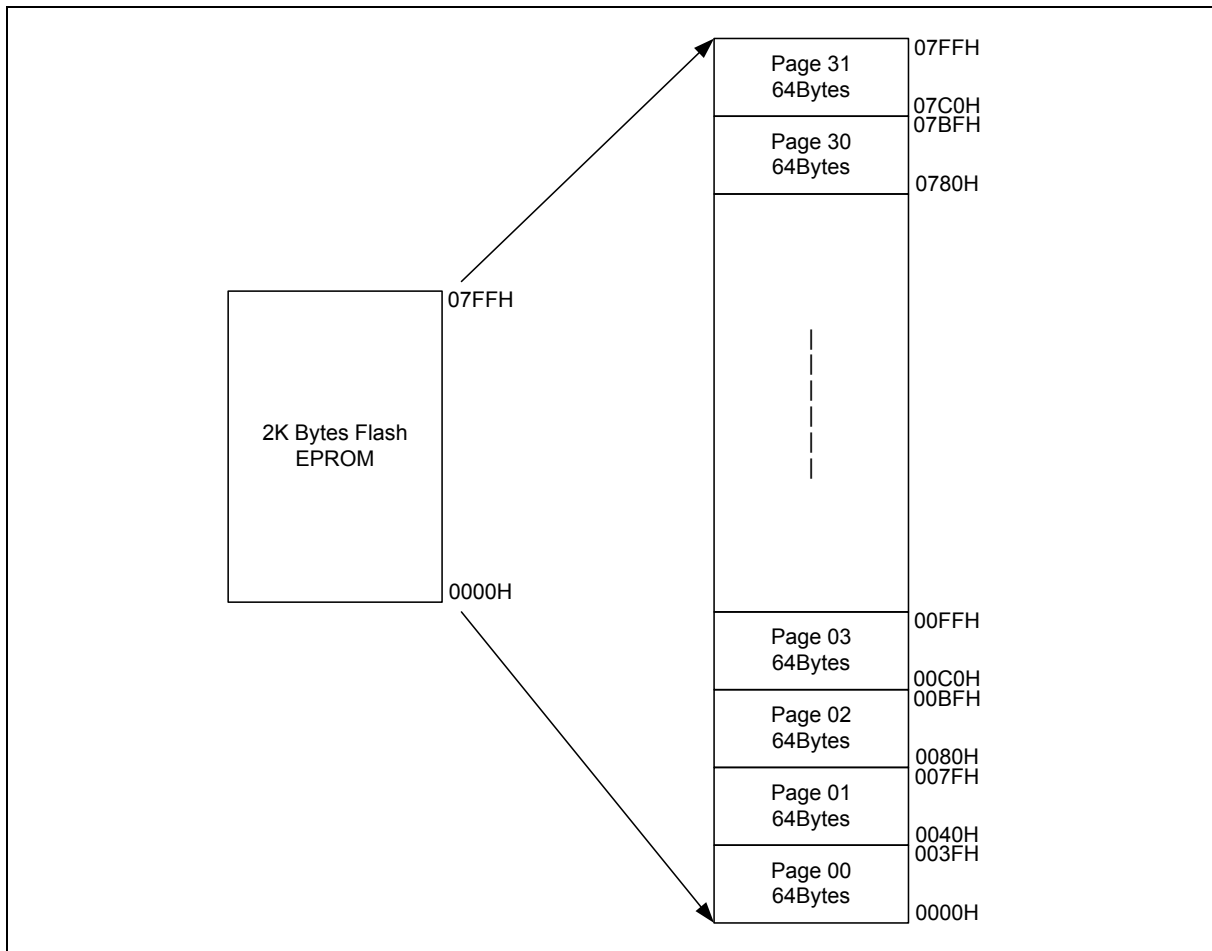


Figure 6-2: W79E217 NVM Memory Mapping

Preliminary W79E217A Data Sheet



PAGE	START ADDRESS	END ADDRESS	PAGE	START ADDRESS	END ADDRESS
0	0000h	003Fh	16	0400h	043Fh
1	0040h	007Fh	17	0440h	047Fh
2	0080h	00BFh	18	0480h	04BFh
3	00C0h	00FFh	19	04C0h	04FFh
4	0100h	013Fh	20	0500h	053Fh
5	0140h	017Fh	21	0540h	057Fh
6	0180h	01BFh	22	0580h	05BFh
7	01C0h	01FFh	23	05C0h	05FFh
8	0200h	023Fh	24	0600h	063Fh
9	0240h	027Fh	25	0640h	067Fh
10	0280h	02BFh	26	0680h	06BFh
11	02C0h	02FFh	27	06C0h	06FFh
12	0300h	033Fh	28	0700h	073Fh
13	0340h	037Fh	29	0740h	077Fh
14	0380h	03BFh	30	0780h	07BFh
15	03C0h	03FFh	31	07C0h	07FFh

Table 6-3: W79E217 NVM page (n) area definition table

It has a dedicated On-Chip RC Oscillator that is fixed at 6MHz +/- 25% frequency to support clock source for the 2K NVM data Flash Memory. The on chip oscillator is enabled only during program or erase operation, through EWR or EER in NVMCON SFR. EWR or EER bits are cleared by hardware after program or erase operation completed. The program/erase time is automatically controlled by hardware.

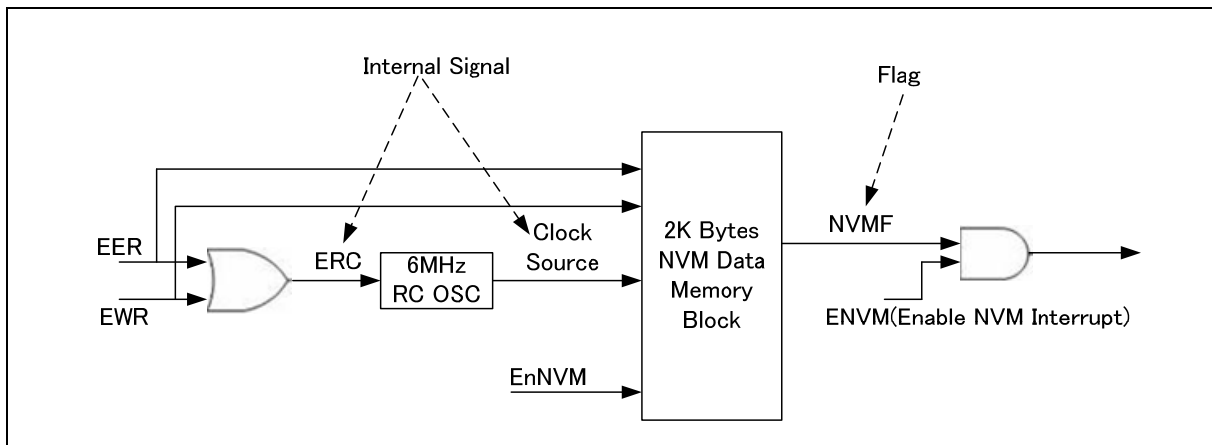


Figure 6-3: NVM control

6.4.1 Operation

User is required to enable EnNVM (NVMCON.5) bit for all NVM access (read/write/erase).



Before write data to NVM memory, the page must be erased. A page is erased by setting page address which address will decode and enable page (n) on NVMADDRH and NVMAADDRL, then set EER (NVMCON.7) and EnNVM (NVMCON.5). The device will then automatic execute page erase. When completed, NVMF will be set by hardware. NVMF should be cleared by software. Interrupt request will be generated if ENVM (EIE1.5) is enabled. EER bit will be cleared by hardware when erase is completed. The total erase time is about 5ms.

For write, user must set address and data to NVMADDRH/L and NVMDAT, respectively. And then set EWR (NVMCON.6) and EnNVM (NVMCON.5) to enable data write. When completed, the device will set NVMF flag. NVMF flag should be cleared by software. Similarly, interrupt request will be generated if ENVM (EIE1.5) is enabled. The program time is about 50us.

The following shows some examples of NVM operations:

Read NVM data is by MOVX A,@DPTR/R0/R1 instruction:

A read exceed 2k will read the external address

Example1: DPTR=0x07FF, R0/R1 = 0xFF, XRAMAH=0x07, EnNVM=1

MOVX A,@DPTR → read NVM data at address 0x07FF

MOVX A,@R0 → read NVM data at address 0x07FF

MOVX A,@R1 → read NVM data at address 0x07FF

Example2: DPTR = 0x2000, EnNVM=1, DME0=0

MOVX A,@DPTR → read external RAM data at address 0x2000,

Erase NVM by SFR register:

Example1: NVMADDRH = 0x07, NVMAADDRL = 0xF0, page 31 will be enabled. After set EER, the page 31 will be erased.

Example2: NVMADDRH = 0x10, NVMAADDRL = 0x00, invalid NVM erase instruction (address exceed NVM boundary).

Write NVM by SFR register:

Example1: NVMADDRH = 0x07, NVMAADDRL = 0xF0

After set EWR, data will be written to the NVM address = 0x07F0 location.

Example2: NVMADDRH = 0x10, NVMAADDRL = 0x00, after set EWR, invalid NVM write instruction (address exceed NVM boundary).

During erase, write is invalid. Likewise, during write, erase is invalid. An erase or write is invalid if NVMF is not clear by software. A write to NVMADDRH and NVMAADDRL is invalid during Erase or Write, and a write to NVMDAT is invalid only during NVM write access.

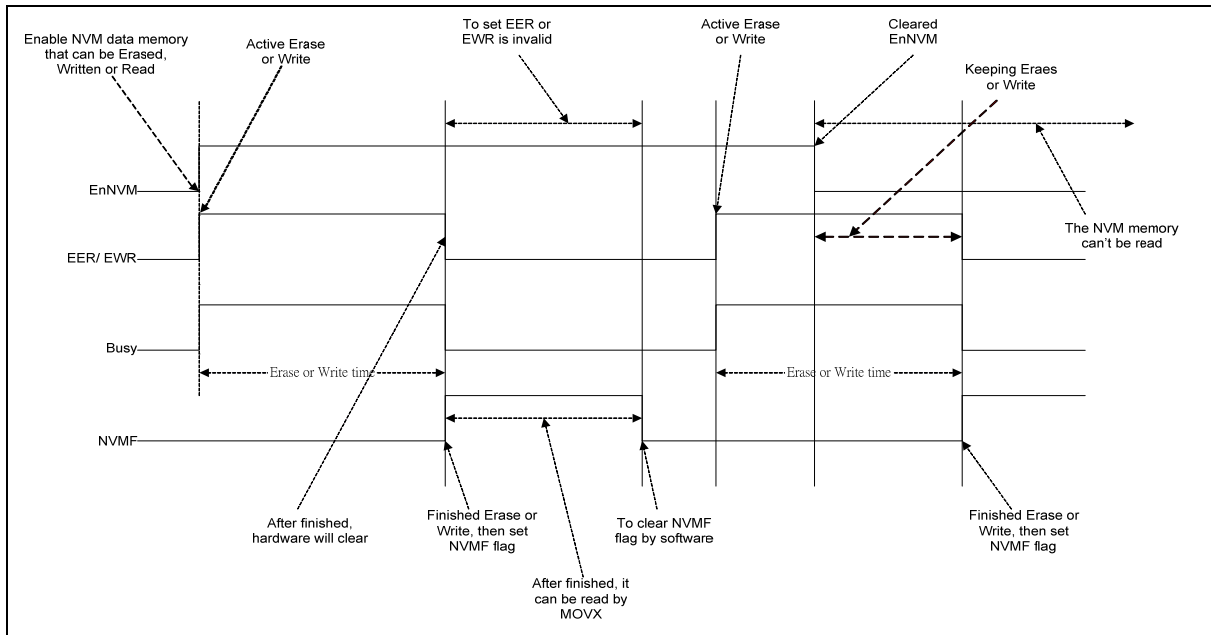


Figure 6-4: NVM data memory control timing

For security purposes, this NVM data flash provides an independent “Lock bit” located in Security bits. It is used to protect the customer’s 2K bytes of data code. It may be enabled after the external programmer finishes the programming and verifying sequence. Once this bit is set to logic 0, the 2K bytes of NVM Flash EPROM data can not be accessed again by external device.

- Note:
1. NVMF can be polled or by h/w interrupt to indicate NVM data memory erase or write operation has completed.
 2. While user program is erasing or writing to NVM data memory, the PC counter will continue to fetch for next instruction.
 3. When uC is in idle mode and if NVM interrupt and global interrupt are enabled, the completion of either erasing or programming the NVM data memory will exit the idle condition.

Preliminary W79E217A Data Sheet



7. SPECIAL FUNCTION REGISTERS

The W79E217 uses Special Function Registers (SFR) to control and monitor peripherals. The SFR reside in register locations 80-FFh and are only accessed by direct addressing. The W79E217 contains all the SFR present in the standard 8051/52, as well as some additional SFR, and, in some cases, unused bits in the standard 8051/52 have new functions. SFR whose addresses end in 0 or 8 (hex) are bit-addressable. The following table of SFR is condensed, with eight locations per row. Empty locations indicate that there are no registers at these addresses.

F8	EIP	EIE1	EIP1	CCL0 /PCNTL	CCH0 /PCNTH	CCL1 /PLSCNTL	CCH1 /PLSCNTH	INTCTRL
F0	B			SPCR	SPSR	SPDR	I2CSADEN	EIPH
E8	EIE	I2CON	I2ADDR	NVMADDR RH	I2DAT	I2STATUS	I2CLK	I2TIMER
E0	ACC	ADCCON	ADCH	ADCL	LCDCN	PDTC1	PDTC0	PWMCON4
D8	WDCON	PWMPL	PWM0L	NVMADDR L	PWMCON1	PWM2L	PWM6L	PWMCON3
D0	PSW	PWMPH	PWM0H	NVMDAT	QEICON	PWM2H	PWM6H	WDCON2
C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	PWMCON2	PWM4L
C0	SCON1	SBUF1	T3MOD	T3CON	PMR	FSPLT	ADCPS	TA
B8	IP	SADEN	SADEN1	POVM	POVD	PIO	PWMEN	PWM4H
B0	P3	P5	P6	P7	RCAP3L	RCAP3H	EIP1H	IPH
A8	IE	SADDR	SADDR1	LCDPT	SFRAL	SFRAH	SFRFD	SFRCN
A0	P2	XRAMAH	P4CSIN	CAPCON0	CAPCON1	P4	CCL2 /MAXCNTL	CCH2 /MAXCNTH
98	SCON	SBUF	P42AL	P42AH	P43AL	P43AH	NVMCON	CHPCON
90	P1	EXIF	P4CONA	P4CONB	P40AL	P40AH	P41AL	P41AH
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	CKCON1
80	P0	SP	DPL	DPH	TL3	TH3	LCDDATA	PCON

Table 7-1: Special Function Register Location Table

Preliminary W79E217A Data Sheet



SYMBOL	DEFINITION	ADD RESS	BIT_ADDRESS,								SYMBOL	RESET	
			MSB	LSB									
INTCTRL	INTERRUPT CONTROL REGISTER	FFH	-	-	INT5CT1	INT5CT0	INT4CT1	INT4CT0	INT3CT1	INT3CT0	xx00 0000B		
CCH1 /PLSCNTH	CAPTURE COUNTER HIGH 1 REGISTER	FEH	CCH1.7 /PLSCNTH.7	CCH1.6 /PLSCNTH.6	CCH1.5 /PLSCNTH.5	CCH1.4 /PLSCNTH.4	CCH1.3 /PLSCNTH.3	CCH1.2 /PLSCNTH.2	CCH1.1 /PLSCNTH.1	CCH1.0 /PLSCNTH.0	0000 0000B		
CCL1 /PLSCNTL	CAPTURE COUNTER LOW 1 REGISTER	FDH	CCL1.7 /PLSCNTL.7	CCL1.6 /PLSCNTL.6	CCL1.5 /PLSCNTL.5	CCL1.4 /PLSCNTL.4	CCL1.3 /PLSCNTL.3	CCL1.2 /PLSCNTL.2	CCL1.1 /PLSCNTL.1	CCL1.0 /PLSCNTL.0	0000 0000B		
CCH0 /PCNTH	CAPTURE COUNTER HIGH 0 REGISTER	FCH	CCH0.7 /PCNTH.7	CCH0.6 /PCNTH.6	CCH0.5 /PCNTH.5	CCH0.4 /PCNTH.4	CCH0.3 /PCNTH.3	CCH0.2 /PCNTH.2	CCH0.1 /PCNTH.1	CCH0.0 /PCNTH.0	0000 0000B		
CCL0 /PCNTL	CAPTURE COUNTER LOW 0 REGISTER	FBH	CCL0.7 /PCNTL.7	CCL0.6 /PCNTL.6	CCL0.5 /PCNTL.5	CCL0.4 /PCNTL.4	CCL0.3 /PCNTL.3	CCL0.2 /PCNTL.2	CCL0.1 /PCNTL.1	CCL0.0 /PCNTL.0	0000 0000B		
EIP1	EXTENDED INTERRUPT PRIORITY 1	FAH	-	-	PNVMI	PCPTF	PT3	PBKF	PPWMF	PSPI	xx00 0000B		
EIE1	INTERRUPT ENABLE 1	F9H	-	-	ENVM	ECPTF	ET3	EBK	EPWM	ESPI	xx00 0000B		
EIP	EXTENDED INTERRUPT PRIORITY	F8H	(FF) PS1	(FE) PX5	(FD) PX4	(FC) PWDI	(FB) PX3	(FA) PX2	(F9) -	(F8) PI2C	0000 00x0B		
EIPH	EXTENDED INTERRUPT HIGH PRIORITY	F7H	PS1H	PX5H	PX4H	PWDIH	PX3H	PX2H	-	PI2CH	0000 00x0B		
I2CSADEN	I2C SLAVE ADDRESS MASK	F6H	I2CSAD EN.7	I2CSAD EN.6	I2CSAD EN.5	I2CSAD EN.4	I2CSAD EN.3	I2CSAD EN.2	I2CSAD EN.1	I2CSAD EN.0	1111 1110B		
SPDR	SERIAL PERIPHERAL DATA REGISTER	F5H	SPD.7	SPD.6	SPD.5	SPD.4	SPD.3	SPD.2	SPD.1	SPD.0	xxxx xxxxB		
SPSR	SERIAL PERIPHERAL STATUS REGISTER	F4H	SPIF	WCOL	SPIOVF	MODF	DRSS	-	-	-	0000 0xxxB		
SPCR	SERIAL PERIPHERAL CONTROL REGISTER	F3H	SSOE	SPE	LSBFE	MSTR	CPOL	CPHA	SPR1	SPR0	0000 0100B		
B	B REGISTER	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	0000 0000B		
I2TIMER	I2C TIMER COUNTER REGISTER	EFH	-	-	-	-	-	ENTI	DIV4	TIF	xxxx x000B		
I2CLK	I2C CLOCK RATE	EEH	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0	0000 0000B		
I2STATUS	I2C STATUS REGISTER	EDH									1111 1000B		
I2DAT	I2C DATA	ECH	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0	0000 0000B		
NVMADDRH	NVM HIGH BYTE ADDRESS	EBH	-	-	-	-	-	NVMAD DRH.10	NVMAD DRH.9	NVMAD DRH.8	xxxx x000B		
I2ADDR	I2C SLAVE ADDRESS	EAH	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	GC	0000 0000B		
I2CON	I2C CONTROL REGISTER	E9H	-	ENS	STA	STO	SI	AA	I2CIN	-	X000 000xB		
EIE	EXTENDED INTERRUPT ENABLE	E8H	(EF) ES1	(EE) EX5	(ED) EX4	(EC) EWDI	(EB) EX3	(EA) EX2	(E9)	(E8) EI2C	0000 00x0B		
PWMCON4	PWM CONTROL REGISTER 4	E7H	PWMEOM	PWMOOM	PWM6OM	PWM7OM	-	-	-	BKF	0000 xxx0B		
PDTC0	DEAD TIME CONTROL REGISTER 0	E6H	PDTC0.7	PDTC0.6	PDTC0.5	PDTC0.4	PDTC0.3	PDTC0.2	PDTC0.1	PDTC0.0	0000 0000B		
PDTC1	DEAD TIME CONTROL REGISTER 1	E5H	PDTC1.7	PDTC1.6	PDTC1.5	PDTC1.4	PDTC1.3	PDTC1.2	PDTC1.1	PDTC1.0	0000 0000B		
LCDCN	LCD CONTROL REGISTER	E4H	LCDEN	Clear	Duty	Pump	-	FS2	FS1	FS0	0000 x000B		
ADCL	ADC CONVERTER RESULT LOW BYTE	E3H	ADCLK1	ADCLK0	-	-	-	-	ADC.1	ADC.0	00xx xxxxB		

Preliminary W79E217A Data Sheet



Continued

SYMBOL	DEFINITION	ADD RESS	MSB LSB	BIT_ADDRESS,							SYMBOL	RESET
ADCH	ADC CONVERTER RESULT HIGH BYTE	E2H	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2	xxxx xxxxB	
ADCCON	ADC CONTROL REGISTER	E1H	ADCEN	-	ADCEX	ADCI	ADCS	AADR2	AADR1	AADR0	0x00 0000B	
ACC	ACCUMULATOR	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	0000 0000B	
PWMCON3	PWM CONTROL REGISTER 3	DFH	PWM7B	PWM6B	PWM5B	PWM4B	PWM3B	PWM2B	PWM1B	PWM0B	0000 0000B	
PWM6L	PWM 6 LOW BITS REGISTER	DEH	PWM6.7	PWM6.6	PWM6.5	PWM6.4	PWM6.3	PWM6.2	PWM6.1	PWM6.0	0000 0000B	
PWM2L	PWM 2 LOW BITS REGISTER	DDH	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0	0000 0000B	
PWMCON1	PWM CONTROL REGISTER 1	DCH	PWMRU N	Load	PWMF	CLRPW M	PWM6I	PWM4I	PWM2I	PWM0I	0000 0000B	
NVMADDR1	NVM LOW BYTE ADDRESS	DBH	NVMAD DRH.7	NVMAD DRH.6	NVMAD DRH.5	NVMAD DRH.4	NVMAD DRH.3	NVMAD DRH.2	NVMAD DRH.1	NVMAD DRH.0	0000 0000B	
PWM0L	PWM 0 LOW BITS REGISTER	DAH	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0	0000 0000B	
PWMPL	PWM COUNTER LOW REGISTER	D9H	PWMP.7	PWMP.6	PWMP.5	PWMP.4	PWMP.3	PWMP.2	PWMP.1	PWMP.0	0000 0000B	
WDCON	WATCH-DOG CONTROL	D8H	(DF) -	(DE) POR	(DD) -	(DC) -	(DB) WDIF	(DA) WTRF	(D9) EWT	(D8) RWT	0100 0000B	
WDCON2	WATCH-DOG CONTROL2	D7H	-	-	-	-	-	-	-	STRLD	0000 0000B	
PWM6H	PWM 6 HIGH BITS REGISTER	D6H	-	-	-	-	PWM6.1 1	PWM6.1 0	PWM6.9	PWM6.8	xxxx 0000B	
PWM2H	PWM 2 HIGH BITS REGISTER	D5H	-	-	-	-	PWM2.1 1	PWM2.1 0	PWM2.9	PWM2.8	xxxx 0000B	
QEICON	QEI CONTROL REGISTER	D4H	-	-	-	DISIDX	DIR	QEIM1	QEIM0	QEIEI	xxx0 0000B	
NVMDAT	NVM DATA	D3H	NVMDA T.7	NVMDA T.6	NVMDA T.5	NVMDA T.4	NVMDA T.3	NVMDA T.2	NVMDA T.1	NVMDA T.0	0000 0000B	
PWM0H	PWM 0 HIGH BITS REGISTER	D2H	-	-	-	-	PWM0.1 1	PWM0.1 0	PWM0.9	PWM0.8	xxxx 0000B	
PWMPH	PWM COUNTER HIGH REGISTER	D1H	-	-	-	-	PWMP.1 1	PWMP.1 0	PWMP.9	PWMP.8	xxxx 0000B	
PSW	PROGRAM STATUS WORD	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P	0000 0000B	
PWM4L	PWM 4 LOW BITS REGISTER	CFH	PWM4.7	PWM4.6	PWM4.5	PWM4.4	PWM4.3	PWM4.2	PWM4.1	PWM4.0	0000 0000B	
PWMCON2	PWM CONTROL REGISTER 2	CEH	BKCH	BKPS	BPEN	BKEN	FP1	FP0	PMOD1	PMOD0	0000 0000B	
TH2	T2 REG. HIGH	CDH	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0	0000 0000B	
TL2	T2 REG. LOW	CCH	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0	0000 0000B	
RCAP2H	T2 CAPTURE LOW	CBH	RCAP2H .7	RCAP2H .6	RCAP2H .5	RCAP2H .4	RCAP2H .3	RCAP2H .2	RCAP2H .1	RCAP2H .0	0000 0000B	
RCAP2L	T2 CAPTURE HIGH	CAH	RCAP2L .7	RCAP2L .6	RCAP2L .5	RCAP2L .4	RCAP2L .3	RCAP2L .2	RCAP2L .1	RCAP2L .0	0000 0000B	
T2MOD	TIMER 2 MODE	C9H	HC5	HC4	HC3	HC2	T2CR	-	-	DCEN	0000 0xx0B	
T2CON	TIMER 2 CONTROL	C8H	(CF) TF2	(CE) EXF2	(CD) RCLK	(CC) TCLK	(CB) EXEN2	(CA) TR2	(C9) C/ $\bar{T}$	(C8) CP/RL2	0000 0000B	
TA	TIME ACCESS REGISTER	C7H	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0	0000 0000B	
DDIO	DISABLE DIGITAL I/O	C6H	DDIO.7	DDIO.6	DDIO.5	DDIO.4	DDIO.3	DDIO.2	DDIO.1	DDIO.0	0000 0000B	
FSPLT	FAULT SAMPLING TIME REGISTER	C5H	SCMP1	SCMP0	SFP1	SFP0	SFCEN	SFCST	SFCDIR	LSBD	0000 0000B	
PMR	POWER MANAGEMENT REGISTER	C4H	-	-	-	-	-	ALEOFF	-	DME0	xxxx x0x0B	
T3CON	TIMER 3 CONTROL	C3H	TF3	-	-	-	-	TR3	-	CMP/RL3	0xxx x0x0B	

Preliminary W79E217A Data Sheet



Continued

SYMBOL	DEFINITION	ADD RESS	MSB LSB	BIT_ADDRESS,						SYMBOL	RESET
T3MOD	TIMER 3 MODE CONTROL	C2H	ENLD	ICEN2	ICEN1	ICEN0	T3CR	-	-	-	0000 0xxxB
SBUF1	SERIAL BUFFER 1	C1H	SBUF1.7	SBUF1.6	SBUF1.5	SBUF1.4	SBUF1.3	SBUF1.2	SBUF1.1	SBUF1.0	xxxx xxxxB
SCON1	SERIAL CONTROL 1	C0H	(BF) SM0_1/F E_1	(BE) SM1_1	(BD) SM2_1	(BC) REN_1	(BB) TB8_1	(BA) RB8_1	(B9) TI_1	(B8) RI_1	0000 0000B
PWM4H	PWM 4 HIGH BITS REGISTER	BFH	-	-	-	-	PWM4.1 1	PWM4.1 0	PWM4.9	PWM4.8	xxxx 0000B
PWMEN	PWM OUTPUT ENABLE REGISTER	BEH	PWM7E N	PWM6E N	PWM5E N	PWM4E N	PWM3E N	PWM2E N	PWM1E N	PWM0E N	0000 0000B
PIO	PWM PIN OUTPUT SOURCE SELECT	BDH	PIO7	PIO6	PIO5	PIO4	PIO3	PIO2	PIO1	PIO0	0000 0000B
POVD	PWM OUTPUT STATE REGISTERS	BCH	POVD.7	POVD.6	POVD.5	POVD.4	POVD.3	POVD.2	POVD.1	POVD.0	0000 0000B
POVM	PWM OUTPUT OVERRIDE CONTROL REGISTERS	BBH	POVM.7	POVM.6	POVM.5	POVM.4	POVM.3	POVM.2	POVM.1	POVM.0	0000 0000B
SADEN1	SLAVE ADDRESS MASK 1	BAH	SADEN1 .7	SADEN1 .6	SADEN1 .5	SADEN1 .4	SADEN1 .3	SADEN1 .2	SADEN1 .1	SADEN1 .0	0000 0000B
SADEN	SLAVE ADDRESS MASK	B9H	SADEN. 7	SADEN. 6	SADEN. 5	SADEN. 4	SADEN. 3	SADEN. 2	SADEN. 1	SADEN. 0	0000 0000B
IP	INTERRUPT PRIORITY	B8H	(BF) RD	(BE) PADC	(BD) PT2	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	0000 0000B
IPH	INTERRUPT HIGH PRIORITY	B7H	-	PADCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	x000 0000B
EIP1H	EXTENDED INTERRUPT HIGH PRIORITY 1	B6H	-	-	PNVMIH	PCPTFH	PT3H	PBKFH	PPWMH	PSPIH	xx00 0000B
RCAP3H	RELOAD CAPTURE 3 HIGH REGISTER	B5H	RCAP3H .7	RCAP3H .6	RCAP3H .5	RCAP3H .4	RCAP3H .3	RCAP3H .2	RCAP3H .1	RCAP3H .0	0000 0000B
RCAP3L	RELOAD CAPTURE 3 LOW REGISTER	B4H	RCAP3L .7	RCAP3L .6	RCAP3L .5	RCAP3L .4	RCAP3L .3	RCAP3L .2	RCAP3L .1	RCAP3L .0	0000 0000B
P7	PORT 7	B3H	SEG.31	SEG.30	SEG.29	SEG.28	SEG.27	SEG.26	SEG.25	SEG.24	1111 1111B
P6	PORT 6	B2H	SEG.23	SEG.22	SEG.21	SEG.20	SEG.19	SEG.18	SEG.17	SEG.16	1111 1111B
P5	PORT 5	B1H	SEG.15	SEG.14	SEG.13	SEG.12	SEG.11	SEG.10	PWM7	PWM6	1111 1111B
P3	PORT 3	B0H	(B7) RD	(B6) WR	(B5) T1/ IC1/QEB	(B4) T0/ ICO/QEA	(B3) /INT1	(B2) /INT0	(B1) TXD	(B0) RXD	1111 1111B
SFRCN	F/W FLASH CONTROL	AFH	-	WFWIN	NOE	NCE	CTRL3	CTRL2	CTRL1	CTRL0	x011 1111B
SFRFD	F/W FLASH DATA	AEH	D7	D6	D5	D4	D3	D2	D1	D0	xxxx xxxxB
SFRAH	F/W FLASH HIGH ADDRESS	ADH	A15	A14	A13	A12	A11	A10	A9	A8	0000 0000B
SFRAL	F/W FLASH LOW ADDRESS	ACH	A7	A6	A5	A4	A3	A2	A1	A0	0000 0000B
LCDPT	LCD POINTER	ABH	-	-	-	-	LCDPT. 3	LCDPT. 2	LCDPT. 1	LCDPT. 0	xxxx 0000B
SADDR1	SLAVE ADDRESS 1	AAH	SADDR1 .7	SADDR1 .6	SADDR1 .5	SADDR1 .4	SADDR1 .3	SADDR1 .2	SADDR1 .1	SADDR1 .0	0000 0000B
SADDR	SLAVE ADDRESS	A9H	SADDR. 7	SADDR. 6	SADDR. 5	SADDR. 4	SADDR. 3	SADDR. 2	SADDR. 1	SADDR. 0	0000 0000B
IE	INTERRUPT ENABLE	A8H	(AF) EA	(AE) EADC	(AD) ET2	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	0000 0000B
CCH2/MAX CNTH	INPUT CAPTURE 2 HIGH REGISTER/ MAXIMUM COUNTER HIGH REGISTER	A7h	CCH2.7 /MAXCN TH.7	CCH2.6 /MAXCN TH.6	CCH2.5 /MAXCN TH.5	CCH2.4 /MAXCN TH.4	CCH2.3 /MAXCN TH.3	CCH2.2 /MAXCN TH.2	CCH2.1 /MAXCN TH.1	CCH2.0 /MAXCN TH.0	0000 0000B
CCL2/MAX CNTL	INPUT CAPTURE 2 LOW REGISTER/ MAXIMUM COUNTER LOW REGISTER	A6h	CCL2.7 /MAXCN TL.7	CCL2.6 /MAXCN TL.6	CCL2.5 /MAXCN TL.5	CCL2.4 /MAXCN TL.4	CCL2.3 /MAXCN TL.3	CCL2.2 /MAXCN TL.2	CCL2.1 /MAXCN TL.1	CCL2.0 /MAXCN TL.0	0000 0000B
P4	PORT 4	A5H	-	-	-	-	P4.3	P4.2	T2EX/IC 2	STADC	xxxx 1111B

Preliminary W79E217A Data Sheet



Continued

SYMBOL	DEFINITION	ADD RESS	MSB LSB	BIT_ADDRESS,							SYMBOL	RESET
CAPCON1	CAPTURE CONTROL 1 REGISTER	A4H	-	-	ENF2	ENF1	ENF0	CPTF2	CPTF1/ DIRF	CPTF0/ QEIF	xx00 0000B	
CAPCON0	CAPTURE CONTROL 0 REGISTER	A3H	CCT2.1	CCT2.0	CCT1.1	CCT1.0	CCT0.1	CCT0.0	CCLD1	CCLD0	0000 0000B	
P4CSIN	P4 CS SIGN	A2H	P43INV	P42INV	P41INV	P40INV	-	PWDNH	RMWFP	POUP	0000 x000B	
XRAMAH	RAM HIGH BYTE ADDRESS	A1H	-	-	-	-	-	A10	A9	A8	0000 0000B	
P2	PORT 2	A0H	(A7) A15/ SDA	(A6) A14/ SCL	(A5) A13/ PWM5	(A4) A12/ PWM4	(A3) A11/ PWM3	(A2) A10/ PWM2	(A1) A9/ PWM1	(A0) A8/ PWM0	1111 1111B	
CHPCON	ON CHIP PROGRAMMING CONTROL	9FH	SWRST/ REBOOT	-	LD/AP	-	-	-	LDSEL	ENP	0000 0000B	
NVMCON	NVM CONTROL	9EH	EER	EWR	EnNVM	-	-	-	-	NVMF	000x xxx0B	
P43AH	HI ADDR. COMPARATOR OF P4.3	9DH	A15	A14	A13	A12	A11	A10	A9	A8	0000 0000B	
P43AL	LO ADDR. COMPARATOR OF P4.3	9CH	A7	A6	A5	A4	A3	A2	A1	A0	0000 0000B	
P42AH	HI ADDR. COMPARATOR OF P4.2	9BH	A15	A14	A13	A12	A11	A10	A9	A8	0000 0000B	
P42AL	LO ADDR. COMPARATOR OF P4.2	9AH	A7	A6	A5	A4	A3	A2	A1	A0	0000 0000B	
SBUF	SERIAL BUFFER	99H	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0	xxxx xxxxB	
SCON	SERIAL CONTROL	98H	(9F) SM0/FE	(9E) SM1	(9D) SM2	(9C) REN	(9B) TB8	(9A) RB8	(99) TI	(98) RI	0000 0000B	
P41AH	HI ADDR. COMPARATOR OF P4.1	97H	A15	A14	A13	A12	A11	A10	A9	A8	0000 0000B	
P41AL	LO ADDR. COMPARATOR OF P4.1	96H	A7	A6	A5	A4	A3	A2	A1	A0	0000 0000B	
P40AH	HI ADDR. COMPARATOR OF P4.0	95H	A15	A14	A13	A12	A11	A10	A9	A8	0000 0000B	
P40AL	LO ADDR. COMPARATOR OF P4.0	94H	A7	A6	A5	A4	A3	A2	A1	A0	0000 0000B	
P4CONB	P4 CONTROL REGISTER B	93H	P43FUN 1	P43FUN 0	P43CMP 1	P43CMP 0	P42FUN 1	P42FUN 0	P42CMP 1	P42CMP 0	0000 0000B	
P4CONA	P4 CONTROL REGISTER A	92H	P41FUN 1	P41FUN 0	P41CMP 1	P41CMP 0	P40FUN 1	P40FUN 0	P40CMP 1	P40CMP 0	0000 0000B	
EXIF	EXTERNAL INTERRUPT FLAG	91H	IE5	IE4	IE3	IE2	-	-	-	-	0000 xxxxB	
P1	PORT 1	90H	(97) ADC7	(96) ADC6	(95) ADC5	(94) ADC4	(93) TXD1/ ADC3	(92) RXD1/ ADC2	(91) ADC1/ Brake	(90) T2/ ADC0	1111 1111B	
CKCON1	CLOCK CONTROL 1	8FH	-	-	-	-	-	-	CCDIV1	CCDIV0	0000 0000B	
CKCON	CLOCK CONTROL	8EH	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0	0000 0001B	
TH1	TIMER HIGH 1	8DH	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0	0000 0000B	
TH0	TIMER HIGH 0	8CH	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0	0000 0000B	
TL1	TIMER LOW 1	8BH	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0	0000 0000B	
TL0	TIMER LOW 0	8AH	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0	0000 0000B	
TMOD	TIMER MODE	89H	GATE	$C/\overline{T}$	M1	M0	GATE	$C/\overline{T}$	M1	M0	0000 0000B	
TCON	TIMER CONTROL	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	0000 0000B	
PCON	POWER CONTROL	87H	SMOD	SMOD0	-	-	GF1	GF0	PD	IDL	00xx 0000B	
LCDDATA	LCD DATA	86H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	0000 0000B	
TH3	TIMER HIGH 3	85H	TH3.7	TH3.6	TH3.5	TH3.4	TH3.3	TH3.2	TH3.1	TH3.0	0000 0000B	
TL3	TIMER LOW 3	84H	TL3.7	TL3.6	TL3.5	TL3.4	TL3.3	TL3.2	TL3.1	TL3.0	0000 0000B	

Preliminary W79E217A Data Sheet



Continued

SYMBOL	DEFINITION	ADDRESS	MSB	BIT_ADDRESS,						SYMBOL	RESET
DPH	DATA POINTER HIGH	83H	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0	0000 0000B
DPL	DATA POINTER LOW	82H	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0	0000 0000B
SP	STACK POINTER	81H	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0	0000 0111B
P0	PORT 0	80H	(87) INT5	(86) INT4	(85) INT3	(84) INT2	(83) /SS	(82) SPCLK	(81) MOSI	(80) MISO	1111 1111B

Table 7-2: Special Function Registers

PORT 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0

Address: 80h

Port 0 is an open-drain 8-bit bi-directional I/O port. As an alternate function Port 0 can function as the multiplexed address/data bus to access off-chip memory. During the time when ALE is high, the LSB of a memory address is presented. When ALE is low, the port transits to a bi-directional data bus. This bus is used for reading external ROM and for reading or writing external RAM memory or peripherals. When used as a memory bus, the port provides active high drivers. The reset condition of Port 0 is tri-state. Pull-up resistors are required when using Port 0 as an I/O port.

BIT	NAME	FUNCTION
0	P0.0	MISO: SPI Master In Slave Out.
1	P0.1	MOSI: SPI Master Out Slave In.
2	P0.2	SPCLK: SPI Clock.
3	P0.3	/SS: Slave Select.
4	P0.4	INT2: External Interrupt 2.
5	P0.5	INT3: External Interrupt 3.
6	P0.6	INT4: External Interrupt 4.
7	P0.7	INT5: External Interrupt 5.

STACK POINTER

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP

Address: 81h

The Stack Pointer stores the Scratch-pad RAM address where the stack begins. In other words it always points to the top of the stack.

DATA POINTER LOW

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL

Address: 82h

This is the low byte of the standard 8032 16-bit data pointer.

Preliminary W79E217A Data Sheet



DATA POINTER HIGH

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH

Address: 83h

This is the high byte of the standard 8032 16-bit data pointer.

TIMER 3 LSB

Bit:	7	6	5	4	3	2	1	0
	TL3.7	TL3.6	TL3.5	TL3.4	TL3.3	TL3.2	TL3.1	TL3.0

Mnemonic: TL3

Address: 84h

BIT	NAME	FUNCTION
7-0	Timer 3 LSB	LSB of Timer3

TIMER 3 MSB

Bit:	7	6	5	4	3	2	1	0
	TH3.7	TH3.6	TH3.5	TH3.4	TH3.3	TH3.2	TH3.1	TH3.0

Mnemonic: TH3

Address: 85h

BIT	NAME	FUNCTION
7-0	Timer 3 MSB	MSB of Timer3

LCD DATA REGISTER

Bit:	7	6	5	4	3	2	1	0
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Mnemonic: LCDDATA

Address: 86h

BIT	NAME	FUNCTION
7-0	LCDDATA	Data written to this register will be display to the LCD Segment and Common. 0: Turn OFF LCD. 1: Turn ON LCD.

POWER CONTROL

Bit:	7	6	5	4	3	2	1	0
	SMOD	SMOD0	-	-	GF1	GF0	PD	IDL

Mnemonic: PCON

Address: 87h