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nuvoTon

8-bit Microcontroller

Table of Contents-

1. GENERAL DESCRIPTION

The W79E22X SERIES is a fast, 8051/52-compatible microcontroller with a redesigned processor core that eliminates wasted clock and memory cycles. Typically, the W79E22X SERIES executes instructions 1.5 to 3 times faster than that of the traditional 8051/52, depending on the type of instruction, and the overall performance is about 2.5 times better at the same crystal speed. As a result, with the fully-static CMOS design, the W79E22X SERIES can accomplish the same throughput with a lower clock speed, reducing power consumption.

The W79E22X SERIES provides 256 bytes of on-chip RAM; 1/2/2-KB of NVM Data Flash EPROM; 1/2/2-KB of auxiliary RAM; four 8-bit, bi-directional and bit-addressable I/O ports; an additional 4-bit port P4 and 2-bit port P5; three 16-bit timer/counters; Motion Feedback Module support; 2 UART serial ports; 1 channels of I2C with master/slave capability; 1 channels of Serial Peripheral Interface (SPI), 8 channels of 12 bit PWM with configurable dead time and 8 channels of 10-bit ADC. These peripherals are all supported by 20 interrupt sources with 4 levels of priority.

The W79E22X SERIES also contains a 16/32/64-KB Flash EPROM whose contents may be updated in-system by a loader program stored in an auxiliary, 4-KB Flash EPROM. Once the contents are confirmed, it can be protected for security.

2. FEATURES

- Fully-static-design 8-bit 4T-8051 CMOS microcontroller up to 40MHz.
- 16/32/64-KB of in-system-programmable Flash EPROM (AP Flash EPROM).
- 4-KB of Auxiliary Flash EPROM for the loader program (LD Flash EPROM). User can optionally reboot from LD Flash EPROM by pull low at either P4.3 or P3.6 and P3.7, at external reset.
- 1/2/2-KB auxiliary RAM, software-selectable, accessed by MOVX instruction.
- 1/2/2-KB of NVM Data Flash EPROM for customer data storage used.
- 256 bytes of scratch-pad RAM.
- Four 8-bit bi-directional ports; Port 0 has internal pull-up resisters enabled by software.
- Multipurpose I/O port4 (4 bits for 48L LQFP; 2 bits for 44L PLCC) with Chips select (CS) and boot function.
- Two bits bi-directional port5.
- Three 16-bit timers.
- One 16-bit Timer 3 for Motion Feed-Back Module.
- Motion Feedback Module - QEI decoder and 3 Inputs Capture.
- Eight channels of 12-bit PWM:-
  - Complementary paired output with programmable dead-time insertion.
  - Three modes: Edge aligned, center aligned and single shot.
  - Output override control for BLDC motor application.
- 10-bit ADC with 8-channel inputs.
- Two enhanced full-duplex UART with framing-error detection and automatic address recognition.
- One channel of I2C with master/slave capability.
- One channel of SPI with master/slave capability.
- Software programmable access cycle to external RAM/peripherals.
- 20 interrupt sources with four levels of priority.
- Software reset function.
- Optional H/L state of ALE/PSEN during power down mode.
- Built-in power management.
- Code protection.
- Package:
  - Lead Free (RoHS) PLCC 44: W79E225APG
  - Lead Free (RoHS) LQFP 48: W79E225ALG
  - Lead Free (RoHS) PLCC 44: W79E226APG
  - Lead Free (RoHS) LQFP 48: W79E226ALG
  - Lead Free (RoHS) PLCC 44: W79E227APG
  - Lead Free (RoHS) LQFP 48: W79E227ALG

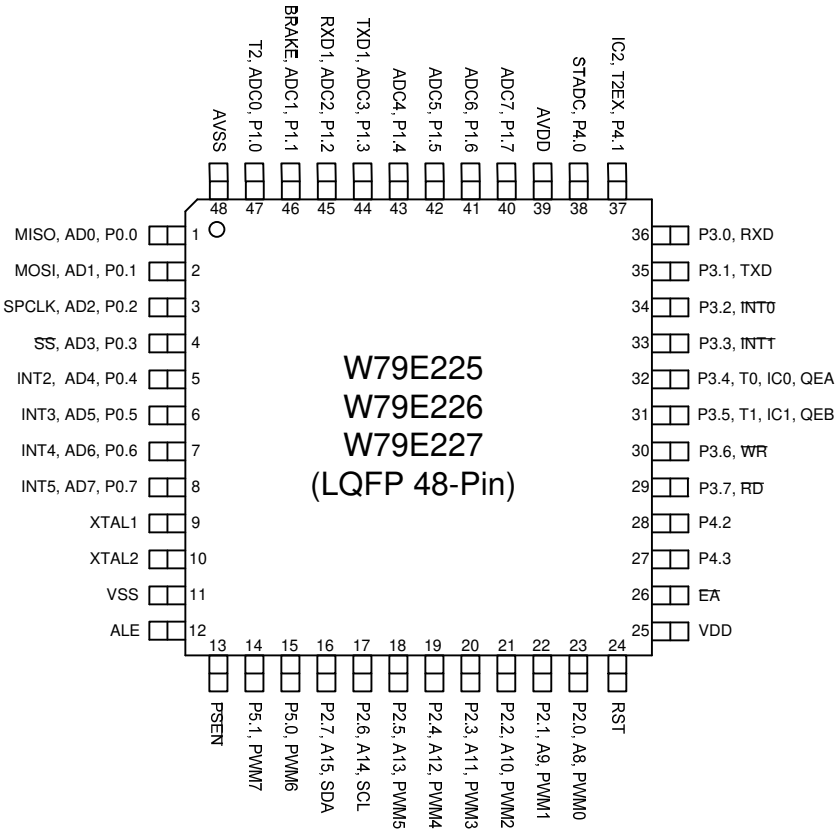
3. PARTS INFORMATION LIST

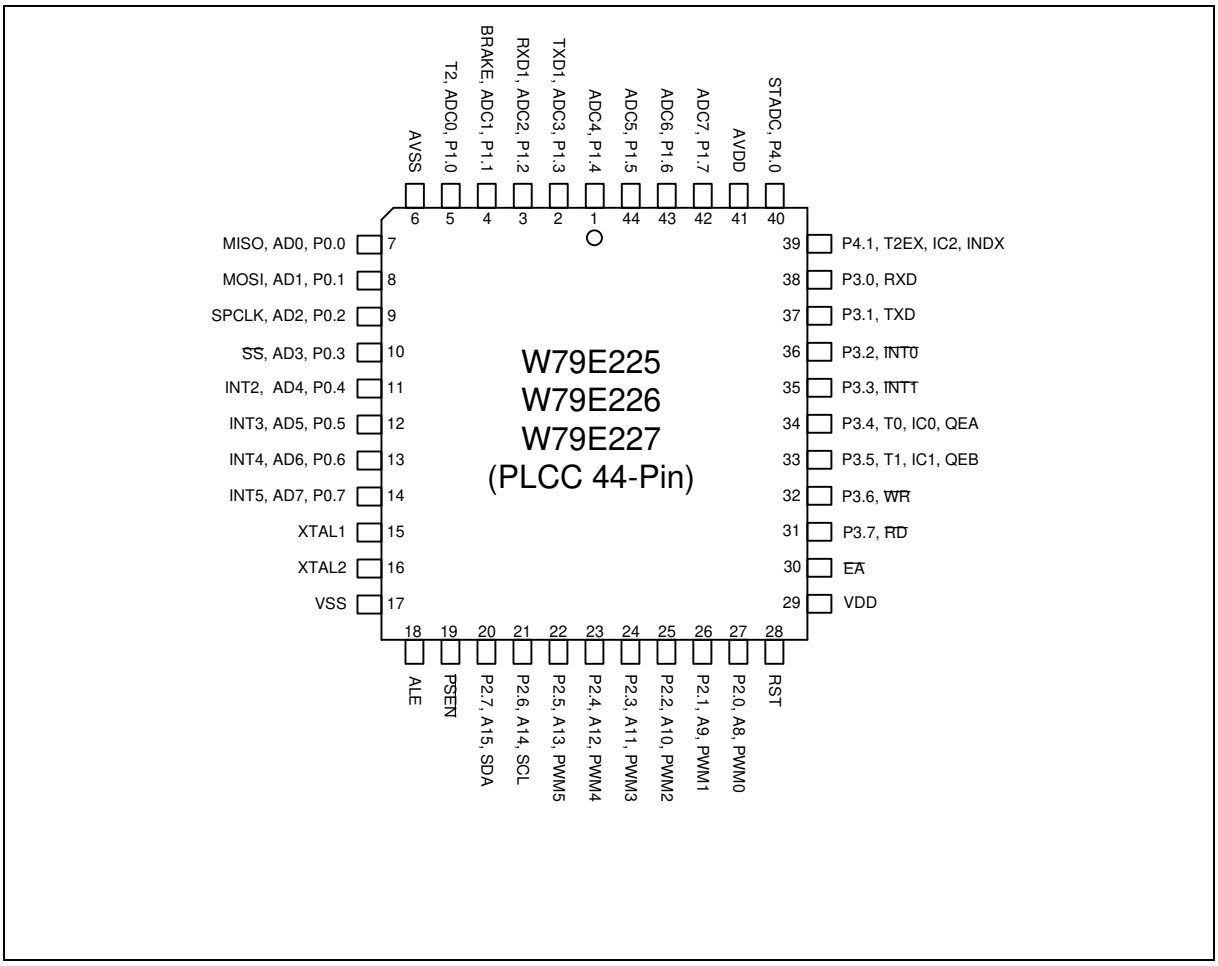
3.1 Lead Free (RoHS) Parts information list

PART NO.	EPROM FLASH SIZE	RAM	OPERATING FREQUENCY	OPERATING VOLTAGE	NVM FLASH EPROM	PACKAGE	REMARK
W79E225APG	16KB	256B + 1KB	up to 40MHz up to 20MHz	4.5V ~ 5.5V 2.7V[1] ~ 5.5V	1KB	PLCC-44 Pin	Internal memory
			up to 24MHz	4.5V ~ 5.5V			External memory
W79E225ALG	16KB	256B+ 1KB	up to 40MHz up to 20MHz	4.5V ~ 5.5V 2.7V[1] ~ 5.5V	1KB	LQFP-48 Pin	Internal memory
			up to 24MHz	4.5V ~ 5.5V			External memory
W79E226APG	32KB	256B + 2KB	up to 40MHz up to 20MHz	4.5V ~ 5.5V 2.7V[1] ~ 5.5V	2KB	PLCC-44 Pin	Internal memory
			up to 24MHz	4.5V ~ 5.5V			External memory
W79E226ALG	32KB	256B + 2KB	up to 40MHz up to 20MHz	4.5V ~ 5.5V 2.7V[1] ~ 5.5V	2KB	LQFP-48 Pin	Internal memory
			up to 24MHz	4.5V ~ 5.5V			External memory
W79E227APG	64KB	256B + 2KB	up to 40MHz up to 20MHz	4.5V ~ 5.5V 2.7V[1] ~ 5.5V	2KB	PLCC-44 Pin	Internal memory
			up to 24MHz	4.5V ~ 5.5V			External memory
W79E227ALG	64KB	256B + 2KB	up to 40MHz up to 20MHz	4.5V ~ 5.5V 2.7V[1] ~ 5.5V	2KB	LQFP-48 Pin	Internal memory
			up to 24MHz	4.5V ~ 5.5V			External memory

Note: 1. Minimum of 3.0V operating voltage for NVM program and erase operations.

4. PIN CONFIGURATION




W79E225
W79E226
W79E227
(PLCC 44-Pin)
AVSS 6
T2, ADC0, P1.0 5
BRAKE, ADC1, P1.1 4
RXD1, ADC2, P1.2 3
TXD1, ADC3, P1.3 2
ADC4, P1.4 1
ADC5, P1.5 44
ADC6, P1.6 43
ADC7, P1.7 42
AVDD 41
STADC, P4.0 40
MISO, AD0, P0.0 7
MOSI, AD1, P0.1 8
SPCLK, AD2, P0.2 9
SS, AD3, P0.3 10
INT2, AD4, P0.4 11
INT3, AD5, P0.5 12
INT4, AD6, P0.6 13
INT5, AD7, P0.7 14
XTAL1 15
XTAL2 16
VSS 17
39 P4.1, T2EX, IC2, INDX
38 P3.0, RXD
37 P3.1, TXD
36 P3.2, INT0
35 P3.3, INT1
34 P3.4, T0, IC0, QEA
33 P3.5, T1, IC1, QEB
32 P3.6, WR
31 P3.7, RD
30 EA
29 VDD
18 ALE
19 PSEN
20 P2.7, A15, SDA
21 P2.6, A14, SCL
22 P2.5, A13, PWM5
23 P2.4, A12, PWM4
24 P2.3, A11, PWM3
25 P2.2, A10, PWM2
26 P2.1, A9, PWM1
27 P2.0, A8, PWM0
28 RST

5. PIN DESCRIPTION

SYMBOL	TYPE	INITIAL STATE	DESCRIPTIONS
$\overline{EA}$	I	-	**EXTERNAL ACCESS ENABLE:** This pin forces the processor to execute from external ROM. The ROM address and data are not presented on the bus if the $\overline{EA}$ pin is high. **Note:** This pin has no internal pull-up or pull-down. The pin needs externally pull-up to execute from internal APROM. For executing from external APROM, the pin needs externally pull-down. The pin state is internally latched during all reset. User needs to take note that changes to /EA pin state after reset will not be effective.
$\overline{PSEN}$	O H	High	**PROGRAM STORE ENABLE:** $\overline{PSEN}$ enables the external ROM data in the Port 0 address/data bus. When internal ROM access is performed, $\overline{PSEN}$ strobe signal will not be output from this pin.
ALE	O H	High	**ADDRESS LATCH ENABLE:** ALE enables the address latch that separates the address from the data on Port 0.
RST	I L	-	**RESET:** Set this pin high for two machine cycles while the oscillator is running to reset the device.
XTAL1	I	-	**CRYSTAL 1:** Crystal oscillator input or external clock input.
XTAL2	O	-	**CRYSTAL 2:** Crystal oscillator output.
V_{SS}	I	-	**GROUND**: Ground potential.
V_{DD}	I	-	**POWER SUPPLY:** Supply voltage for operation.
AVDD	I	-	Analog power supply.
AVSS	I	-	Analog ground potential.
P0.0–P0.7	I/O D S H	High-Z	**PORT 0**: Port 0 is an open-drain bi-directional I/O port. This port also provides a multiplexed low byte address/data bus during accesses to external memory. There is an embedded weakly pull-up resistor on each port 0 pin which can be enabled or disabled by setting or clearing of PUP0, bit0 in A2h. The ports have alternate functions which are described below: P0.0, AD0, MISO P0.1, AD1, MOSI P0.2, AD2, SPCLK P0.3, AD3, /SS P0.4, AD4, INT2 P0.5, AD5, INT3 P0.6, AD6, INT4 P0.7, AD7, INT5

PIN DESCRIPTION, continued

SYMBOL	TYPE	INITIAL STATE	DESCRIPTIONS
P1.0–P1.7	I/O S H	High	**PORT 1**: 8-bit, bi-directional I/O port with internal pull-ups. The ports have alternate functions which are described below: P1.0, ADC0, T2 P1.1, ADC1, BRAKE P1.2, ADC2, RXD1 P1.3, ADC3, TXD1 P1.4, ADC4 P1.5, ADC5 P1.6, ADC6 P1.7, ADC7
P2.0-P2.5	I/O S	Tri-state	**PORT 2**: 8-bit, bi-directional I/O port. This port also provides the upper address bits for accesses to external memory. P2.6 to P2.7 can be software configured as I2C serial ports. P2.0 to P2.5 also provides PWM0 to PWM5 outputs. P2.0, A8, PWM0 P2.1, A9, PWM1 P2.2, A10, PWM2 P2.3, A11, PWM3 P2.4, A12, PWM4 P2.5, A13, PWM5 P2.6, A14, SCL P2.7, A15, SDA **Note:** P2.6 and P2.7 are permanent open drain pins. When access to external memory beyond 16K region, user requires to add external pull-up registers (up to 2Kohm) on these pins. This will result in slight increase in current consumption.
P2.6-P2.7	I/O D S	High-Z	
P3.0-P3.7	I/O S H	High	**PORT 3**: 8-bit, bi-directional I/O port with internal pull-ups. The ports have alternate functions which are described below: P3.0, RXD P3.1, TXD P3.2, /INT0 P3.3, /INT1 P3.4, T0, IC0, QEA P3.5, T1, IC1, QEB P3.6, /WR P3.7, /RD

PIN DESCRIPTION, continued

SYMBOL	TYPE	INITIAL STATE	DESCRIPTIONS
P4.0-P4.3	I/O S H	High	**PORT 4**: 4-bit multipurpose programmable I/O port with alternate functions. The Port 4 has four different operation modes. P4.0, STADC P4.1, T2EX, IC2 P4.2 P4.3 **Note:** P4.2 & P4.3 are not supported in PLCC44 pins package.
P5.0-P5.1	I/O S	Tri-state	**PORT 5**: 2-bit, bit-directional I/O port. This port is not bit addressable. The alternate functions are described below: P5.0, PWM6 P5.1, PWM7 **Note:** P5.0 & P5.1 are not supported in PLCC44 pins package.

Note ：TYPE I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain S: Schmitt Trigger

5.1 Port 4

Port 4, SFR P4 at address A5H, is a 4-bit multipurpose programmable I/O port which functions are I/O and chip-select function. It has four different operation modes:

- Mode 0 - P4.0 ~ P4.3 is 4-bit bi-directional I/O port which is the same as port 1. The default Port 4 is a general I/O function.
- Mode1 - P4.0 ~ P4.3 are read data strobe signals which are synchronized with $\overline{RD}$ signal at specified addresses. These read data strobe signals can be used as chip-select signals for external peripherals.
- Mode2 - P4.0 ~ P4.3 are write data strobe signals which are synchronized with $\overline{WR}$ signal at specified addresses. These write data strobe signals can be used as chip-select signals for external peripherals.
- Mode3 - P4.0 ~ P4.3 are read/write data strobe signals which are synchronized with $\overline{RD}$ or $\overline{WR}$ signal at specified addresses. These read/write data strobe signals can be used as chip-select signals for external peripherals.

When Port 4 is configured with the feature of chip-select signals, the chip-select signal address range depends on the contents of the SFR P4xAH, P4xAL, P4CONA and P4CONB. P4xAH and P4xAL contain the 16-bit base address of P4.x. P4CONA and P4CONB contain the control bits to configure the Port 4 operation mode.

6. MEMORY ORGANIZATION

The W79E22X SERIES separates the memory into two sections; Program Memory and Data Memory. Program Memory stores instruction op-codes, while Data Memory stores data or memory-mapped devices.

6.1 Program Memory (on-chip Flash)

W79E22X SERIES includes one 16/32/64K bytes of main FLASH EPROM for application program (AP FLASH EPROM) and one 4K bytes of FLASH EPROM for loader program (LD FLASH EPROM) to operate the in-system programming (ISP) feature, and one 1/2/2K bytes of NVM Flash EPROM for data storage. The 16/32/64K bytes Flash EPROM is AP0 bank. The default active bank is AP0.

In normal operation, the microcontroller will execute the code from main FLASH EPROM. By setting program registers, user can force the microcontroller to switch to programming mode which will cause it to execute the code (loader program) from the 4K bytes of auxiliary LD FLASH EPROM to update the contents of the 16/32/64K bytes of main FLASH EPROM. After reset, the microcontroller will executes the new application program in the main FLASH EPROM. This ISP feature makes the job easy and efficient in which the application needs to update firmware frequently without opening the chassis.

6.2 Data Memory

W79E22X SERIES can access up to 64Kbytes of external Data Memory. This memory region is accessed by the MOVX instructions. Unlike the 8051 derivatives, W79E22X SERIES contains on-chip 1/2/2 Kbytes of Data Memory, which only can be accessed by MOVX instructions. These 1/2/2 Kbytes of SRAM is between address 0000h and 03FFH/07FFH. Access to the on-chip Data Memory is optional under software control. When enabled by DMEO bit of PMR register, a MOVX instruction that uses this area will go to the on-chip RAM. If MOVX instruction accesses the addresses greater than 03FFH/07FFH CPU will automatically access external memory through Port 0 and 2. When disabled, the 1/2/2 KB memory area is transparent to the system memory map. Any MOVX directed to the space between 0000h and FFFFH goes to the expanded bus on the Port 0 and 2. This is the default condition. In addition, the device has the standard 256 bytes of on-chip RAM. This can be accessed either by direct addressing or by indirect addressing. There are also some Special Function Registers (SFRs), which can only be accessed by direct addressing.

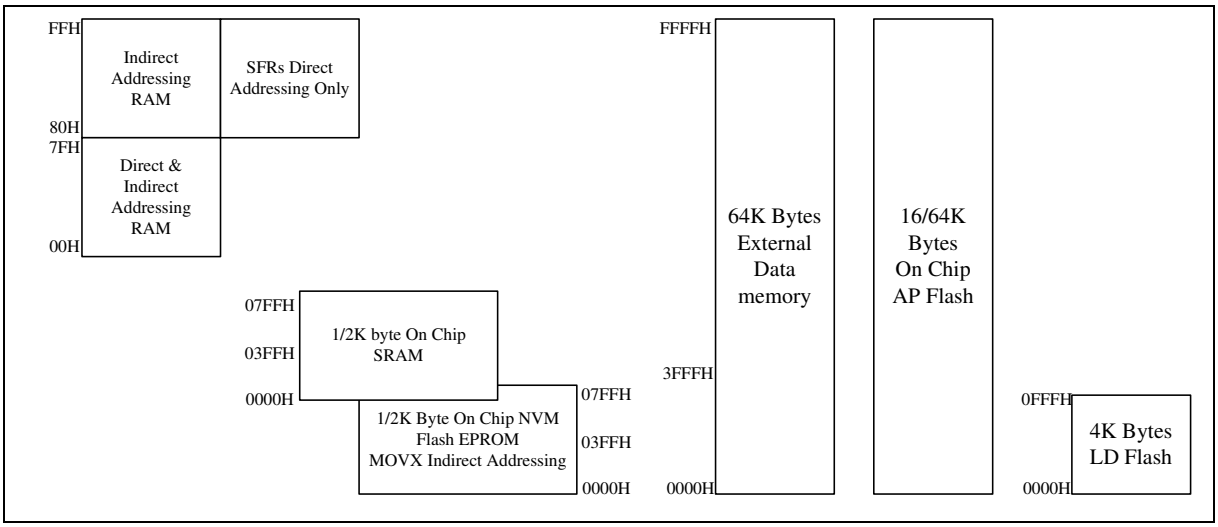


Figure 6-1: W79E22X SERIESA Memory Map

6.3 Auxiliary SRAM

W79E22X SERIES has a 1/2/2 KB of data space SRAM which is read/write accessible and is memory mapped. This on-chip SRAM is accessed by the MOVX instruction. There is no conflict or overlap among the 256 bytes scratch-pad memory and the 1/2/2 KB auxiliary sram as they use different addressing modes and instructions. Access to the on-chip Data Memory is optional under software control. Set DMEO bit of PMR SFR to 1 will enable the on-chip 1/2/2 KB MOVX SRAM and at the same time EnNVM bit must be cleared as NVM Data uses the same instruction of MOVX. Refer to.

6.4 NVM Data Flash

W79E22X SERIES 1/2/2-KB NVM Data block shown in the diagram on Figure 6-1 shares the same address as AUX-RAM address.

Due to overlapping of AUX-RAM, NVM data memory and external data memory physical address, the following table is defined. EnNVM bit (NVMCON.5) will enable read access to NVM data flash area. DME0 (PMR.0) will enable read access to AUX-RAM.

ENNVM	DME0	DATA MEMORY AREA
0	0	Enable External RAM read/write access by MOVX
0	1	Enable AUX-RAM read/write access by MOVX
1	X	Enable NVM data Memory read access by MOVX only. If EER or EWR is set and NVM flash erase or write control is busy, to set this bit read NVM data is invalid.

Table 6-1: Bits setting for MOVX access to Data Memory Area

INSTRUCTIONS		ENNVM = 1 NVM SIZE = SRAM (1K)	
		ADDR ≤ 1K	ADDR > 1K
Read access	MOVX A, @DPTR (Read)	NVM[1]	Ext memory[1]
	MOVX A, @R0 (Read)	NVM[2]	NOP
	MOVX A, @R1 (Read)	NVM[2]	NOP
Write access	MOVX @DPTR, A (Write)	NOP	Ext memory[1]
	MOVX @R0, A (Write)	NOP	NOP
	MOVX @R1, A (Write)	NOP	NOP

Table 6-2: W79E225 MOVX read/write access destination

INSTRUCTIONS		ENNVM = 1 NVM SIZE = SRAM (2K)	
		ADDR ≤ 2K	ADDR > 2K
Read access	MOVX A, @DPTR (Read)	NVM[1]	Ext memory[1]
	MOVX A, @R0 (Read)	NVM[2]	NOP
	MOVX A, @R1 (Read)	NVM[2]	NOP
Write access	MOVX @DPTR, A (Write)	NOP	Ext memory[1]
	MOVX @R0, A (Write)	NOP	NOP
	MOVX @R1, A (Write)	NOP	NOP

Table 6-3: W79E226/227 MOVX read/write access destination

Note:

1. A15~A0=DPTR
2. A15~A8=XRAMAH

It is partition into 16/32/32 pages area and each page has 64 bytes data as below figure. The page 0 is from 0000h ~ 003Fh, page 1 is from 0040h ~ 007Fh until page 31 address located at 07COh ~ 07FFh.

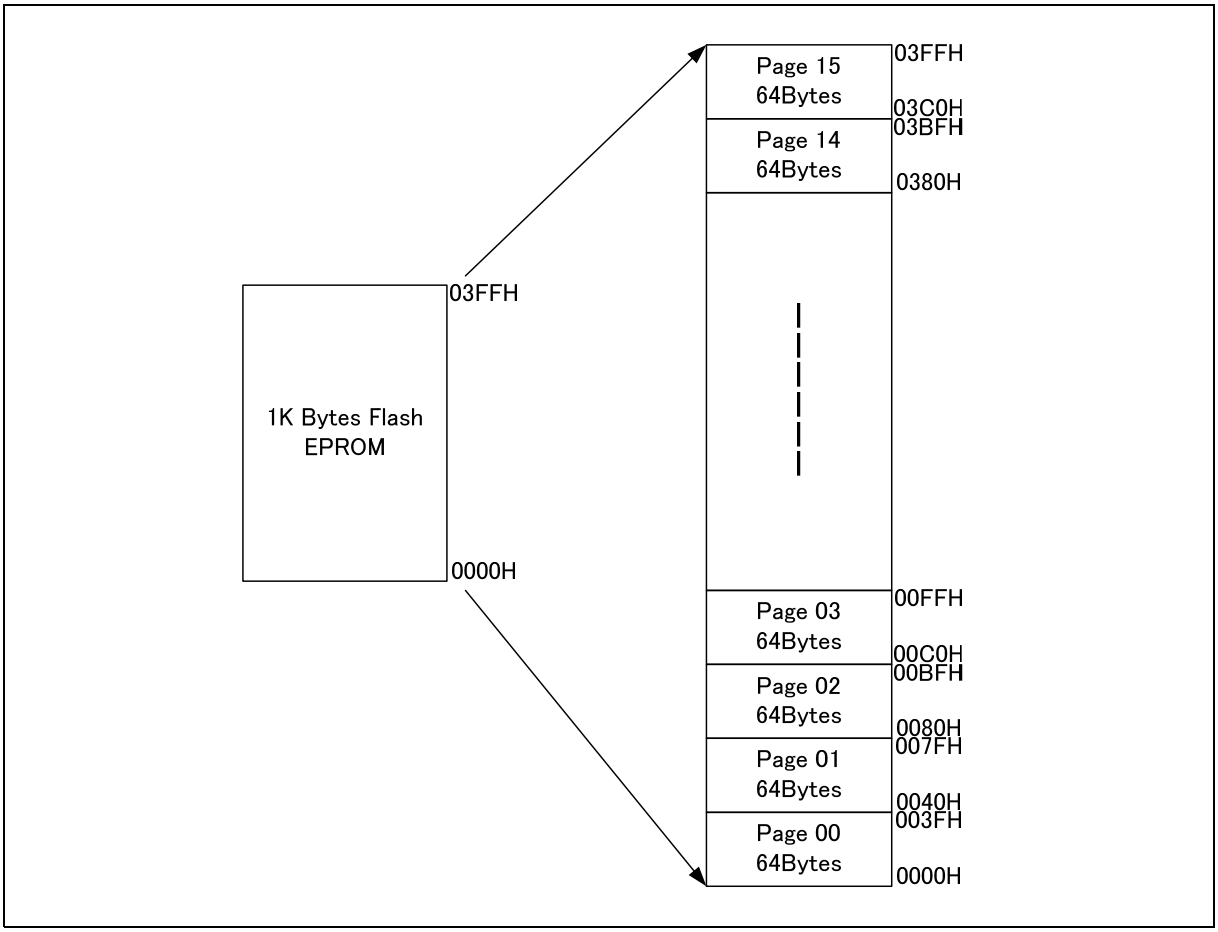


Figure 6-2: W79E225 NVM Data Mapping

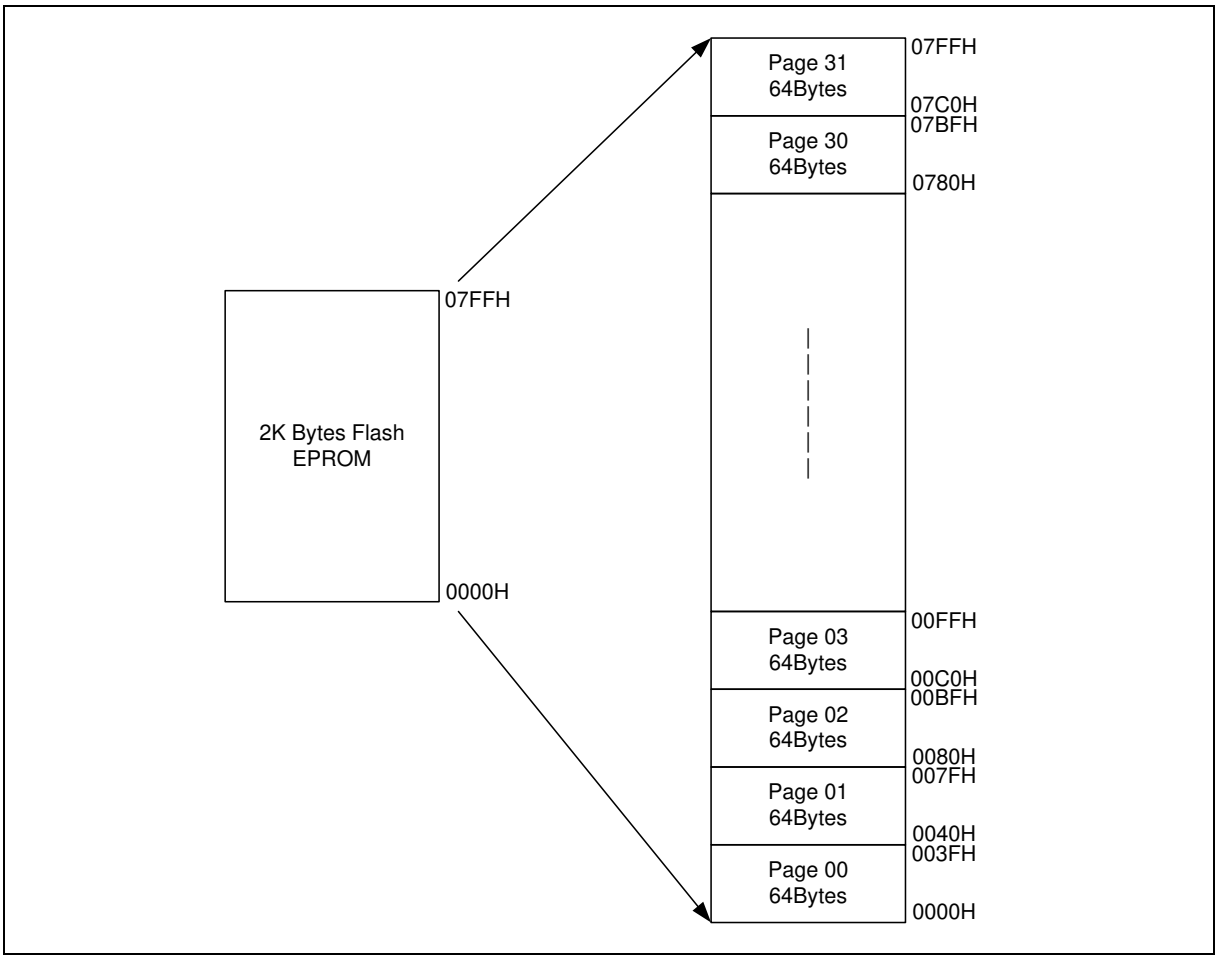


Figure 6-3: W79E226/227 NVM Data Mapping

PAGE	START ADDRESS	END ADDRESS	PAGE	START ADDRESS	END ADDRESS
0	0000h	003Fh	16	0400h	043Fh
1	0040h	007Fh	17	0440h	047Fh
2	0080h	00BFh	18	0480h	04BFh
3	00C0h	00FFh	19	04C0h	04FFh
4	0100h	013Fh	20	0500h	053Fh
5	0140h	017Fh	21	0540h	057Fh
6	0180h	01BFh	22	0580h	05BFh
7	01C0h	01FFh	23	05C0h	05FFh
8	0200h	023Fh	24	0600h	063Fh
9	0240h	027Fh	25	0640h	067Fh
10	0280h	02BFh	26	0680h	06BFh
11	02C0h	02FFh	27	06C0h	06FFh
12	0300h	033Fh	28	0700h	073Fh
13	0340h	037Fh	29	0740h	077Fh
14	0380h	03BFh	30	0780h	07BFh
15	03C0h	03FFh	31	07C0h	07FFh

[**Note**: Page 16-31 is for W79E226/227 only]

Table 6-4: W79E22X SERIES NVM page (n) area definition table

It has a dedicated On-Chip RC Oscillator that is fixed at 6MHz +/- 50% frequency to support clock source for the 1/2/2K NVM data Flash. The on chip oscillator is enabled only during program or erase operation, through EWR or EER in NVMCON SFR. EWR or EER bits are cleared by hardware after program or erase operation completed. The program/erase time is automatically controlled by hardware.

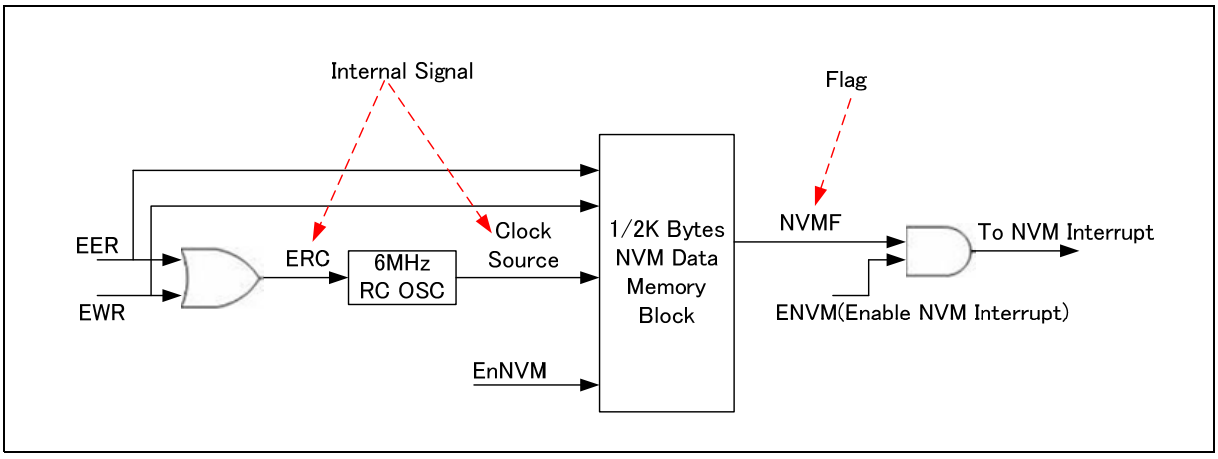


Figure 6-4: NVM control

6.4.1 Operation

User is required to enable EnNVM (NVMCON.5) bit for all NVM access (read/write/erase).

Before write data to NVM Data, the page must be erased. A page is erased by setting page address which address will decode and enable page (n) on NVMADDRH and NVMADDRL, then set EER (NVMCON.7) and EnNVM (NVMCON.5). The device will then automatic execute page erase. When completed, NVMF will be set by hardware. NVMF should be cleared by software. Interrupt request will be generated if ENVM (EIE1.5) is enabled. EER bit will be cleared by hardware when erase is completed. The total erase time is about 5ms.

For write, user must set address and data to NVMADDRH/L and NVMDAT, respectively. And then set EWR (NVMCON.6) and EnNVM (NVMCON.5) to enable data write. When completed, the device will set NVMF flag. NVMF flag should be cleared by software. Similarly, interrupt request will be generated if ENVM (EIE1.5) is enabled. The program time is about 50us.

The following shows some examples of NVM operations (using W79E226/227):

Read NVM data is by MOVX A,@DPTR/R0/R1 instruction:

A read exceed 2k will read the external address

Example1: DPTR=0x07FF, R0/R1 = 0xFF, XRAMAH=0x07, EnNVM=1

MOVX A,@DPTR → read NVM data at address 0x07FF

MOVX A,@R0 → read NVM data at address 0x07FF

MOVX A,@R1 → read NVM data at address 0x07FF

Example2: DPTR = 0x2000, EnNVM=1, DME0=0

MOVX A,@DPTR → read external RAM data at address 0x2000,

Erase NVM by SFR register:

Example1: NVMADDRH = 0x07, NVMADDRL = 0xF0, page 31 will be enabled. After set EER, the page 31 will be erased.

Example2: NVMADDRH = 0x10, NVMADDRL = 0x00, invalid NVM erase instruction (address exceed NVM boundary).

Write NVM by SFR register:

Example1: NVMADDRH = 0x07, NVMADDRL = 0xF0

After set EWR, data will be written to the NVM address = 0x07F0 location.

Example2: NVMADDRH = 0x10, NVMADDRL = 0x00, after set EWR, invalid NVM write instruction (address exceed NVM boundary).

During erase, write is invalid. Likewise, during write, erase is invalid. An erase or write is invalid if NVMF is not clear by software. A write to NVMADDRH and NVMADDRL is invalid during Erase or Write, and a write to NVMDAT is invalid only during NVM write access.

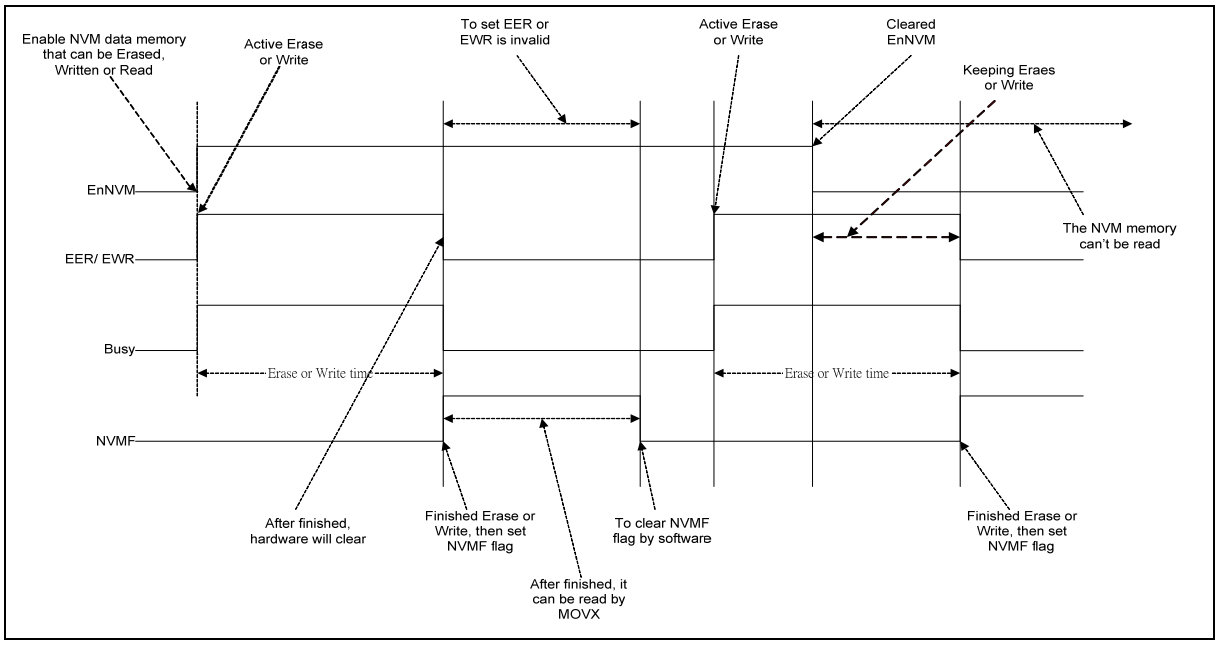


Figure 6-5: NVM data memory control timing

For security purposes, this NVM data flash provides an independent “Lock bit” located in Security bits. It is used to protect the customer’s 1/2/2K bytes of data code. It may be enabled after the external programmer finishes the programming and verifying sequence. Once this bit is set to logic 0, the 1/2/2K bytes of NVM Flash EPROM data can not be accessed again by external device.

Note: 1. NVMF can be polled or by h/w interrupt to indicate NVM data memory erase or write operation has completed.

2. While user program is erasing or writing to NVM data memory, the PC counter will continue to fetch for next instruction.

3. When uC is in idle mode and if NVM interrupt and global interrupt are enabled, the completion of either erasing or programming the NVM data memory will exit the idle condition.

7. SPECIAL FUNCTION REGISTERS

The W79E22X SERIES uses Special Function Registers (SFR) to control and monitor peripherals. The SFR reside in register locations 80-FFh and are only accessed by direct addressing. The W79E22X SERIES contains all the SFR present in the standard 8051/52, as well as some additional SFR, and, in some cases, unused bits in the standard 8051/52 have new functions. SFR whose addresses end in 0 or 8 (hex) are bit-addressable. The following table of SFR is condensed, with eight locations per row. Empty locations indicate that there are no registers at these addresses.

F8	EIP	EIE1	EIP1	CCL0 /PCNTL	CCH0 /PCNTH	CCL1 /PLSCNTL	CCH1 /PLSCNTH	INTCTRL
F0	B			SPCR	SPSR	SPDR	I2CSADEN	EIPH
E8	EIE	I2CON	I2ADDR	NVMADDRH	I2DAT	I2STATUS	I2CLK	I2TIMER
E0	ACC	ADCCON	ADCH	ADCL		PDTC1	PDTC0	PWMCON4
D8	WDCON	PWMPL	PWM0L	NVMADDRL	PWMCON1	PWM2L	PWM6L	PWMCON3
D0	PSW	PWMPH	PWM0H	NVMDAT	QEICON	PWM2H	PWM6H	WDCON2
C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	PWMCON2	PWM4L
C0	SCON1	SBUF1	T3MOD	T3CON	PMR	FSPLT	ADCPS	TA
B8	IP	SADEN	SADEN1	POVM	POVD	PIO	PWMEN	PWM4H
B0	P3	P5			RCAP3L	RCAP3H	EIP1H	IPH
A8	IE	SADDR	SADDR1		SFRAL	SFRAH	SFRFD	SFRCN
A0	P2	XRAMAH	P4CSIN	CAPCON0	CAPCON1	P4	CCL2 /MAXCNTL	CCH2 /MAXCNTH
98	SCON	SBUF	P42AL	P42AH	P43AL	P43AH	NVMCON	CHPCON
90	P1	EXIF	P4CONA	P4CONB	P40AL	P40AH	P41AL	P41AH
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	CKCON1
80	P0	SP	DPL	DPH	TL3	TH3		PCON

Table 7-1: Special Function Register Location Table

SYMBOL	DEFINITION	ADDRESS	MSB BIT_ADDRESS, LSB							SYMBOL	RESET
INTCTRL	INTERRUPT CONTROL REGISTER	FFH	-	-	INT5CT1	INT5CT0	INT4CT1	INT4CT0	INT3CT1	INT3CT0	xx00 0000B
CCH1 /PLSCNTH	CAPTURE COUNTER HIGH 1 REGISTER	FEH	CCH1.7 /PLSCNTH.7	CCH1.6 /PLSCNTH.6	CCH1.5 /PLSCNTH.5	CCH1.4 /PLSCNTH.4	CCH1.3 /PLSCNTH.3	CCH1.2 /PLSCNTH.2	CCH1.1 /PLSCNTH.1	CCH1.0 /PLSCNTH.0	0000 0000B
CCL1 /PLSCNTL	CAPTURE COUNTER LOW 1 REGISTER	FDH	CCL1.7 /PLSCNTL.7	CCL1.6 /PLSCNTL.6	CCL1.5 /PLSCNTL.5	CCL1.4 /PLSCNTL.4	CCL1.3 /PLSCNTL.3	CCL1.2 /PLSCNTL.2	CCL1.1 /PLSCNTL.1	CCL1.0 /PLSCNTL.0	0000 0000B
CCH0 /PCNTH	CAPTURE COUNTER HIGH 0 REGISTER	FCH	CCH0.7 /PCNTH.7	CCH0.6 /PCNTH.6	CCH0.5 /PCNTH.5	CCH0.4 /PCNTH.4	CCH0.3 /PCNTH.3	CCH0.2 /PCNTH.2	CCH0.1 /PCNTH.1	CCH0.0 /PCNTH.0	0000 0000B
CCL0 /PCNTL	CAPTURE COUNTER LOW 0 REGISTER	FBH	CCL0.7 /PCNTL.7	CCL0.6 /PCNTL.6	CCL0.5 /PCNTL.5	CCL0.4 /PCNTL.4	CCL0.3 /PCNTL.3	CCL0.2 /PCNTL.2	CCL0.1 /PCNTL.1	CCL0.0 /PCNTL.0	0000 0000B
EIP1	EXTENDED INTERRUPT PRIORITY 1	FAH	-	-	PNVMI	PCPTF	PT3	PBKF	PPWMF	PSPI	xx00 0000B
EIE1	INTERRUPT ENABLE 1	F9H	-	-	ENVM	ECPTF	ET3	EBK	EPWM	ESPI	xx00 0000B
EIP	EXTENDED INTERRUPT PRIORITY	F8H	(FF) PS1	(FE) PX5	(FD) PX4	(FC) PWDI	(FB) PX3	(FA) PX2	(F9) -	(F8) PI2C	0000 00x0B
EIPH	EXTENDED INTERRUPT HIGH PRIORITY	F7H	PS1H	PX5H	PX4H	PWDIH	PX3H	PX2H	-	PI2CH	0000 00x0B
I2CSADEN	I2C SLAVE ADDRESS MASK	F6H	I2CSADEN.7	I2CSADEN.6	I2CSADEN.5	I2CSADEN.4	I2CSADEN.3	I2CSADEN.2	I2CSADEN.1	I2CSADEN.0	1111 1110B
SPDR	SERIAL PERIPHERAL DATA REGISTER	F5H	SPD.7	SPD.6	SPD.5	SPD.4	SPD.3	SPD.2	SPD.1	SPD.0	xxxx xxxxB
SPSR	SERIAL PERIPHERAL STATUS REGISTER	F4H	SPIF	WCOL	SPIOVF	MODF	DRSS	-	-	-	0000 0xxxB
SPCR	SERIAL PERIPHERAL CONTROL REGISTER	F3H	SSOE	SPE	LSBFE	MSTR	CPOL	CPHA	SPR1	SPR0	0000 0100B
B	B REGISTER	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	0000 0000B
I2TIMER	I2C TIMER COUNTER REGISTER	EFH	-	-	-	-	-	ENTI	DIV4	TIF	xxxx x000B
I2CLK	I2C CLOCK RATE	EEH	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0	0000 0000B
I2STATUS	I2C STATUS REGISTER	EDH									1111 1000B
I2DAT	I2C DATA	ECH	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0	0000 0000B
NVMADDRH	NVM HIGH BYTE ADDRESS	EBH	-	-	-	-	-	NVMADDRH.10	NVMADDRH.9	NVMADDRH.8	xxxx x000B
I2ADDR	I2C SLAVE ADDRESS	EAH	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	GC	0000 0000B
I2CON	I2C CONTROL REGISTER	E9H	-	ENS	STA	STO	SI	AA	I2CIN	-	X000 000xB
EIE	EXTENDED INTERRUPT ENABLE	E8H	(EF) ES1	(EE) EX5	(ED) EX4	(EC) EWDI	(EB) EX3	(EA) EX2	(E9)	(E8) EI2C	0000 00x0B
PWMCON4	PWM CONTROL REGISTER 4	E7H	PWMEOM	PWMOOM	PWM6OM	PWM7OM	-	-	-	BKF	0000 xxx0B
PDTC0	DEAD TIME CONTROL REGISTER 0	E6H	PDTC0.7	PDTC0.6	PDTC0.5	PDTC0.4	PDTC0.3	PDTC0.2	PDTC0.1	PDTC0.0	0000 0000B
PDTC1	DEAD TIME CONTROL REGISTER 1	E5H	PDTC1.7	PDTC1.6	PDTC1.5	PDTC1.4	PDTC1.3	PDTC1.2	PDTC1.1	PDTC1.0	0000 0000B
ADCL	ADC CONVERTER RESULT LOW BYTE	E3H	ADCLK1	ADCLK0	-	-	-	-	ADC.1	ADC.0	00xx xxxxB

Continued

SYMBOL	DEFINITION	ADDRESS	MSB BIT_ADDRESS, LSB SYMBOL								RESET
ADCH	ADC CONVERTER RESULT HIGH BYTE	E2H	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2	xxxx xxxxB
ADCCON	ADC CONTROL REGISTER	E1H	ADCEN	-	ADCEX	ADCI	ADCS	AADR2	AADR1	AADR0	0x00 0000B
ACC	ACCUMULATOR	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	0000 0000B
PWMCON3	PWM CONTROL REGISTER 3	DFH	PWM7B	PWM6B	PWM5B	PWM4B	PWM3B	PWM2B	PWM1B	PWM0B	0000 0000B
PWM6L	PWM 6 LOW BITS REGISTER	DEH	PWM6.7	PWM6.6	PWM6.5	PWM6.4	PWM6.3	PWM6.2	PWM6.1	PWM6.0	0000 0000B
PWM2L	PWM 2 LOW BITS REGISTER	DDH	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0	0000 0000B
PWMCON1	PWM CONTROL REGISTER 1	DCH	PWMRUN	Load	PWMF	CLRPWM	PWM6I	PWM4I	PWM2I	PWM0I	0000 0000B
NVMADDRL	NVM LOW BYTE ADDRESS	DBH	NVMADDRH.7	NVMADDRH.6	NVMADDRH.5	NVMADDRH.4	NVMADDRH.3	NVMADDRH.2	NVMADDRH.1	NVMADDRH.8	0000 0000B
PWM0L	PWM 0 LOW BITS REGISTER	DAH	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0	0000 0000B
PWMPL	PWM COUNTER LOW REGISTER	D9H	PWMP.7	PWMP.6	PWMP.5	PWMP.4	PWMP.3	PWMP.2	PWMP.1	PWMP.0	0000 0000B
WDCON	WATCH-DOG CONTROL	D8H	(DF) -	(DE) POR	(DD) -	(DC) -	(DB) WDIF	(DA) WTRF	(D9) EWT	(D8) RWT	0100 0000B
WDCON2	WATCH-DOG CONTROL2	D7H	-	-	-	-	-	-	-	STRLD	0000 0000B
PWM6H	PWM 6 HIGH BITS REGISTER	D6H	-	-	-	-	PWM6.11	PWM6.10	PWM6.9	PWM6.8	xxxx 0000B
PWM2H	PWM 2 HIGH BITS REGISTER	D5H	-	-	-	-	PWM2.11	PWM2.10	PWM2.9	PWM2.8	xxxx 0000B
QEICON	QEI CONTROL REGISTER	D4H	-	-	-	DISIDX	DIR	QEIM1	QEIM0	QEIEN	xxx0 0000B
NVMDAT	NVM DATA	D3H	NVMDAT.7	NVMDAT.6	NVMDAT.5	NVMDAT.4	NVMDAT.3	NVMDAT.2	NVMDAT.1	NVMDAT.0	0000 0000B
PWM0H	PWM 0 HIGH BITS REGISTER	D2H	-	-	-	-	PWM0.11	PWM0.10	PWM0.9	PWM0.8	xxxx 0000B
PWMPH	PWM COUNTER HIGH REGISTER	D1H	-	-	-	-	PWMP.11	PWMP.10	PWMP.9	PWMP.8	xxxx 0000B
PSW	PROGRAM STATUS WORD	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P	0000 0000B
PWM4L	PWM 4 LOW BITS REGISTER	CFH	PWM4.7	PWM4.6	PWM4.5	PWM4.4	PWM4.3	PWM4.2	PWM4.1	PWM4.0	0000 0000B
PWMCON2	PWM CONTROL REGISTER 2	CEH	BKCH	BKPS	BPEN	BKEN	FP1	FP0	PMOD1	PMOD0	0000 0000B
TH2	T2 REG. HIGH	CDH	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0	0000 0000B
TL2	T2 REG. LOW	CCH	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0	0000 0000B
RCAP2H	T2 CAPTURE LOW	CBH	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0	0000 0000B
RCAP2L	T2 CAPTURE HIGH	CAH	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0	0000 0000B
T2MOD	TIMER 2 MODE	C9H	HC5	HC4	HC3	HC2	T2CR	-	-	DCEN	0000 0xx0B
T2CON	TIMER 2 CONTROL	C8H	(CF) TF2	(CE) EXF2	(CD) RCLK	(CC) TCLK	(CB) EXEN2	(CA) TR2	(C9) $C/\overline{T}$	(C8) $CP/\overline{RL2}$	0000 0000B
TA	TIME ACCESS REGISTER	C7H	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0	0000 0000B
DDIO	DISABLE DIGITAL I/O	C6H	DDIO.7	DDIO.6	DDIO.5	DDIO.4	DDIO.3	DDIO.2	DDIO.1	DDIO.0	0000 0000B

Continued

SYMBOL	DEFINITION	ADDRESS	MSB BIT_ADDRESS, LSB SYMBOL								RESET
FSPLT	FAULT SAMPLING TIME REGISTER	C5H	SCMP1	SCMP0	SFP1	SFP0	SFCEN	SFCST	SFCDIR	LSBD	0000 0000B
PMR	POWER MANAGEMENT REGISTER	C4H	-	-	-	-	-	ALEOFF	-	DME0	xxxx x0x0B
T3CON	TIMER 3 CONTROL	C3H	TF3	-	-	-	-	TR3	-	CMP/$\overline{RL3}$	0xxx x0x0B
T3MOD	TIMER 3 MODE CONTROL	C2H	ENLD	ICEN2	ICEN1	ICEN0	T3CR	-	-	-	0000 0xxxB
SBUF1	SERIAL BUFFER 1	C1H	SBUF1.7	SBUF1.6	SBUF1.5	SBUF1.4	SBUF1.3	SBUF1.2	SBUF1.1	SBUF1.0	xxxx xxxxB
SCON1	SERIAL CONTROL 1	C0H	(BF) SM0_1/FE_1	(BE) SM1_1	(BD) SM2_1	(BC) REN_1	(BB) TB8_1	(BA) RB8_1	(B9) TI_1	(B8) RI_1	0000 0000B
PWM4H	PWM 4 HIGH BITS REGISTER	BFH	-	-	-	-	PWM4.11	PWM4.10	PWM4.9	PWM4.8	xxxx 0000B
PWMEN	PWM OUTPUT ENABLE REGISTER	BEH	PWM7EN	PWM6EN	PWM5EN	PWM4EN	PWM3EN	PWM2EN	PWM1EN	PWM0EN	0000 0000B
PIO	PWM PIN OUTPUT SOURCE SELECT	BDH	PIO7	PIO6	PIO5	PIO4	PIO3	PIO2	PIO1	PIO0	0000 0000B
POVD	PWM OUTPUT STATE REGISTERS	BCH	POVD.7	POVD.6	POVD.5	POVD.4	POVD.3	POVD.2	POVD.1	POVD.0	0000 0000B
POVM	PWM OUTPUT OVERRIDE CONTROL REGISTERS	BBH	POVM.7	POVM.6	POVM.5	POVM.4	POVM.3	POVM.2	POVM.1	POVM.0	0000 0000B
SADEN1	SLAVE ADDRESS MASK 1	BAH	SADEN1.7	SADEN1.6	SADEN1.5	SADEN1.4	SADEN1.3	SADEN1.2	SADEN1.1	SADEN1.0	0000 0000B
SADEN	SLAVE ADDRESS MASK	B9H	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0	0000 0000B
IP	INTERRUPT PRIORITY	B8H	(BF)	(BE) PADC	(BD) PT2	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	0000 0000B
IPH	INTERRUPT HIGH PRIORITY	B7H	-	PADCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	x000 0000B
EIP1H	EXTENDED INTERRUPT HIGH PRIORITY 1	B6H	-	-	PNVMIH	PCPTFH	PT3H	PBKFH	PPWMH	PSPIH	xx00 0000B
RCAP3H	RELOAD CAPTURE 3 HIGH REGISTER	B5H	RCAP3H.7	RCAP3H.6	RCAP3H.5	RCAP3H.4	RCAP3H.3	RCAP3H.2	RCAP3H.1	RCAP3H.0	0000 0000B
RCAP3L	RELOAD CAPTURE 3 LOW REGISTER	B4H	RCAP3L.7	RCAP3L.6	RCAP3L.5	RCAP3L.4	RCAP3L.3	RCAP3L.2	RCAP3L.1	RCAP3L.0	0000 0000B
P5	PORT 5	B1H	-	-	-	-	-	-	PWM7	PWM6	xxxx xx11B
P3	PORT 3	B0H	(B7) RD	(B6) WR	(B5) T1/ IC1/QEB	(B4) T0/ ICO/QEA	(B3) /INT1	(B2) /INT0	(B1) TXD	(B0) RXD	1111 1111B
SFRCN	F/W FLASH CONTROL	AFH	-	WFWIN	NOE	NCE	CTRL3	CTRL2	CTRL1	CTRL0	x011 1111B
SFRFD	F/W FLASH DATA	AEH	D7	D6	D5	D4	D3	D2	D1	D0	xxxx xxxxB
SFRAH	F/W FLASH HIGH ADDRESS	ADH	A15	A14	A13	A12	A11	A10	A9	A8	0000 0000B
SFRAL	F/W FLASH LOW ADDRESS	ACH	A7	A6	A5	A4	A3	A2	A1	A0	0000 0000B
SADDR1	SLAVE ADDRESS 1	AAH	SADDR1.7	SADDR1.6	SADDR1.5	SADDR1.4	SADDR1.3	SADDR1.2	SADDR1.1	SADDR1.0	0000 0000B
SADDR	SLAVE ADDRESS	A9H	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0	0000 0000B
IE	INTERRUPT ENABLE	A8H	(AF) EA	(AE) EADC	(AD) ET2	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	0000 0000B

Continued

SYMBOL	DEFINITION	ADDRESS	MSB BIT_ADDRESS, LSB SYMBOL								RESET
CCH2/MAXCNTH	INPUT CAPTURE 2 HIGH REGISTER/ MAXIMUM COUNTER HIGH REGISTER	A7h	CCH2.7 /MAXCNTH.7	CCH2.6 MAXCNTH.6	CCH2.5 /MAXCNTH.5	CCH2.4 /MAXCNTH.4	CCH2.3 /MAXCNTH.3	CCH2.2 /MAXCNTH.2	CCH2.1 /MAXCNTH.1	CCH2.0 /MAXCNTH.0	0000 0000B
CCL2/MAXCNTL	INPUT CAPTURE 2 LOW REGISTER/ MAXIMUM COUNTER LOW REGISTER	A6h	CCL2.7 /MAXCNTL.7	CCL2.6 /MAXCNTL.6	CCL2.5 /MAXCNTL.5	CCL2.4 /MAXCNTL.4	CCL2.3 /MAXCNTL.3	CCL2.2 /MAXCNTL.2	CCL2.1 /MAXCNTL.1	CCL2.0 /MAXCNTL.0	0000 0000B
P4	PORT 4	A5H	-	-	-	-	P4.3	P4.2	T2EX/IC2	STADC	xxxx 1111B
CAPCON1	CAPTURE CONTROL 1 REGISTER	A4H	-	-	ENF2	ENF1	ENF0	CPTF2	CPTF1/ DIRF	CPTF0/ QEIF	xx00 0000B
CAPCON0	CAPTURE CONTROL 0 REGISTER	A3H	CCT2.1	CCT2.0	CCT1.1	CCT1.0	CCT0.1	CCT0.0	CCLD1	CCLD0	0000 0000B
P4CSIN	P4 CS SIGN	A2H	P43INV	P42INV	P41INV	P40INV	-	PWDNH	RMWFP	P0UP	0000 x000B
XRAMAH	RAM HIGH BYTE ADDRESS	A1H	-	-	-	-	-	A10	A9	A8	0000 0000B
P2	PORT 2	A0H	(A7) A15/ SDA	(A6) A14/ SCL	(A5) A13/ PWM5	(A4) A12/ PWM4	(A3) A11/ PWM3	(A2) A10/ PWM2	(A1) A9/ PWM1	(A0) A8/ PWM0	1111 1111B
CHPCON	ON CHIP PROGRAMMING CONTROL	9FH	SWRST/ REBOOT	-	LD/AP	-	-	-	LDSEL	ENP	0000 0000B
NVMCON	NVM CONTROL	9EH	EER	EWR	EnNVM	-	-	-	-	NVMF	000x xxx0B
P43AH	HI ADDR. COMPARATOR OF P4.3	9DH	A15	A14	A13	A12	A11	A10	A9	A8	0000 0000B
P43AL	LO ADDR. COMPARATOR OF P4.3	9CH	A7	A6	A5	A4	A3	A2	A1	A0	0000 0000B
P42AH	HI ADDR. COMPARATOR OF P4.2	9BH	A15	A14	A13	A12	A11	A10	A9	A8	0000 0000B
P42AL	LO ADDR. COMPARATOR OF P4.2	9AH	A7	A6	A5	A4	A3	A2	A1	A0	0000 0000B
SBUF	SERIAL BUFFER	99H	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0	xxxx xxxxB
SCON	SERIAL CONTROL	98H	(9F) SM0/FE	(9E) SM1	(9D) SM2	(9C) REN	(9B) TB8	(9A) RB8	(99) TI	(98) RI	0000 0000B
P41AH	HI ADDR. COMPARATOR OF P4.1	97H	A15	A14	A13	A12	A11	A10	A9	A8	0000 0000B
P41AL	LO ADDR. COMPARATOR OF P4.1	96H	A7	A6	A5	A4	A3	A2	A1	A0	0000 0000B
P40AH	HI ADDR. COMPARATOR OF P4.0	95H	A15	A14	A13	A12	A11	A10	A9	A8	0000 0000B
P40AL	LO ADDR. COMPARATOR OF P4.0	94H	A7	A6	A5	A4	A3	A2	A1	A0	0000 0000B
P4CONB	P4 CONTROL REGISTER B	93H	P43FUN1	P43FUN0	P43CMP1	P43CMP0	P42FUN1	P42FUN0	P42CMP1	P42CMP0	0000 0000B
P4CONA	P4 CONTROL REGISTER A	92H	P41FUN1	P41FUN0	P41CMP1	P41CMP0	P40FUN1	P40FUN0	P40CMP1	P40CMP0	0000 0000B
EXIF	EXTERNAL INTERRUPT FLAG	91H	IE5	IE4	IE3	IE2	-	-	-	-	0000 xxxxB
P1	PORT 1	90H	(97) ADC7	(96) ADC6	(95) ADC5	(94) ADC4	(93) TXD1/ ADC3	(92) RXD1/ ADC2	(91) ADC1/ Brake	(90) T2/ ADC0	1111 1111B
CKCON1	CLOCK CONTROL 1	8FH	-	-	-	-	-	-	CCDIV1	CCDIV0	0000 0000B
CKCON	CLOCK CONTROL	8EH	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0	0000 0001B
TH1	TIMER HIGH 1	8DH	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0	0000 0000B