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8-BIT MICROCONTROLLER

Table of Contents-

1 GENERAL DESCRIPTION

The W79E4051/2051 series are an 8-bit Turbo 51 microcontroller which has an in-system programmable Flash EPROM which Flash EPROM can program by **ICP (In Circuit Program) Writer**. The instruction set of the W79E4051/2051 series are fully compatible with the standard 8052. The W79E4051/2051 series contain a **4K**/**2K** bytes of program Flash EPROM; a **256** bytes of RAM; **128** bytes data Flash EPROM for customer data storage; two 8-bit bi-directional and bit-addressable I/O ports; two 16-bit timer/counters; an enhanced full duplex serial port; 1 channel PWM by 10-bit counter, Brownout voltage detection/reset, Power on reset detection and one analog comparator. These peripherals are supported by **9** sources of four-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W79E4051/2051 series allow the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

2 FEATURES

- Fully static design 8-bit Turbo 51 CMOS microcontroller up to 24MHz
- Single power: 2.4~5.5V Up to 12MHz, 4.5~5.5V up to 24MHz
- Flexible CPU clock source configurable by config bit and software:
  - High speed external oscillator: upto 24MHz Crystal and resonator (enabled by config bit).
  - Internal RC oscillator: 22.1184/11.0592MHz with ±2% accuracy (selectable by config bit), at 5.0 voltage and 25℃condition, for W79E2051R and W79E4051R
- Instruction-set compatible with MCS-51
- **4K/2K** bytes of Program Flash EPROM, with ICP and external writer programmable mode.
- **256** bytes of on-chip RAM
- W79E4051/2051 supports **128** bytes Data Flash EPROM for customer data storage used and 10K writer cycles.
  - 8 pages. Page size is 16 bytes.
  - Data Flash program/erase V_{DD}=3.0V to 5.5V
- **One 8-bit** bi-directional port(Port1), **one 7-bit** bi-directional port(Port3) and **one 2-bit** bi-directional port(P2.0 and P2.1 shared with XT1 and XT2 pins)
- I/O capable of driving LED max. 20mA per pin, max to 80mA for total pins.
- **Two** 16-bit timer/counters
- **9** Interrupt source with four levels of priority
- **One** enhanced full duplex serial port with framing error detection and automatic address recognition
- **One** channel 10-bit PWM output
- **One** analog Comparator
- Built-in Power Management
  - Power on reset flag
  - Brownout voltage detect/reset
- Operating Temperature: -40~85℃
- Packages:
  - Lead Free (RoHS) PDIP 20: W79E4051AKG
  - Lead Free (RoHS) SOP 20: W79E4051ASG
  - Lead Free (RoHS) SSOP 20: W79E4051ARG
  - Lead Free (RoHS) PDIP 20: W79E2051AKG
  - Lead Free (RoHS) SOP 20: W79E2051ASG
  - Lead Free (RoHS) SSOP 20: W79E2051ARG
  - Lead Free (RoHS) PDIP 20: W79E4051RAKG
  - Lead Free (RoHS) SOP 20: W79E4051RASG
  - Lead Free (RoHS) SSOP 20: W79E4051RARG

- Lead Free (RoHS) PDIP 20: W79E2051RAKG
- Lead Free (RoHS) SOP 20: W79E2051RASG
- Lead Free (RoHS) SSOP 20: W79E2051RARG

3 PARTS INFORMATION LIST

3.1 Lead Free (RoHS) Parts information list

Table 3-1: Lead Free (RoHS) Parts information list

PART NO.	PROGRAM FLASH EPROM	RAM	DATA FLASH EPROM	INTERNAL RC OSCILLATOR ACCURACY[1]	PACKAGE
W79E4051AKG	4KB	256B	128B	22MHz ± 25%	PDIP-20 Pin
W79E4051ASG	4KB	256B	128B	22MHz ± 25%	SOP-20 Pin
W79E4051ARG	4KB	256B	128B	22MHz ± 25%	SSOP-20 Pin
W79E2051AKG	2KB	256B	128B	22MHz ± 25%	PDIP-20 Pin
W79E2051ASG	2KB	256B	128B	22MHz ± 25%	SOP-20 Pin
W79E2051ARG	2KB	256B	128B	22MHz ± 25%	SSOP-20 Pin
W79E4051RAKG	4KB	256B	128B	22.1184MHz ± 2%	PDIP-20 Pin
W79E4051RASG	4KB	256B	128B	22.1184MHz ± 2%	SOP-20 Pin
W79E4051RARG	4KB	256B	128B	22.1184MHz ± 2%	SSOP-20 Pin
W79E2051RAKG	2KB	256B	128B	22.1184MHz ± 2%	PDIP-20 Pin
W79E2051RASG	2KB	256B	128B	22.1184MHz ± 2%	SOP-20 Pin
W79E2051RARG	2KB	256B	128B	22.1184MHz ± 2%	SSOP-20 Pin

Note:

1. Factory calibration condition: V_{DD}=5.0V, TA = 25°C

4 PIN CONFIGURATION

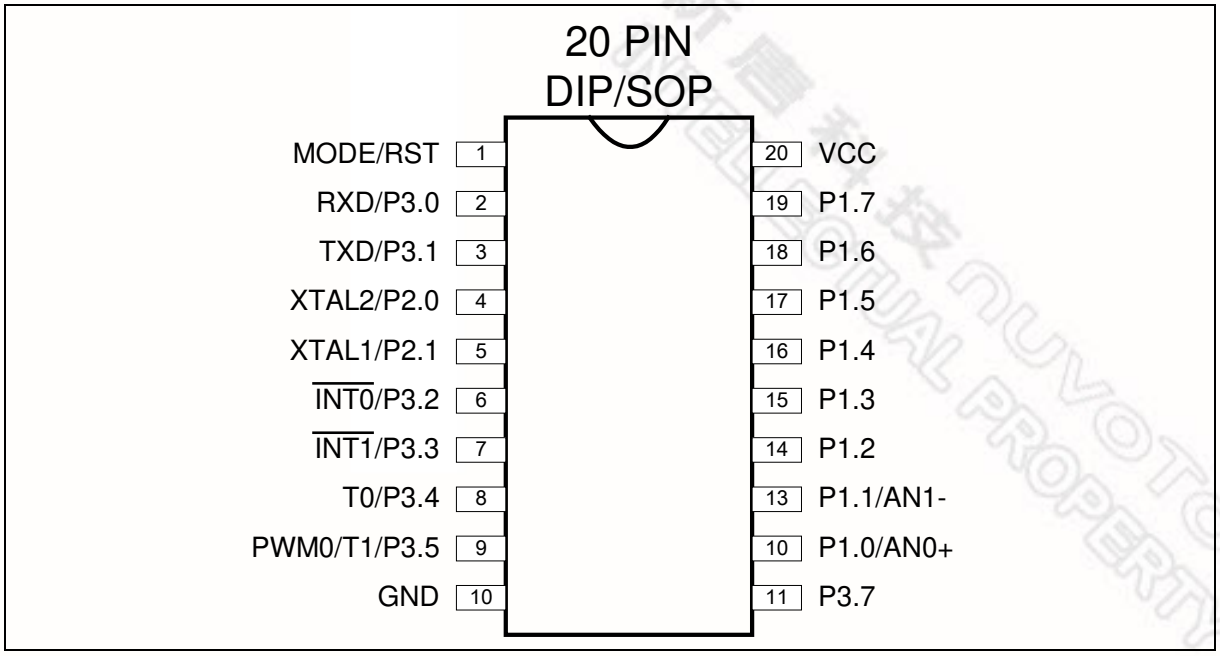

Table 4-1: Pin Configuration

5 PIN DESCRIPTION

SYMBOL	Alternate Function 1	Alternate function 2	Alternate function 3 (ICP mode)	Type		DESCRIPTIONS
P2.1	X1			I/O	I	**CRYSTAL1**: This is the crystal oscillator input. This pin may be driven by an external clock or configurable i/o pin.
P2.0	X2/CLKOUT			I/O	O	**CRYSTAL2**: This is the crystal oscillator output. It is the inversion of XTAL1. Also a configurable i/o pin.
VDD	-			P		**POWER SUPPLY**: Supply voltage for operation.
VSS	-			P		**GROUND**: Ground potential.
RST			MODE	I		**RESET**: A high on this pin for two machine cycles while the oscillator is running resets the device. MODE: used in ICP mode.
P1.0	AN0+			I/O, D		**Port1**: 8-bit bi-directional I/O port with internal weakly pull-ups. P1.0~P1.1 are open-drain mode after reset. Multifunction pins: AN0+ and AN1- are analog comparator inputs. Data and SCK are used in ICP mode.
P1.1	AN1-			I/O, D		
P1.2				I/O		
P1.3				I/O		
P1.4				I/O		
P1.5				I/O		
P1.6			Data	I/O		
P1.7			SCK	I/O		
P3.0	RXD			I/O		**Port3**: 7-bit bi-directional I/O port, P3.0~P3.7 except P3.6, with internal weakly pull-ups. P3.6 is internal wired to analog comparator output. Multifunction pins for TXD & RXD (UART),/INT0-1, T0, T1/PWM0.
P3.1	TXD			I/O		
P3.2	/INT0			I/O		
P3.3	/INT1			I/O		
P3.4	T0			I/O		
P3.5	T1	PWM0		I/O		
P3.6				S		
P3.7				I/O		

* Note : **TYPE P**: Power, I: input, **O**: output, **I/O**: bi-directional, **S**: internal Signal.

6 FUNCTIONAL DESCRIPTION

The W79E4051/2051 architecture consist of a 4T 8051 core controller surrounded by various registers, **4K/2K** bytes AP Flash EPROM, **256** bytes of RAM, **128** bytes Data Flash EPROM, three general purpose I/O ports, two timer/counters, one serial port, Flash EPROM program by Writer and ICP.

6.1 On-Chip Flash EPROM

The W79E4051/2051 includes one **4K/2K** bytes of main Flash EPROM for application program. A Writer or ICP programming board is required to program the AP Flash EPROM and Data Flash EPROM.

This ICP (In-Circuit Programming) feature makes the job easy and efficient when the application's firmware needs to be updated frequently. In some applications, the in-circuit programming feature makes it possible for the end-user to easily update the system firmware without opening the chassis.

6.2 I/O Ports

W79E4051/2051 has one 8-bit, one 7-bit and one 2-bit ports using on-chip oscillator by reset options. Except P1.0 and P1.1, all ports are in quasi-bidirectional structure that the internal weakly pull-ups are present as the port registers are set to logic one. P1.0~P1.1, the alternate function are analog comparator inputs, stays in PMOS-off open-drain mode after CPU reset.

6.3 Serial I/O

The W79E4051/2051 has one serial port that is functionally similar to the serial port of the original 8051 family. However the serial port on the W79E4051/2051 can operate in different modes in order to obtain timing similarity as well. The Serial port has the enhanced features of Automatic Address recognition and Frame Error detection.

6.4 Timers

The W79E4051/2051 has two 16-bit timers that are functionally and similar to the timers of the 8051 family. When used as timers, user has a choice to set 12 or 6 clocks per count that emulates the timing of the original 8051. Each timer's count value is stored in two SFR locations that can be written or read by software. There are also some other SFRs associated with the timers that control their mode and operation.

6.5 Interrupts

The Interrupt structure in the W79E4051/2051 is slightly different from that of the standard 8051. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased.

6.6 Data Pointers

The data pointer of W79E4051/2051 is similar to standard 8051 but has dual 16-bit Data Pointers (DPTR) by setting DPS of AUXR2.0. In addition there is an added instruction, DEC DPTR (op-code A5H), which helps in improving programming flexibility for the user.

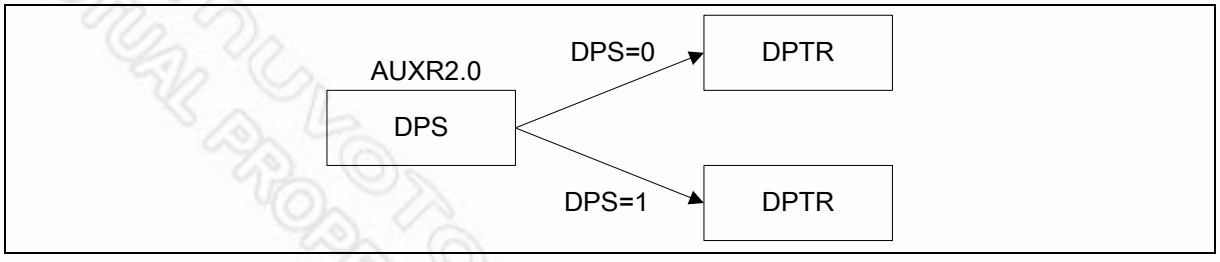

Table 6-1: Data Pointer

6.7 Architecture

The W79E4051/2051 is based on the standard MCS-51 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard MCS-51 instruction set.

6.7.1 ALU

The ALU is the heart of the W79E4051/2051. It is responsible for the arithmetic and logical functions. It is also used in decision making, in case of jump instructions, and is also used in calculating jump address. The user cannot directly use the ALU, but the Instruction Decoder reads the op-code, decodes it, and sequences the data through the ALU and its associated registers to generate the required result. The ALU mainly uses the ACC which is a special function register (SFR) on the chip. Another SFR, namely B register is also used in Multiply and Divide instructions. The ALU generates several status signals which are stored in the Program Status Word register (PSW).

6.7.2 Accumulator

The Accumulator (ACC) is the primary register used in arithmetic, logical and data transfer operations in the W79E4051/2051. Since the Accumulator is directly accessible by the CPU, most of the high speed instructions make use of the ACC as one argument.

6.7.3 B Register

This is an 8-bit register that is used as the second argument in the MUL and DIV instructions. For all other instructions it can be used simply as a general purpose register.

6.7.4 Program Status Word:

This is an 8-bit SFR that is used to store the status bits of the ALU. It holds the Carry flag, the Auxiliary Carry flag, General purpose flags, the Register Bank Select, the Overflow flag, and the Parity flag.

6.7.5 Scratch-pad RAM

The W79E4051/2051 has a 256 byte on-chip scratch-pad RAM. This can be used by the user for temporary storage during program execution. A certain section of this RAM is bit addressable, and can be directly addressed for this purpose.

6.7.6 Stack Pointer

The W79E4051/2051 has an 8-bit Stack Pointer which points to the top of the Stack. This stack resides in the Scratch Pad RAM in the W79E4051/2051. Hence the size of the stack is limited by the size of this RAM.

7 MEMORY ORGANIZATION

The W79E4051/2051 series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

7.1 Program Memory (on-chip Flash)

The Program Memory on the W79E4051/2051 series can be up to **4K/2K** bytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

7.2 Data Flash Memory

The Data Flash EPROM on the W79E4051/2051 series is **128** bytes long with page size of **16** bytes. The W79E4051/2051 series read the content of data memory by using "MOVC A, @A+DPTR". To write data is by NVMADDRL, NVMDATA and NVMCON SFR's registers.

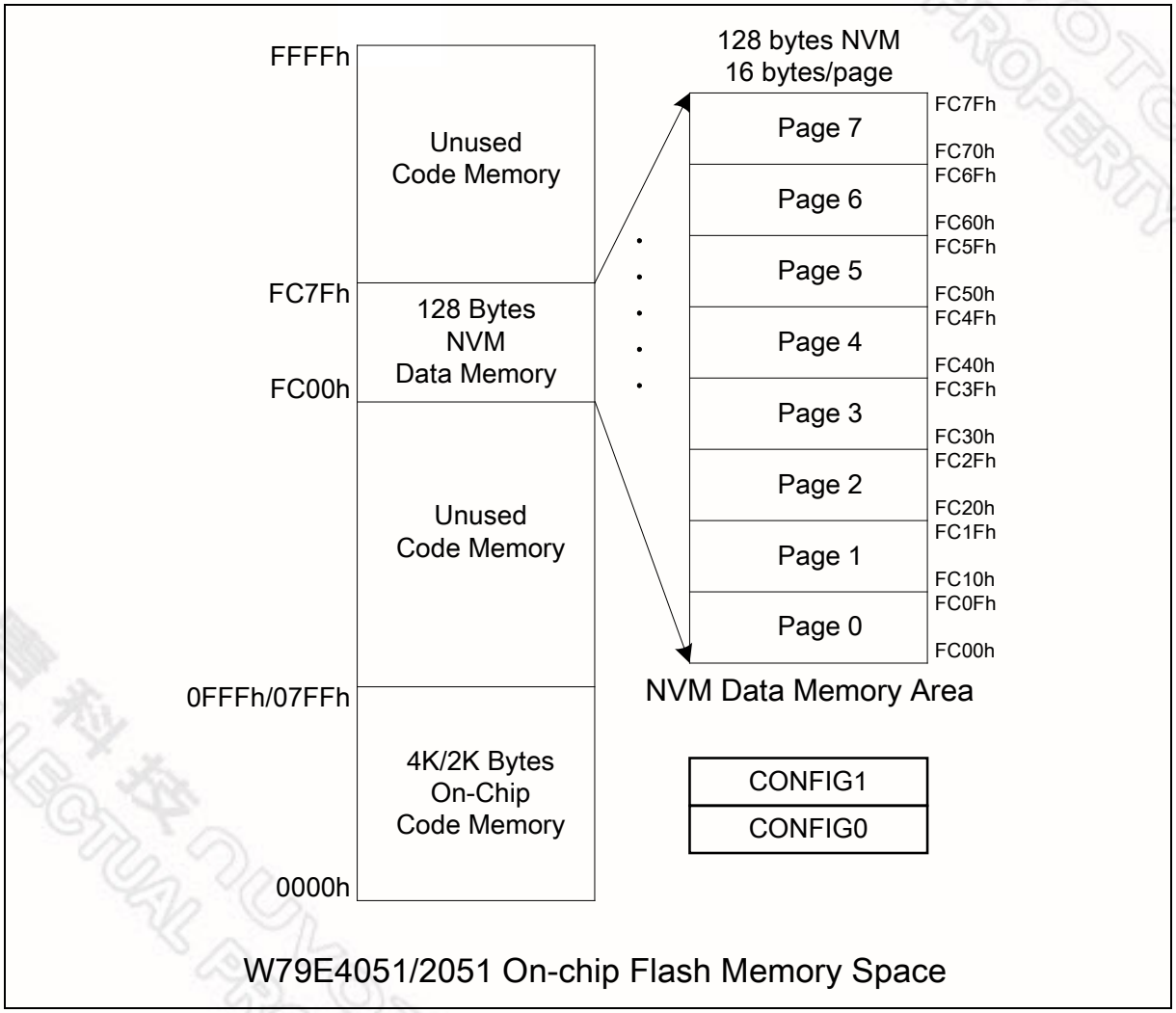

Table 7-1 W79E4051/2051 On-chip Flash Memory Map

7.3 Scratch-pad RAM and Register Map

As mentioned before the W79E4051/2051 series have separate Program and Data Memory areas. The on-chip **256** bytes scratch pad RAM is built in W79E4051/2051. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.

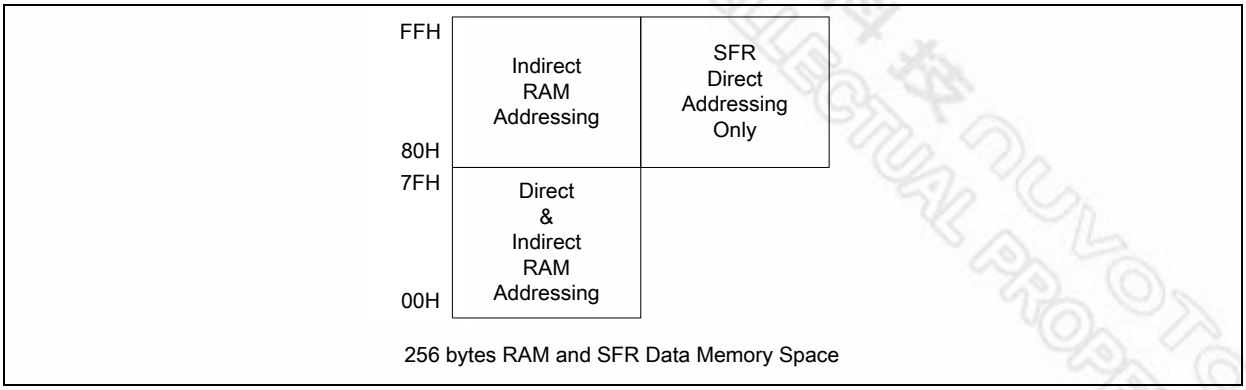

Table 7-2 W79E4051/2051 256 bytes RAM and SFR memory map

Since the scratch-pad RAM is **256** bytes it can be used only when data contents are small. There are several other special purpose areas within the scratch-pad RAM. These are illustrated in next figure.

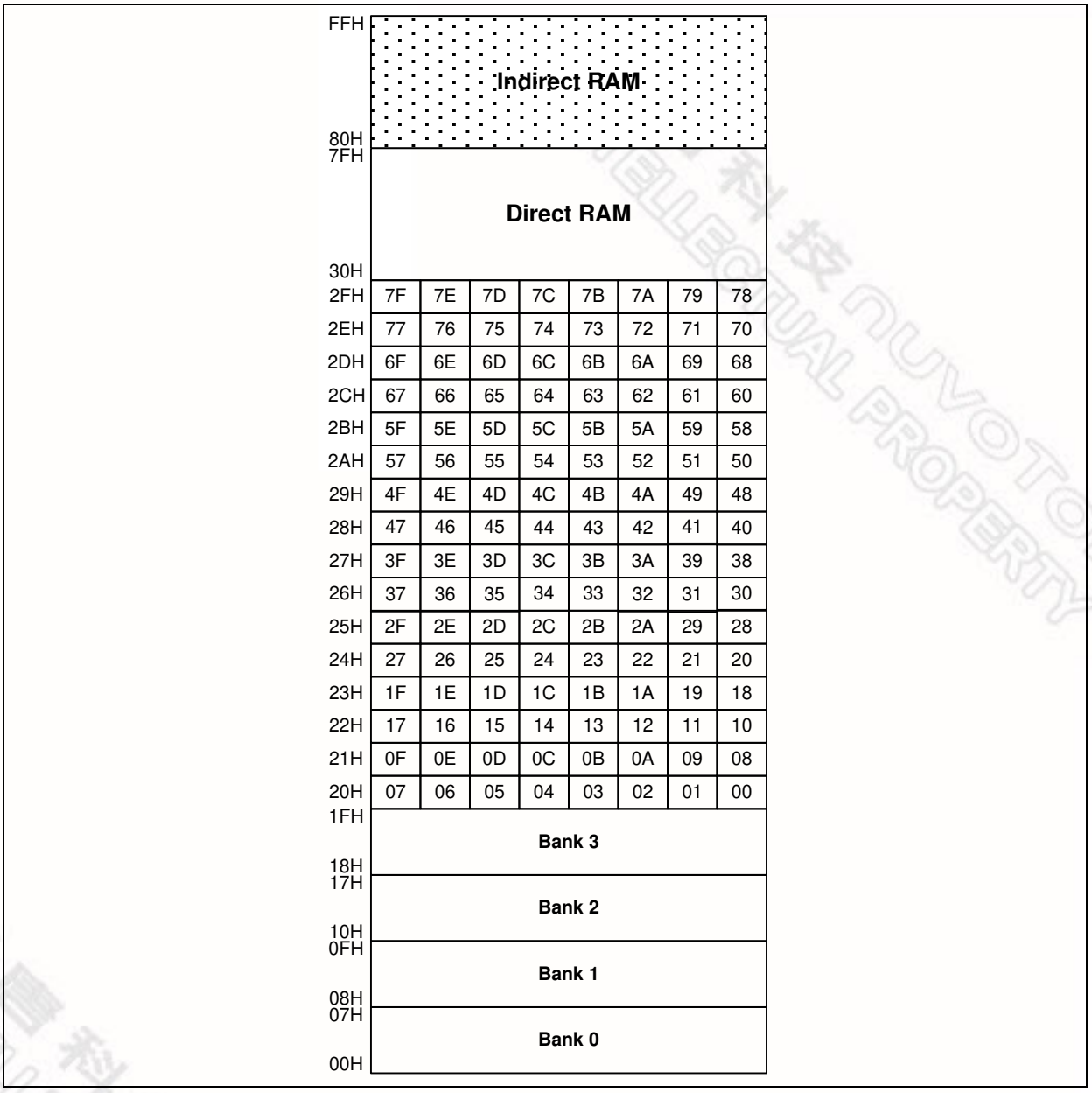

Table 7-3 Scratch-pad RAM

7.4 Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed as Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at one time the W79E4051/2051 series can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

7.5 Bit addressable Locations

The Scratch-pad RAM area from location 20h to 2Fh is byte as well as bit addressable. This means that a bit in this area can be individually addressed. In addition some of the SFRs are also bit addressable. The instruction decoder is able to distinguish a bit access from a byte access by the type of the instruction itself. In the SFR area, any existing SFR whose address ends in a 0 or 8 is bit addressable.

7.6 Stack

The scratch-pad RAM can be used for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a jump, call or interrupt is invoked the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07h at reset. The user can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, and then the SP is decreased.

8 SPECIAL FUNCTION REGISTERS

The W79E4051/2051 series uses Special Function Registers (SFRs) to control and monitor peripherals and their Modes. The SFRs reside in the register locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where users wish to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. The W79E4051/2051 series contain all the SFRs present in the standard 8052. However some additional SFRs are added. In some cases the unused bits in the original 8052, have been given new functions. The list of the SFRs is as follows.

F8	**IP1**							
F0	**B**						PCMPIDS	IP1H
E8	**EIE**							
E0	**ACC**							
D8	**WDCON**	PWMPL	PWM0L		PWMCON1			
D0	**PSW**	PWMPH	PWM0H					PWMCON3
C8							NVMCON	NVMDATA
C0							NVMADDRL	TA
B8	**IP0**	SADEN						
B0	**P3**			P1M1				IP0H
A8	**IE**	SADDR						
A0	**P2**		AUXR1	AUXR2				
98	**SCON**	SBUF						
90	**P1**						ACCK	ACSR
88	**TCON**	TMOD	TL0	TL1	TH0	TH1	CKCON	CLKREG
80		SP	DPL	DPH				PCON

Table 8-1: Special Function Register Location Table

Note:
1. The SFRs in the column with dark borders are bit-addressable
2. The table is condensed with eight locations per row. Empty locations indicate that these are no registers at these addresses.

Special Function Registers:

SYMBOL	DEFINITION	ADDRESS	MSB	BIT ADDRESS, SYMBOL						LSB	RESET
IP1	Interrupt priority 1	F8H	(FF) -	(FE) PBOV	(FD) PPWM	(FC) PWDI	(FB) -	(FA) -	(F9) -	(F8) -	x000 xxxxB
IP1H	Interrupt high priority 1	F7H	-	PBOVH	PPWMH	PWDIH	-	-	-	-	x000 xxxxB
PCMPIDS	Port Comparator Input Disable	F6H	-	-	-	-	-	-	B1	B0	xxxx 0000B
B	B register	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	00000000B
EIE	Interrupt enable 1	E8H	(EF) -	(EE) EBOV	(ED) EPWM	(EC) EWDI	(EB) -	(EA) -	(E9) -	(E8) -	xx000 xxxxB
ACC	Accumulator	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	00000000B
PWMCON1	PWM CONTROL REGISTER 1	DCH	PWMRUN	load	PWMF	CLRPWM	-	-	-	PWM0I	0000 0000B
PWM0L	PWM 0 LOW BITS REGISTER	DAH	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0	0000 0000B
PWMPL	PWM COUNTER LOW REGISTER	D9H	PWMP0.7	PWMP0.6	PWMP0.5	PWMP0.4	PWMP0.3	PWMP0.2	PWMP0.1	PWMP0.0	0000 0000B
WDCON	WATCH-DOG CONTROL	D8H	(DF) WDRUN	(DE) -	(DD) WD1	(DC) WD0	(DB) WDIF	(DA) WTRF	(D9) EWRST	(D8) WDCLR	0X00 0000B
PWMCON3	PWM CONTROL REGISTER 3	D7H	-	-	-	PWM0OE	-	-	FP1	FP0	0000 XX00B
PWM0H	PWM 0 HIGH BITS REGISTER	D2H	-	-	-	-	-	-	PWM0.9	PWM0.8	XXXX XX00B
PWMPH	PWM COUNTER HIGH REGISTER	D1H	-	-	-	-	-	-	PWMP0.9	PWMP0.8	XXXX XX00B
PSW	Program status word	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P	00000000B
NVMDATA	NVM Data	CFH									00000000B
NVMCON	NVM Control	CEH	EER	EWR	-	-	-	-	-		00xxxxxxB
TA	Timed Access Protection	C7H	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0	11111111B
NVMADDRL	NVM byte address	C6H	NVMADDR .7	NVMADDR. 6	NVMADDR .5	NVMADDR .4	NVMADD R.3	NVMADD R.2	NVMADD R.1	NVMADDR .0	00000000B
SADEN	Slave address mask	B9H									00000000B
IP0	Interrupt priority 0	B8H	(BF) -	(BE) PC	(BD) -	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	x0x00000B
IP0H	Interrupt high priority 0	B7H	-	PCH	-	PSH	PT1H	PX1H	PT0H	PX0H	x0x00000B
P1M1	Port1 Mode 1	B3H	-	-	-	-	-	-	P1M1.1	P1M1.0	xxxx xx00B
P3	Port 3	B0H	(B7)	(B6)	(B5) T1	(B4) T0	(B3) INT1	(B2) INT0	(B1) TXD	(B0) RXD	11111111B
SADDR	Slave address	A9H									00000000B
IE	Interrupt enable	A8H	(AF) EA	(AE) EC	(AD) -	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	00x00000B
AUXR2	AUX function register 2	A3H								DPS	xxxx xxx0B
AUXR1	AUX function register 1	A2H	BOF	BOD[2]	BOI	LPBOV	SRST	BOV1[3]	BOV0[3]	BOS	0x00 0xx0B
P2	Port 2	A0H	(A7) -	(A6) -	(A5) -	(A4) -	(A3) -	(A2) -	(A1) P2.1 XTAL1	(A0) P2.0 XTAL2 CLKOUT	xxxx xxxxB
SBUF	Serial buffer	99H									xxxxxxxxB
SCON	Serial control	98H	(9F) SM0/FE	(9E) SM1	(9D) SM2	(9C) REN	(9B) TB8	(9A) RB8	(99) TI	(98) RI	00000000B
ACSR	Analog Comparator Control & Status Register	97H	-	-	CIPE	CF	CEN	CM2	CM1	CM0	xx000000B
ACCK	Analog Comparator Debounce Clock Control	96H	ENCLK	-	-	-	-	CPCK2	CPCK1	CPCK0	0000 0000B
P1	Port 1	90H	(97)	(96)	(95)	(94)	(93)	(92)	(91)	(90)	11111111B
CLKREG		8FH						PWDEX1	PWDEX0		Xxxx x00xB
CKCON	**Clock control**	**8EH**	**-**	**-**	**-**	**T1M**	**T0M**	**-**	**-**	**-**	**xxx00xxxB**
TH1	Timer high 1	8DH									00000000B
TH0	Timer high 0	8CH									00000000B
TL1	Timer low 1	8BH									00000000B
TL0	Timer low 0	8AH									00000000B
TMOD	Timer mode	89H	GATE	C/T1#	M1	M0	GATE	C/T0#	M1	M0	00000000B
TCON	Timer control	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	00000000B
PCON	Power control	87H	SMOD	SMOD0		POR	GF1	GF0	PD	IDL	00xx0000B
DPH	Data pointer high	83H									00000000B
DPL	Data pointer low	82H									00000000B
SP	Stack pointer	81H									00000111B

Table 8-2: Special Function Registers

Note :
1. In column **BIT_ADDRESS, SYMBOL**, containing ( ) item means the bit address.
2. BOD is initialized at reset with the inversed value of bit CBOD in config0-bits.
3. (BOV1,BOV0) are initialized at reset with the reversed value of config0-bits (CBOV1,CBOV0)

STACK POINTER

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

BIT	NAME	FUNCTION
7-0	SP.[7:0]	The Stack Pointer stores the Scratch-pad RAM address where the stack begins. In other words it always points to the top of the stack.

DATA POINTER LOW

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

BIT	NAME	FUNCTION
7-0	DPL.[7:0]	This is the low byte of the standard 8052 16-bit data pointer.

DATA POINTER HIGH

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

BIT	NAME	FUNCTION
7-0	DPH.[7:0]	This is the high byte of the standard 8052 16-bit data pointer.

POWER CONTROL

Bit:	7	6	5	4	3	2	1	0
	SMOD	SMOD0	-	POR	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: This bit doubles the serial port baud rate in mode 1, 2, and 3.
6	SMOD0	0: Framing Error Detection Disable. SCON.7 (SM0/FE) bit is used as SM0 (standard 8052 function). 1: Framing Error Detection Enable. SCON.7 (SM0/FE) bit is used to reflect as Frame Error (FE) status flag.
5	-	Reserved
4	POR	0: Cleared by software. 1: Set automatically when a power-on reset has occurred.
3	GF1	General purpose user flags.
2	GF0	General purpose user flags.
1	PD	1: The CPU goes into the POWER DOWN mode. In this mode, all the clocks are stopped and program execution is frozen.

0	IDL	1: The CPU goes into the IDLE mode. In this mode, the clocks CPU clock stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating.

TIMER CONTROL

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 Overflow Flag. This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
5	TF0	Timer 0 Overflow Flag. This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
3	IE1	Interrupt 1 Edge Detect Flag: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
2	IT1	Interrupt 1 Type Control. Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect Flag. Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
0	IT0	Interrupt 0 Type Control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
	TIMER1				TIMER0			

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.
5	M1	Timer 1 mode select bit 1. See table below.

4	M0	Timer 1 mode select bit 0. See table below.
3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 control bit is set.
2	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the T0 pin.
1	M1	Timer 0 mode select bit 1. See table below.
0	M0	Timer 0 mode select bit 0. See table below.

M1, M0: Mode Select bits:

M1	M0	MODE
0	0	Mode 0: 8-bit timer/counter TLx serves as 5-bit pre-scale.
0	1	Mode 1: 16-bit timer/counter, no pre-scale.
1	0	Mode 2: 8-bit timer/counter with auto-reload from THx.
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer0 control bits. TH0 is an 8-bit timer only controlled by Timer1 control bits. (Timer 1) Timer/Counter 1 is stopped.

TIMER 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

BIT	NAME	FUNCTION
7-0	TL0.[7:0]	Timer 0 LSB.

TIMER 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

BIT	NAME	FUNCTION
7-0	TL1.[7:0]	Timer 1 LSB.

TIMER 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

BIT	NAME	FUNCTION
7-0	TH0.[7:0]	Timer 0 MSB.

TIMER 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

BIT	NAME	FUNCTION
7-0	TH1.[7:0]	Timer 1 MSB.

CLOCK CONTROL

Bit:	7	6	5	4	3	2	1	0
	-	-	-	T1M	T0M	-	-	-

Mnemonic: CKCON Address: 8Eh

BIT	NAME	FUNCTION
7-5	-	Reserved.
4	T1M	Timer 1 clock select: 0: Timer 1 uses a divide by 12 clocks. 1: Timer 1 uses a divide by 6 clocks.
3	T0M	Timer 0 clock select: 0: Timer 0 uses a divide by 12 clocks. 1: Timer 0 uses a divide by 6 clocks.
2-0	-	Reserved.

CLOCK REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	PWDEX1	PWDEX0	-

Mnemonic: CLDREG Address: 8Fh

BIT	NAME	FUNCTION
7-5	-	Reserved.
2	PWDEX1	Power Down Exit Mode.
1	PWDEX0	Power Down Exit Mode.
0	-	Reserved.

Power Down Exit Mode:

PWDEX1	PWDEX0	Power Down Exit Mode
0	0	Wake up from Power Down is internally timed. $\overline{INT0}$ or $\overline{INT1}$ must be configured for low-level trigger mode.
0	1	Wake up from Power Down is externally controlled. $\overline{INT0}$ or $\overline{INT1}$ must be configured for low-level trigger mode.
1	x	Wake up from Power Down immediately. $\overline{INT0}$ or $\overline{INT1}$ can be configured for low-level or edge trigger mode.

PORT 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
1	P1.1	AN1+
0	P1.0	AN0-

ANALOG COMPARATOR DEBOUNCE CLOCK CONTROL

Bit:	7	6	5	4	3	2	1	0
	ENCLK	-	-	-	-	CPCK2	CPCK1	CPCK0

Mnemonic: ACCK Address: 96h

BIT	NAME	FUNCTION
7	ENCLK	1: Enable clock output to the XTAL2 pin (P2.0) when CPU clock is from the external OSC or on-chip RC oscillator. The frequency of the clock output is 1/4 of the CPU clock rate.
6-3	-	Reserved.
2	CPCK2	See as below table.
1	CPCK1	See as below table.
0	CPCK0	See as below table.

Comparator Debouncing Time Setting:

CPCK2	CPCK 1	CPCK 0	Debouncing Time
0	0	0	$(3/F_{DB})*2$~$(4/F_{DB})*2$
0	0	1	$(3/F_{DB})*4$~$(4/F_{DB})*4$
0	1	0	$(3/F_{DB})*8$~$(4/F_{DB})*8$
0	1	1	$(3/F_{DB})*16$~$(4/F_{DB})*16$
1	0	0	$(3/F_{DB})*32$~$(4/F_{DB})*32$
1	0	1	$(3/F_{DB})*64$~$(4/F_{DB})*64$
1	1	0	$(3/F_{DB})*128$~$(4/F_{DB})*128$

ANALOG COMPARATOR CONTROL & STATUS REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	CIPE	CF	CEN	CM2	CM1	CM0

Mnemonic: ACSR Address: 97h

BIT	NAME	FUNCTION
7-6	-	Reserved.
5	CIPE	Comparator Enabled in Idle and Power down Mode. 0: Comparator disabled in idle and power down mode. (default) 1: Comparator enabled in idle and power down mode.
4	CF	Comparator Interrupt Flag. Set by hardware when the comparator output meet the conditions specified by the CM[2:0] bits and CEN is set. The flag must be cleared by software. The interrupt may be enabled/disabled by setting/clearing bit 6 of IE.
3	CEN	Enable Comparator. Set this bit to enable the comparator. Clearing this bit will force the comparator output low and prevent further events from setting CF.
2	CM2	See as below table.
1	CM1	See as below table.
0	CM0	See as below table.

Comparator Interrupt Mode Setting:

CM2	CM1	CM0	Interrupt Mode
0	0	0	Negative (Low) level
0	0	1	Positive edge
0	1	0	Toggle with debounce
0	1	1	Positive edge with debounce
1	0	0	Negative edge
1	0	1	Toggle
1	1	0	Negative edge with debounce
1	1	1	Positive (High) level

SERIAL PORT CONTROL

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial port mode select bit 0 or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.
6	SM1	Serial Port mode select bit 1. See table below.
5	SM2	Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1, then RI will not be activated if a valid stop bit was not received. In mode 0, the SM2 bit controls the serial port clock. If set to 0, then the serial port runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052. When set to 1, the serial clock become

		divide by 4 of the oscillator clock. This results in faster synchronous serial communication.
4	REN	Receive enable: 0: Disable serial reception. 1: Enable serial reception.
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.

SM1, SM0: Mode Select bits:

Mode	SM0	SM1	Description	Length	Baud Rate
0	0	0	Synchronous	8	Tclk divided by 4 or 12
1	0	1	Asynchronous	10	Variable
2	1	0	Asynchronous	11	Tclk divided by 32 or 64
3	1	1	Asynchronous	11	Variable

SERIAL DATA BUFFER

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

BIT	NAME	FUNCTION
7~0	SBUF	Serial data on the serial port is read from or written to this location. It actually consists of two separate internal 8-bit registers. One is the receive resister, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

PORT 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	P2.1	P2.0

Mnemonic: P2 Address: A0h

BIT	NAME	ALTERNATE FUNCTION
7-2	-	Reserved
1	P2.1	XTAL1 clock input pin.
0	P2.0	XTAL2 or CLKOUT pin by alternative.

AUX FUNCTION REGISTER 1