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8-BIT MICROCONTROLLER

Table of Contents-

1. General Description

The W79E659 is a fast, 8051/52-compatible microcontroller with a redesigned processor core that eliminates wasted clock and memory cycles. Typically, the W79E659 executes instructions 1.5 to 3 times faster than that of the traditional 8051/52, depending on the type of instruction, and the overall performance is about 2.5 times better at the same crystal speed. As a result, with the fully-static CMOS design, the W79E659 can accomplish the same throughput with a lower clock speed, reducing power consumption.

The W79E659 provides 256 bytes of on-chip RAM; 1-KB of auxiliary RAM; seven 8-bit, bi-directional and bit-addressable I/O ports; an additional 4-bit port P4; three 16-bit timer/counters; an UART serial port, 2 channels of I2C with master/slave capability and 8 channels of 10-bit ADC. These peripherals are all supported by ten interrupt sources with 2 levels of priority.

The W79E659 contains a 32-KB Flash EPROM whose contents may be updated in-system by a loader program stored in an auxiliary, 4-KB Flash EPROM. Once the contents are confirmed, it can be protected for security.

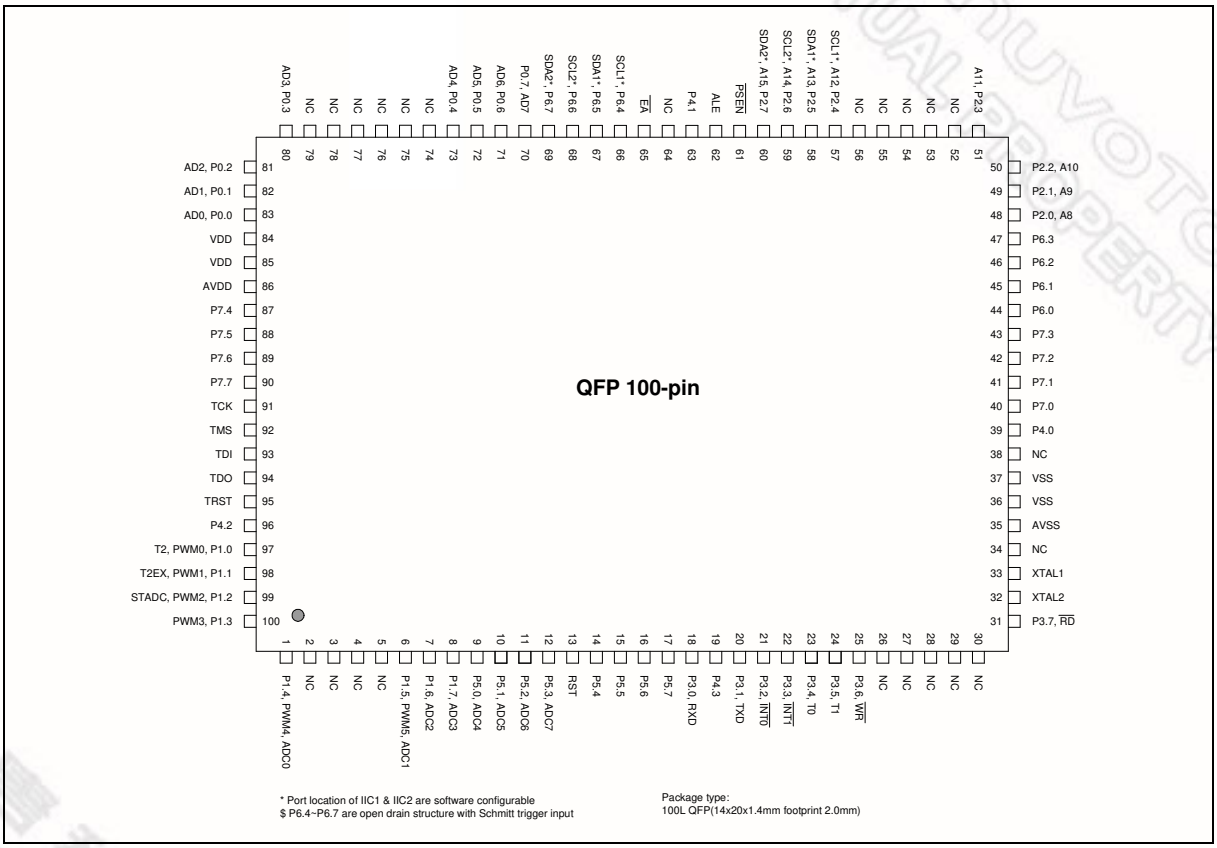
Note: If the applied V_{DD} is not stable, especially with long transition time of power on/off, it's recommended to apply an external RESET IC to the RST pin for improving the stability of system.

2. Features

- Fully-static-design 8-bit Turbo 51 CMOS microcontroller up to 40MHz
- 32-KB of in-system-programmable Flash EPROM (AP Flash EPROM with ISP)
- 4-KB of Auxiliary Flash EPROM for the loader program (LD Flash EPROM)
- 1-KB auxiliary RAM, software-selectable, accessed by MOVX instruction
- 256 bytes of scratch-pad RAM
- Seven 8-bit bi-directional ports
- All pins with Schmitt trigger inputs
- One 4-bit multipurpose I/O port4 with Chips select(CS) and boot function
- Three 16-bit timers
- 6 channels of 8-bit PWM
- One enhanced full-duplex UART with framing-error detection and automatic address recognition
- 2-channels of I2C with master/slave capability
- 10-bit ADC with 8-channel inputs
- Software programmable access cycle to external RAM/peripherals
- 10 interrupt sources with two levels of priority
- Software reset function
- Optional H/L state of ALE/PSEN during power down mode
- Built-in power management
- Code protection
- Development tool
  - JTAG ICE(In Circuit Emulator) tool
- Packages:
  - Lead Free(RoHS) QFP 100: W79E659A40FL, W79L659A25FL

DEVICE	OPERATING FREQUENCY	OPERATING VOLTAGE	PACKAGE
			LEAD FREE(ROHS)
W79E659A40FL	up to 40MHz	4.5V ~ 5.5V	QFP100
W79L659A25FL	up to 25MHz	3.0V ~ 4.5V	QFP100

3. Pin Configuration



* Port location of IIC1 & IIC2 are software configurable
$ P6.4~P6.7 are open drain structure with Schmitt trigger input

Package type:
100L QFP(14x20x1.4mm footprint 2.0mm)

4. PIN DESCRIPTION

SYMBOL	TYPE[1]	DESCRIPTIONS
$\overline{EA}$	I	**EXTERNAL ACCESS ENABLE:** This pin forces the processor to execute the external ROM. The ROM address and data are not presented on the bus if the $\overline{EA}$ pin is high.
$\overline{PSEN}$	O H	**PROGRAM STORE ENABLE:** $\overline{PSEN}$ enables the external ROM data in the Port 0 address/data bus. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs originate from this pin.
ALE	O H	**ADDRESS LATCH ENABLE:** ALE enables the address latch that separates the address from the data on Port 0.
RST	I L	**RESET:** Set this pin high for two machine cycles while the oscillator is running to reset the device.
XTAL1	I	**CRYSTAL 1:** Crystal oscillator input or external clock input.
XTAL2	O	**CRYSTAL 2:** Crystal oscillator output.
V_{SS}	I	**GROUND**: ground potential.
V_{DD}	I	**POWER SUPPLY:** Supply voltage for operation.
AV_{SS}	I	**Analog GROUND:** for ADC
AV_{DD}	I	**Analog Power Supply:** for ADC
P0.0–P0.7	I/O D S H	**PORT 0:** 8-bit, bi-directional I/O port with internal pull-up resisters. This port also provides a multiplexed, low-order address / data bus during accesses to external memory.
P1.0–P1.7	I/O S H	**PORT 1:** 8-bit, bi-directional I/O port with internal pull-up resistors. This port also provides alternate functions as below. P1.0 ~ P1.5 provide PWM0 ~ PWM5. P1.4 ~ P1.7 provide ADC0 ~ ADC3. P1.0 alternately provides Timer2 external count input.(T2) P1.1 alternately provides Timer2 Reload/Capture/Direction control.(T2Ex)
P2.0–P2.7	I/O S H	**PORT 2:** 8-bit, bi-directional I/O port with internal pull-ups. This port also provides the upper address bits when accessing external memory. P2.4 to P2.7 can be software configured as I2C serial ports
P3.0–P3.7	I/O S H	**PORT 3:** 8-bit, bi-directional I/O port with internal pull-up resistors. All bits have alternate functions, which are described below: RXD (P3.0): Serial Port 0 input TXD (P3.1): Serial Port 0 output $\overline{INT0}$ (P3.2): External Interrupt 0 $\overline{INT1}$(P3.3): External Interrupt 1 T0 (P3.4):Timer 0 External Input T1 (P3.5):Timer 1 External Input $\overline{WR}$ (P3.6): External Data Memory Write Strobe $\overline{RD}$ (P3.7): External Data Memory Read Strobe

PIN DESCRIPTION, continued

SYMBOL	TYPE	DESCRIPTIONS
P4.0–P4.3	I/O S H	**PORT 4:** 4-bit bi-directional I/O port. The P4.3 also provides the alternate function $\overline{\text{REBOOT}}$ which is H/W reboot from LD flash.
P5.0-P5.7	I/O H	**PORT 5:** A bi-directional I/O port with internal pull-ups. This port is not bit-addressable. The alternate functions of P5.0 to P5.3 are inputs of ADC4 to ADC7.
P6.0-P6.7	I/O D H	**PORT 6:** A bi-directional I/O port with internal pull-ups. This port is not bit-addressable. Pins P6.4 to P6.7 are open drain type and can be software configured as the I2C ports.
P7.0-P7.7	I/O H	**PORT 7:** A bi-directional I/O port with internal pull-ups. This port is not bit-addressable.
TCK[2]	I H	Used in debug mode with internal pull-up
TMS[2]	I H	Used in debug mode with internal pull-up
TDI[2]	I H	Used in debug mode with internal pull-up
TDO[2]	O L	Used in debug mode with internal weakly pull-low
TRST[2]	I H	Used in debug mode with internal pull-up

Note: 1. TYPE I : input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain S: Schmitt Trigger
2. Keep debug pins in NC(no connection) if chip is not in debug mode.

4.1 Port 4

SFR P4 at address A5H, is a 4-bit multipurpose programmable I/O port which functions are I/O, insert wait function and chip-select function. The Port 4 has four different operation modes:

In mode 0, P4.0 ~ P4.3 is a 4-bit bi-directional I/O port which is the same as port 1. The default Port 4 is a general I/O function.

In mode1, P4.0 ~ P4.3 are read data strobe signals which are synchronized with $\overline{\text{RD}}$ signal at specified addresses. These read data strobe signals can be used as chip-select signals for external peripherals.

In mode2, P4.0 ~ P4.3 are write data strobe signals which are synchronized with $\overline{\text{WR}}$ signal at specified addresses. These write data strobe signals can be used as chip-select signals for external peripherals.

In mode3, P4.0 ~ P4.3 are read/write data strobe signals which are synchronized with $\overline{\text{RD}}$ or $\overline{\text{WR}}$ signal at specified addresses. These read/write data strobe signals can be used as chip-select signals for external peripherals.

In mode1~mode3, Port 4 is configured with the feature of chip-select signals, the address range for chip-select signals depends on the contents of registers P4xAH and P4xAL, which contain the high-order byte and low-order byte, respectively, of the 16-bit address comparator for P4.x. The registers P4CONA and P4CONB contain the control bits to configure the Port 4 operation mode. This is illustrated in the following schematic.

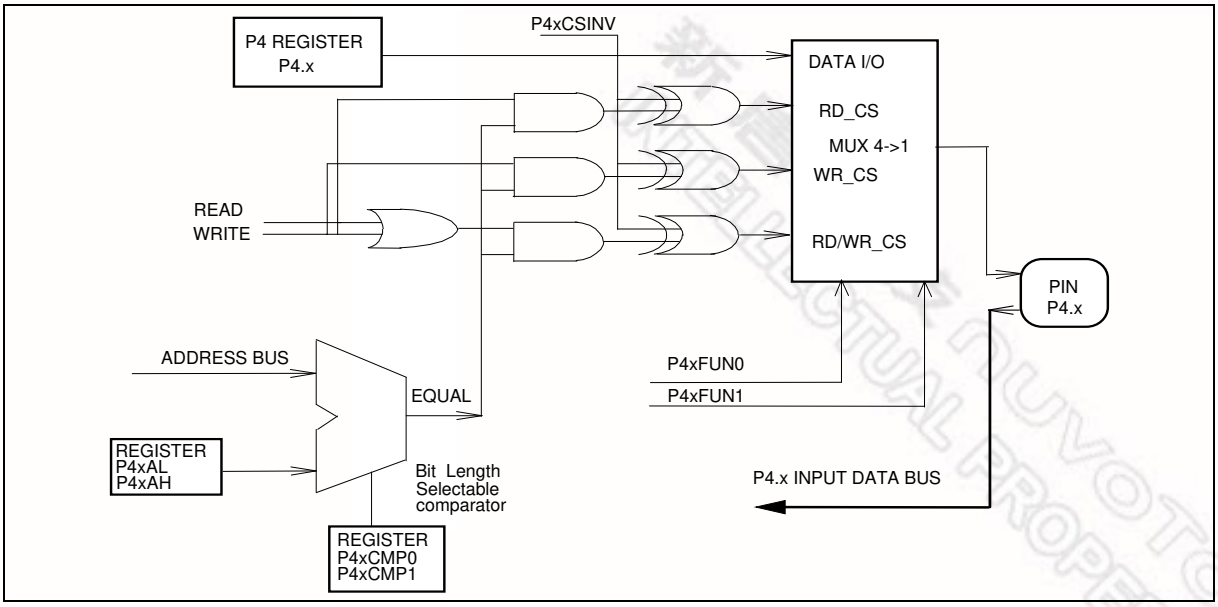


Figure 4-1

For example, the following program sets up P4.0 as a write-strobe signal for I/O port addresses 1234H – 1237H with positive polarity, while P4.1 – P4.3 are used as general I/O ports.

```
MOV  P40AH, #12H
MOV  P40AL, #34H       ; Base I/O address 1234H for P4.0
MOV  P4CONA, #00001010B    ; P4.0 is a write-strobe signal; address lines A0 and A1 are masked.
MOV  P4CONB, #00H   ; P4.1 – P4.3 are general I/O ports
MOV  P2ECON, #10H   ; Set P40SINV to 1 to invert the P4.0 write-strobe to positive polarity.
```

Then, any instruction MOVX @DPTR, A (where DPTR is in 1234H – 1237H) generates a positive-polarity, write-strobe signal on pin P4.0, while the instruction MOV P4, #XX puts bits 3 – 1 of data #XX on pins P4.3 – P4.1.

5. Memory Organization

The W79E659 separates the memory into two separate sections, the Program Memory and the Data Memory. Program Memory stores instruction op-codes, while Data Memory stores data or memory-mapped devices.

5.1 Program Memory (on-chip Flash)

On the standard 8051/52, only 64 KB of Program Memory can be addressed, and, in the W79E659, this area is the 32-KB Flash EPROM (AP Flash EPROM). All instructions are fetched from this area, and the MOVC instruction can also access this region. Pull $\overline{EA}$ high to let the CPU fetch code in the embedded flash ROM, as long as the program counter is lower than 32K. When the program counter is higher than 32K, the CPU automatically fetches program code from extended external program memory.

There is an auxiliary 4-KB Flash EPROM (LD Flash EPROM), where the loader program for In-System Programming (ISP) resides. The AP Flash EPROM is re-programmed by serial or parallel download according to this loader program.

5.2 Data Memory

The W79E659 can access up to 64Kbytes of external Data Memory. This memory region is accessed by the MOVX instructions. Unlike the 8051 derivatives, the W79E659 contains on-chip 1K-bytes of Data Memory, which only can be accessed by MOVX instructions. The 1-Kbytes of SRAM located between address 0000h and 03FFh is enabled by setting DMEO bit of PMR register. If MOVX instruction accesses the addresses greater than 03FFh CPU will automatically access external memory through Port 0 and 2. In default condition the 1K-bytes SRAM is disabled and any MOVX directed to the space between 0000h and FFFFh goes to the expanded bus on the Port 0 and 2. The W79E659 also has the standard 256 bytes of on-chip Scratchpad RAM. This can be accessed either by direct addressing or by indirect addressing. There are also some Special Function Registers (SFRs), which can only be accessed by direct addressing. Since the Scratchpad RAM is only 256 bytes, it can be used only when data contents are small.

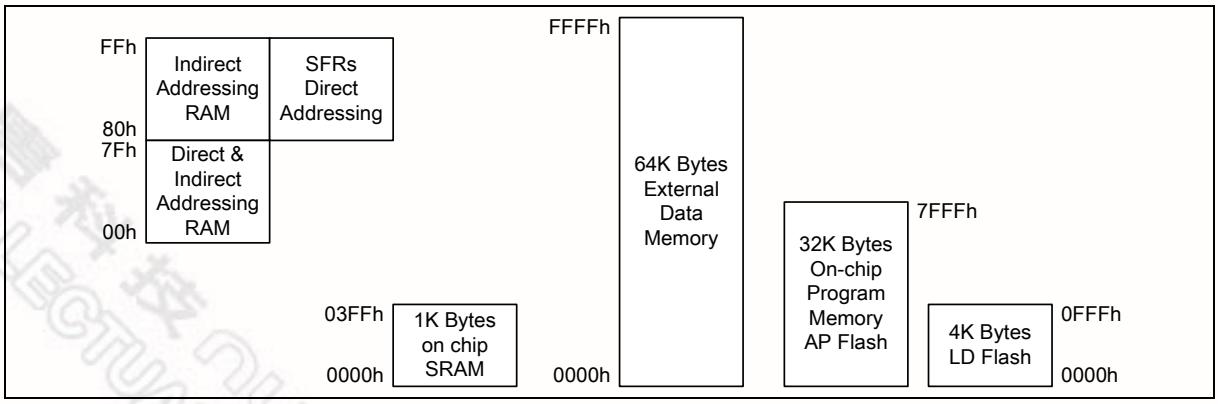


Figure 5-1 Memory Map

6. Special Function Registers

The W79E659 uses Special Function Registers (SFR) to control and monitor peripherals. The SFR reside in register locations 80-FFh and are only accessed by direct addressing. The W79E659 contains all the SFR present in the standard 8051/52, as well as some additional SFR, and, in some cases, unused bits in the standard 8051/52 have new functions. SFR whose addresses end in 0 or 8 (hex) are bit-addressable. The following table of SFR is condensed, with eight locations per row. Empty locations indicate that there are no registers at these addresses. When a bit or register is not implemented, it reads high.

Table 6-1 Special Function Register Location Table

F8	EIP	I2CON2	I2ADDR20	I2ADDR21	I2DATA2	I2STATUS2	I2CLK2	I2TIMER2
F0	B							
E8	EIE	I2CON	I2ADDR10	I2ADDR11	I2DATA	I2STATUS	I2CLK	I2TIMER
E0	ACC							
D8	WDCON	PWMP	PWM0	PWM1	PWMCON1	PWM2	PWM3	
D0	PSW							WDCON2
C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	PWMCON2	PWM4
C0	ADDCON	ADCL	ADCH	PWM5	PMR	STATUS	ADCPS	TA
B8	IP	SADEN						
B0	P3	P5	P6	P7				
A8	IE	SADDR			SFRAL	SFRAH	SFRFD	SFRCN
A0	P2	XRAMAH	P4CSIN			P4		
98	SCON	SBUF	P42AL	P42AH	P43AL	P43AH		CHPCON
90	P1		P4CONA	P4CONB	P40AL	P40AH	P41AL	P41AH
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	
80	P0	SP	DPL	DPH				PCON

1. The SFRs in the column with dark borders are bit-addressable
2. The table is condensed with eight locations per row. Empty locations indicate that these are no registers at these addresses. When a bit or register is not implemented, it will read high.

Table 6-2 Special Function Registers

SYMBOL	DEFINITION	ADDRESS	MSB	BIT_ADDRESS, SYMBOL					LSB		RESET
I2TIMER2	I2C2 Timer Counter Register	FFH	-	-	-	-	-	ENTI2	DIV42	TIF2	0000 0000B
I2CLK2	I2C2 Clock Rate	FEH	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0	0000 0000B
I2STATUS2	I2C2 Status Register	FDH						-	-	-	0000 0000B
I2DAT2	I2C2 Data	FCH	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0	xxxx xxxxxB
I2ADDR21	I2C2 Slave Address1	FBH	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	-	xxxx xxxxxB
I2ADDR20	I2C2 Slave Address0	FAH	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	GC	xxxx xxxx0B
I2CON2	I2C2 Control Register	F9H	-	ENS2	STA	STO	SI	AA	-	PSEL2	x000 00x0B
EIP	Extended Interrupt Priority	F8H	(FF) -	(FE) -	(FD) -	(FC) PWDI	(FB) -	(FA) -	(F9) PI2C2	(F8) PI2C1	0000 0000B
PCH	PC Counter high register	F2H									00000000B
PCL	PC Counter low register	F1H									00000000B
B	B Register	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	0000 0000B
I2TIMER	I2C1 Timer Counter Register	EFH	-	-	-	-	-	ENTI	DIV4	TIF	0000 0000B
I2CLK	I2C1 Clock Rate	EEH	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0	0000 0000B
I2STATUS	I2C1 Status Register	EDH						-	-	-	0000 0000B
I2DAT	I2C1 Data	ECH	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0	xxxx xxxxxB
I2ADDR11	I2C1 Slave Address1	EBH	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	-	xxxx xxxxxB
I2ADDR10	I2C1 Slave Address0	EAH	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	GC	xxxx xxxx0B
I2CON	I2C1 Control Register	E9H	-	ENS1	STA	STO	SI	AA	-	-	x000 00x0B
EIE	Extended Interrupt Enable	E8H	(EF) -	(EE) -	(ED) -	(EC) EWDI	(EB) -	(EA) -	(E9) EI2C2	(E8) EI2C1	0000 0000B
ACC	Accumulator	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	0000 0000B
PWM3	PWM3 Output	DEH									0000 0000B
PWM2	PWM2 Output	DDH									0000 0000B
PWMCON1	PWM Control Register1	DCH	PWM3OE	PWM2OE	ENPWM3	ENPWM2	PWM1OE	PWM0OE	ENPWM1	ENPWM0	0000 0000B
PWM1	PWM1 Output	DBH									0000 0000B
PWM0	PWM0 Output	DAH									0000 0000B
PWMP	PWM Pre-scale Register	D9H									0000 0000B
WDCON	Watch-Dog Control	D8H	(DF) -	(DE) POR	(DD) -	(DC) -	(DB) WDIF	(DA) WTRF	(D9) EWT	(D8) RWT	0100 0000B
WDCON2	Watch-Dog Control2	D7H	-	-	-	-	-	-	-	STRLD	0000 0000B
PSW	Program Status Word	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P	0000 0000B

Table 6-3 Special Function Registers, continued

SYMBOL	DEFINITION	ADDRESS	MSB	BIT_ADDRESS, SYMBOL						LSB	RESET
PWM4	PWM4 Output	CFH									0000 0000B
PWMCON2	PWM Control Register 2	CEH	-	-	-	-	PWM5OE	PWM4OE	ENPWM5	ENPWM4	0000 0000B
TH2	T2 reg. High	CDH									0000 0000B
TL2	T2 reg. Low	CCH									0000 0000B
RCAP2H	T2 Capture Low	CBH									0000 0000B
RCAP2L	T2 Capture High	CAH									0000 0000B
T2MOD	Timer 2 Mode	C9H	-	-	-	-	T2CR	-	-	DCEN	xxxx 0xx0B
T2CON	Timer 2 Control	C8H	(CF) TF2	(CE) EXF2	(CD) RCLK	(CC) TCLK	(CB) EXEN2	(CA) TR2	(C9) C/T2	(C8) CP/RL2	0000 0000B
TA	Time Access Register	C7H									0000 0000B
ADCPS	ADC Input Pin Switch	C6H	ADCPS.7	ADCPS.6	ADCPS.5	ADCPS.4	ADCPS.3	ADCPS.2	ADCPS.1	ADCPS.0	0000 0000B
STATUS	Status Register	C5H	-	HIP	LIP	-	-	-	-	-	x00x xxxxB
PMR	Power Management Register	C4H	-	-	-	-	-	ALEOFF	-	DME0	xxxx x0x0B
PWM5	PWM5 Output	C3H									0000 0000B
ADCH	ADC converter Result High Byte	C2H	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2	xxxx xxxxxB
ADCL	ADC converter Result Low Byte	C1H	ADCLK1	ADCLK0	-	-	-	-	ADC.1	ADC.0	00xx xxxxxB
ADCCON	ADC Control Register	C0H	ADCEN	-	ADCEX	ADCI	ADCS	AADR2	AADR1	AADR0	0x000000B
SADEN	Slave Address Mask	B9H									0000 0000B
IP	Interrupt Priority	B8H	(BF) -	(BE) PADC	(BD) PT2	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	x000 0000B
P7	Port 7	B3H									1111 1111B
P6	Port 6	B2H									1111 1111B
P5	Port 5	B1H									1111 1111B
P3	Port 3	B0H	(B7) RD	(B6) WR	(B5) T1	(B4) T0	(B3) INT1	(B2) INT0	(B1) TXD	(B0) RXD	1111 1111B
SFRCN	F/W Flash Control	AFH	0	WFWIN	NOE	NCE	CTRL3	CTRL2	CTRL1	CTRL0	0011 1111B
SFRFD	F/W Flash Data	AEH									xxxx xxxxxB
SFRAH	F/W Flash High Address	ADH									0000 0000B
SFRAL	F/W Flash Low Address	ACH									0000 0000B
SADDR	Slave Address	A9H									0000 0000B
IE	Interrupt Enable	A8H	(AF) EA	(AE) EADC	(AD) ET2	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	0000 0000B
P4	Port 4	A5H	-	-	-	-					xxxx 1111B

Table 6-4 Special Function Registers, continued

SYMBOL	DEFINITION	ADDRESS	MSB BIT_ADDRESS, SYMBOL LSB								RESET
P4CSIN	P4 CS SIGN	A2H	P43CSINV	P42CSINV	P41CSINV	P40CSINV	-	PWDNH	RMWFP	-	0000 0000B
XRAMAH	RAM High byte Address	A1H	-	-	-	-	-	-	0	0	0000 0000B
P2	Port 2	A0H	(A7) A15	(A6) A14	(A5) A13	(A4) A12	(A3) A11	(A2) A10	(A1) A9	(A0) A8	1111 1111B
CHPCON	On chip Programming Control	9FH	SWRST/REBOOT	-	LD/AP	-	0	0	LDSEL	ENP	0000 0000B
P43AH	HI Addr. Comparator of P4.3	9DH									0000 0000B
P43AL	LO Addr. Comparator of P4.3	9CH									0000 0000B
P42AH	HI Addr. Comparator of P4.2	9BH									0000 0000B
P42AL	LO Addr. Comparator of P4.2	9AH									0000 0000B
SBUF	Serial Buffer	99H									xxxx xxxxxB
SCON	Serial Control	98H	(9F) SM0/FE	(9E) SM1	(9D) SM2	(9C) REN	(9B) TB8	(9A) RB8	(99) TI	(98) RI	0000 0000B
P41AH	HI Addr. Comparator of P4.1	97H									0000 0000B
P41AL	LO Addr. Comparator of P4.1	96H									0000 0000B
P40AH	HI Addr. Comparator of P4.0	95H									0000 0000B
P40AL	LO Addr. Comparator of P4.0	94H									0000 0000B
P4CONB	P4 Control Register	93H	P43FUN1	P43FUN0	P43CMP1	P43CMP0	P42FUN1	P42FUN0	P42CMP1	P42CMP0	0000 0000B
P4CONA	P4 Control Register	92H	P41FUN1	P41FUN0	P41CMP1	P41CMP0	P40FUN1	P40FUN0	P40CMP1	P40CMP0	0000 0000B
P1	Port 1	90H	(97)	(96)	(95)	(94)	(93) TXD_1	(92) RXD_1	(91) T2EX	(90) T2	1111 1111B
CKCON	Clock Control	8EH	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0	0000 0001B
TH1	Timer High 1	8DH									0000 0000B
TH0	Timer High 0	8CH									0000 0000B
TL1	Timer Low 1	8BH									0000 0000B
TL0	Timer Low 0	8AH									0000 0000B
TMOD	Timer Mode	89H	GATE	$C/\overline{T}$	M1	M0	GATE	$C/\overline{T}$	M1	M0	0000 0000B
TCON	Timer Control	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	0000 0000B
PCON	Power Control	87H	SMOD	SMOD0	-	-	GF1	GF0	PD	IDL	00xx 0000B
DPH	Data Pointer High	83H									0000 0000B
DPL	Data Pointer Low	82H									0000 0000B

Table 6-5 Special Function Registers, continued

SYMBOL	DEFINITION	ADDRESS	MSB		BIT_ADDRESS, SYMBOL					LSB	RESET
SP	Stack Pointer	81H									0000 0111B
P0	Port 0	80H	(87)	(86)	(85)	(84)	(83)	(82)	(81)	(80)	1111 1111B

Note: In column **BIT_ADDRESS, SYMBOL**, containing ( ) item means the bit address.

PORT 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

Port 0 is bi-directional I/O port after chip is reset. Besides, it has internal pull-up resisters. This port also provides a multiplexed, low-order address/data bus when the W79E659 accesses external memory.

STACK POINTER

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

The Stack Pointer stores the address in Scratchpad RAM where the stack begins. It always points to the top of the stack.

DATA POINTER LOW

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

This is the low byte of the standard-8051/52, 16-bit data pointer.

DATA POINTER HIGH

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

This is the low byte of the standard-8051/52, 16-bit data pointer.

POWER CONTROL

Bit:	7	6	5	4	3	2	1	0
	SMOD	SMOD0	-	-	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: This bit doubles the serial-port baud rate in modes 1, 2 and 3.
6	SMOD0	0: Disable Framing Error Detection. SCON.7 acts as per the standard 8051/52 function. 1: Enable Framing Error Detection. SCON.7 indicates a Frame Error and acts as the FE flag.
5-4	-	Reserved
3	GF1	General-purpose user flag.
2	GF0	General-purpose user flag.
1	PD	1: Go into POWER DOWN mode. In this mode, all clocks and program execution are stopped.
0	IDL	1: Go into IDLE mode. In this mode, the CPU clock stops, so program execution stops too. However, the clock to the serial port, ADC, PWM timer and interrupt blocks does not stop, so these blocks continue operating.

TIMER CONTROL

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 overflow flag: This bit is set when Timer 1 overflows. It is cleared automatically when the program executes the Timer-1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 run control: This bit turns the Timer 1 on or off by setting TR1 to 1 or 0.
5	TF0	Timer 0 overflow flag: This bit is set when Timer 0 overflows. It is cleared automatically when the program executes the Timer-0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 run control: This bit turns Timer 0 on or off by setting TR0 to 1 or 0.
3	IE1	Interrupt 1 Edge Detect: Set by hardware when an edge / level is detected on $\overline{INT1}$. This bit is cleared by the hardware when the ISR is executed only if the interrupt is edge-triggered. Otherwise, it follows the pin.
2	IT1	Interrupt 1 type control: Specify falling-edge or low-level trigger for $\overline{INT1}$.
1	IE0	Interrupt 0 Edge Detect: Set by hardware when an edge / level is detected on $\overline{INT0}$. This bit is cleared by the hardware when the ISR is executed only if the interrupt is edge-triggered. Otherwise, it follows the pin.
0	IT0	Interrupt 0 type control: Specify falling-edge or low-level trigger for $\overline{INT0}$.

TIMER MODE CONTROL

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
	TIMER1				TIMER0			

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 is set.
6	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.
5	M1	Timer 1 mode select bit 1. See table below.
4	M0	Timer 1 mode select bit 0. See table below.
3	GATE	Gating control: When this bit is set, Timer 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 is set.
2	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the T0 pin.
1	M1	Timer 0 mode select bit 1. See table below.
0	M0	Timer 0 mode select bit 0. See table below.

M1, M0: Mode Select bits:

M1	M0	Mode
0	0	Mode 0: 8-bit timer/counter TLx serves as 5-bit pre-scale.
0	1	Mode 1: 16-bit timer/counter, no pre-scale.
1	0	Mode 2: 8-bit timer/counter with auto-reload from THx
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer-0 control bits. TH0 is an 8-bit timer only controlled by Timer-1 control bits. (Timer 1) Timer/Counter 1 is stopped.

TIMER 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

TL0.7-0 Timer 0 LSB

TIMER 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

TL1.7-0 Timer 1 LSB

TIMER 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

TH0.7-0 Timer 0 MSB

TIMER 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

TH1.7-0 Timer 1 MSB

CLOCK CONTROL

Bit:	7	6	5	4	3	2	1	0
	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0

Mnemonic: CKCON Address: 8Eh

BIT	NAME	FUNCTION
7	WD1	Watchdog Timer mode select bit 1. See table below.
6	WD0	Watchdog Timer mode select bit 0. See table below.
5	T2M	Timer 2 clock select: 1: divide-by-4 clock 0: divide-by-12 clock
4	T1M	Timer 1 clock select: 1: divide-by-4 clock 0: divide-by-12 clock
3	T0M	Timer 0 clock select: 1: divide-by-4 clock 0: divide-by-12 clock

Continued

BIT	NAME	FUNCTION
2	MD2	Stretch MOVX select bit 2: MD2, MD1, and MD0 select the stretch value for the MOVX instruction. The $\overline{RD}$ or $\overline{WR}$ strobe is stretched by the selected interval, which enables the W79E659 to access faster or slower external memory devices or peripherals without the need for external circuits. By default, the stretch value is one. See table below. (Note: When accessing on-chip SRAM, these bits have no effect, and the MOVX instruction always takes two machine cycles.)
1	MD1	Stretch MOVX select bit 1. See MD2.
0	MD0	Stretch MOVX select bit 0. See MD2.

WD1, WD0: Mode Select bits:

These bits determine the time-out periods for the Watchdog Timer. The reset time-out period is 512 clocks more than the interrupt time-out period.

WD1	WD0	INTERRUPT TIME-OUT	RESET TIME-OUT
0	0	2^{17}	2^{17} + 512
0	1	2^{20}	2^{20} + 512
1	0	2^{23}	2^{23} + 512
1	1	2^{26}	2^{26} + 512

MD2, MD1, MD0: Stretch MOVX select bits:

MD2	MD1	MD0	STRETCH VALUE	MOVX DURATION
0	0	0	0	2 machine cycles
0	0	1	1	3 machine cycles *(Default)*
0	1	0	2	4 machine cycles
0	1	1	3	5 machine cycles
1	0	0	4	6 machine cycles
1	0	1	5	7 machine cycles
1	1	0	6	8 machine cycles
1	1	1	7	9 machine cycles

PORT 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7-0: General-purpose digital input port or analog input port AD0~AD7. For digital input, port-read instructions read the port pins, while read-modify-write instructions read the port latch. Additional functions are described below.

	ALTERNATE FUNCTION1	ALTERNATE FUNCTION2	ALTERNATE FUNCTION3
P1.0	T2: External input for Timer/Counter 2	PWM0: PWM output ch0	-
P1.1	T2EX: Timer/Counter 2 Capture/Reload Trigger	PWM1: PWM output ch1	-
P1.2	STADC: External rising edge input to start ADC	PWM2: PWM output ch2	-
P1.3	-	PWM3: PWM output ch3	-
P1.4	-	PWM4: PWM output ch4	ADC0: Analog input0
P1.5	-	PWM5: PWM output ch5	ADC1: Analog input1
P1.6	-	-	ADC2: Analog input2
P1.7	-	-	ADC3: Analog input3

Port 4 Control Register A

Bit:	7	6	5	4	3	2	1	0
	P41M1	P41M0	P41C1	P41C0	P40M1	P40M0	P40C1	P40C0

Mnemonic: P4CONA Address: 92h

Port 4 Control Register B

Bit:	7	6	5	4	3	2	1	0
	P43M1	P43M0	P43C1	P43C0	P42M1	P42M0	P42C1	P42C0

Mnemonic: P4CONB Address: 93h

BIT NAME	FUNCTION
P4xM1, P4xM0	Port 4 alternate modes. =00: Mode 0. P4.x is a general purpose I/O port which is the same as Port 1. =01: Mode 1. P4.x is a Read Strobe signal for chip select purpose. The address range depends on the SFR P4xAH, P4xAL and bits P4xC1, P4xC0. =10: Mode 2. P4.x is a Write Strobe signal for chip select purpose. The address range depends on the SFR P4xAH, P4xAL and bits P4xC1, P4xC0. =11: Mode 3. P4.x is a Read/Write Strobe signal for chip select purpose. The address range depends on the SFR P4xAH, P4xAL and bits P4xC1, P4xC0
P4xC1, P4xC0	Port 4 Chip-select Mode address comparison: =00: Compare the full address (16 bits length) with the base address registers P4xAH and P4xAL. =01: Compare the 15 high bits (A15-A1) of address bus with the base address registers P4xAH and P4xAL. =10: Compare the 14 high bits (A15-A2) of address bus with the base address registers P4xAH and P4xAL. =11: Compare the 8 high bits (A15-A8) of address bus with the base address registers P4xAH and P4xAL.

P4.0 Base Address Low Byte Register

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Mnemonic: P40AL Address: 94h

P4.0 Base Address High Byte Register

Bit:	7	6	5	4	3	2	1	0
	A15	A14	A13	A12	A11	A10	A9	A8

Mnemonic: P40AH Address: 95h

P4.1 Base Address Low Byte Register

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Mnemonic: P41AL Address: 96h

P4.1 Base Address High Byte Register

Bit:	7	6	5	4	3	2	1	0
	A15	A14	A13	A12	A11	A10	A9	A8

Mnemonic: P41AH Address: 97h

Serial Port Control

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial Port mode select bit 0 or Framing Error Flag: This bit is controlled by the SMOD0 bit in the PCON register. (SM0) See table below. (FE) This bit indicates an invalid stop bit. It must be manually cleared by software.
6	SM1	Serial Port mode select bit 1. See table below.
5	SM2	Serial Port Clock or Multi-Processor Communication. (Mode 0) This bit controls the serial port clock. If set to zero, the serial port runs at a divide-by-12 clock of the oscillator. This is compatible with the standard 8051/52. If set to one, the serial clock is a divide-by-4 clock of the oscillator. (Mode 1) If SM2 is set to one, RI is not activated if a valid stop bit is not received. (Modes 2 / 3) This bit enables multi-processor communication. If SM2 is set to one, RI is not activated if RB8, the ninth data bit, is zero.
4	REN	Receive enable: 1: Enable serial reception 0: Disable serial reception
3	TB8	(Modes 2 / 3) This is the 9th bit to transmit. This bit is set by software.

Continued

BIT	NAME	FUNCTION
2	RB8	(Mode 0) No function. (Mode 1) If SM2 = 0, RB8 is the stop bit that was received. (Modes 2 / 3) This is the 9th bit that was received.
1	TI	Transmit interrupt flag: This flag is set by the hardware at the end of the 8th bit in mode 0 or at the beginning of the stop bit in the other modes during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by the hardware at the end of the 8th bit in mode 0 or halfway through the stop bits in the other modes during serial reception. However, SM2 can restrict this behavior. This bit can only be cleared by software.

SM0, SM1: Mode Select bits:

SM0	SM1	MODE	DESCRIPTION	LENGTH	BAUD RATE
0	0	0	Synchronous	8	Tclk divided by 4 or 12
0	1	1	Asynchronous	10	Variable
1	0	2	Asynchronous	11	Tclk divided by 32 or 64
1	1	3	Asynchronous	11	Variable

Serial Data Buffer

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

SBUF.7-0 Serial data is read from or written to this location. It actually consists of two separate 8-bit registers. One is the receive buffer, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

P4.2 Base Address Low Byte Register

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Mnemonic: P42AL Address: 9Ah

P4.2 Base Address High Byte Register

Bit:	7	6	5	4	3	2	1	0
	A15	A14	A13	A12	A11	A10	A9	A8

Mnemonic: P42AH Address: 9Bh

P4.3 Base Address Low Byte Register

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Mnemonic: P43AL Address: 9Ch

P4.3 Base Address High Byte Register

Bit:	7	6	5	4	3	2	1	0
	A15	A14	A13	A12	A11	A10	A9	A8

Mnemonic: P43AH Address: 9Dh

ISP Control Register

Bit:	7	6	5	4	3	2	1	0
	SWRST /HWB	-	LD/AP	-	-	-	LDSEL	ENP

Mnemonic: CHPCON Address: 9Fh

BIT	NAME	FUNCTION
7	W:SWRST R:HWB	Write access to this bit is different from read access. Set this bit to reset the device. This has the same effect as asserting the RST pin. The microcontroller returns to its initial state, and this bit is cleared automatically. Reading this bit indicates whether or not the device is in ISP hardware reboot mode.
6	-	Reserved
5	LD/AP (read-only)	0: CPU is executing AR Flash EPROM 1: CPU is executing LD Flash EPROM
4-2	-	Reserved
1	LDSEL (write-only)	Load ROM Location Selection. This bit should be set before entering ISP mode. 1: Run the program in LD Flash EPROM. 0: Run the program in AP Flash EPROM.
0	ENP	In System Program Enable. 1: Enable in-system programming mode. The erase, program and read operations are executed according to various SFR settings. In this mode, the device runs in IDLE state, so PCON.1 has no effect. 0: Disable in-system programming mode. The device returns to normal operations, and PCON.1 is functional again.

The way to enter ISP mode is to set ENP to 1 and write LDSEL properly then force CPU in IDLE mode, after IDLE mode is released CPU will restart from AP or LD ROM according the value of LDSEL.

PORT 2

Bit:	7	6	5	4	3	2	1	0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

Mnemonic: P2 Address: A0h

P2.7-0: Port 2 is a bi-directional I/O port with internal pull-up resistors. This port also provides the upper address bits for accesses to external memory.

Port 4 Chip-select Polarity

Bit:	7	6	5	4	3	2	1	0
	P43INV	P42INV	P42INV	P40INV	-	PWDNH	RMWFP	-

Mnemonic: P4CSIN Address: A2h

BIT	NAME	FUNCTION
7-4	P4xINV	The Active Polarity of P4.x as P4.x is set as a chip-select strobe output. 1: Active High. 0: Active Low.
3	-	Reserved
2	PWDNH	Set ALE and $\overline{PSEN}$ state in power down mode. 1: ALE and $\overline{PSEN}$ output logic high in power down mode 0: ALE and $\overline{PSEN}$ output logic low in power down mode.
1	RMWFP	Control Read Path of Instruction “Read-Modify-Write”. When this bit is set, the read path of executing “read-modify-write” instruction is from port pin otherwise from SFR.
0	-	Reserved

PORT 4

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	P4.3	P4.2	P4.1	P4.0

Mnemonic: P4 Address: A5h

P4.3-0: Port 4 is a bi-directional I/O port with internal pull-ups.

Interrupt Enable

Bit:	7	6	5	4	3	2	1	0
	EA	EADC	ET2	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

BIT	NAME	FUNCTION
7	EA	Global enable. Enable/disable all interrupts.
6	EADC	Enable ADC interrupt.
5	ET2	Enable Timer 2 interrupt.
4	ES	Enable Serial Port interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt 1.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt 0.

Slave Address

Bit:	7	6	5	4	3	2	1	0
	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0

Mnemonic: SADDR Address: A9h

SADDR The SADDR should be programmed to the given or broadcast address for serial port to which the slave processor is designated.

ISP Address Low Byte

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Mnemonic: SFRAL Address: ACh

Low byte destination address for In System Programming operations.

ISP Address High Byte

Bit:	7	6	5	4	3	2	1	0
	A15	A14	A13	A12	A11	A10	A9	A8

Mnemonic: SFRAH Address: ADh

Low byte destination address for In System Programming operations. (SFRAH, SFRAL) represents the address of the ROM byte that will be erased, programmed or read.

ISP Data Buffer

Bit:	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0

Mnemonic: SFRFD Address: AEh

In ISP mode, read/write a specific byte ROM content must go through SFRFD register.

ISP Operation Modes

Bit:	7	6	5	4	3	2	1	0
		WFWIN	NOE	NCE	CTRL3	CTRL2	CTRL1	CTRL0

Mnemonic: SFRCN Address: AFh

WFWIN On-chip FLASH EPROM bank select for in-system programming.
0= AP FLASH EPROM bank is selected as destination for re-programming.
1= LD FLASH EPROM bank is selected as destination for re-programming.

NOE Flash EPROM output enable.

NCE Flash EPROM chip enable.

CTRL[3:0] The Flash Control Signals.

ISP MODE	BANK	WFWIN	NOE	NCE	CTRL[3:0]	SFRAH, SFRAL	SFRFD
Erase 4KB LD Flash	0	1	1	0	0010	X	X
Erase 32K AP Flash	0	0	1	0	0010	X	X
Program 4KB LD Flash	0	1	1	0	0001	Address in	Data in
Program 32KB AP Flash	0	0	1	0	0001	Address in	Data in
Read 4KB LD Flash	0	1	0	0	0000	Address in	Data out
Read 32KB AP Flash	0	0	0	0	0000	Address in	Data out

PORT 3

Bit:	7	6	5	4	3	2	1	0
	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0

Mnemonic: P3 Address: B0h

P3.7-0: General-purpose I/O port. Each pin also has an alternative input or output function, which is described below.

BIT	NAME	FUNCTION
7	P3.7	$\overline{RD}$: strobe for reading from external RAM
6	P3.6	$\overline{WR}$: strobe for writing to external RAM
5	P3.5	T1: Timer 1 external count input
4	P3.4	T0: Timer 0 external count input
3	P3.3	$\overline{INT1}$: External interrupt 1
2	P3.2	$\overline{INT0}$: External interrupt 0
1	P3.1	TxD: Serial port 0 output
0	P3.0	RxD: Serial port 0 input

PORT 5

Bit:	7	6	5	4	3	2	1	0
	P5.7	P5.6	P5.5	P5.4	P5.3	P5.2	P5.1	P5.0

Mnemonic: P5 Address: B1h

P5.7-0 A bi-directional I/O port with inernal pull-ups. This port is not bit-addressable. The alternate functions of P5.0 to P5.3 are inputs of ADC4 to ADC7.