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1. GENERAL DESCRIPTION

The W79E8213 series are an 8-bit 4T-8051 microcontroller which has Flash EPROM which is programmable by ICP (In Circuit Program) or by hardware writer. The instruction set of the W79E8213 series are fully compatible with the standard 8052. The W79E8213 series contain a 4Kbytes of main Flash EPROM; a 128bytes of RAM; two 16-bit timer/counters; 4-channel 10-bit PWM; 3 edge detector inputs; 8-channel multiplexed 10-bit A/D convert. The W79E8213 series supports 128 bytes NVM Data Flash EPROM. These peripherals are supported by 10 sources four-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W79E8213 series allow the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.



2. FEATURES

- Fully static design 8-bit 4T-8051 CMOS microcontroller:
 - VDD = 4.5V to 5.5V @20MHz
 - VDD = 2.7V to 5.5V @12MHz
 - VDD = 2.4V to 5.5V @4MHz
- Instruction-set compatible with MSC-51.
- Flexible CPU clock source configurable by config bit and software:
 - High speed external oscillator: upto 20MHz Crystal and resonator (enabled by config bit).
 - Internal RC oscillator: 20/10MHz selectable by config bit, only W79E8213R supports $\pm 2\%$ accuracy internal RC oscillator at fixed voltage and temperature condition.
- 4K bytes of AP Flash EPROM, with ICP and external writer programmable mode.
- 128 bytes of on-chip RAM.
- W79E8213 series supports 128 bytes NVM Data Flash EPROM for customer data storage used and 10K writer cycles.
 - 8 pages. Page size is 16 bytes.
- Two 16-bit timer/counters.
- Ten interrupts source with four levels of priority.
- Three-edge detect interrupt inputs.
- Programmable Watchdog Timer.
- Four-channel 10-bit PWM (Pulse Width Modulator).
- Internal square wave generator for buzzer.
- Up to 18 I/O pins.
- The 4 outputs mode and TTL/Schmitt trigger selectable Port.
- LED drive capability on all port pins. Sink 20mA; Drive: -15~-20mA @push-pull mode.
- Eight high sink capability (40mA) port pins.
- Eight-channel multiplexed with 10-bits A/D convert.
- Low Voltage Detect interrupt and reset.
- Development Tools:
 - ICP(In Circuit Programming) writer
- Packages:
 - Lead Free (RoHS) DIP 20: W79E8213AKG
 - Lead Free (RoHS) SOP 20: W79E8213ASG
 - Lead Free (RoHS) DIP 20: W79E8213RAKG
 - Lead Free (RoHS) SOP 20: W79E8213RASG

3. PARTS INFORMATION LIST

3.1 Lead Free (RoHS) Parts information list

PART NO.	EPROM FLASH SIZE	RAM	NVM FLASH EPROM	INTERNAL RC ¹ OSCILLATOR ACCURACY	PACKAGE
W79E8213AKG	4KB	128B	128B	±30%	DIP-20 Pin
W79E8213ASG	4KB	128B	128B	±30%	SOP-20 Pin
W79E8213RAKG	4KB	128B	128B	±2%	DIP-20 Pin
W79E8213RASG	4KB	128B	128B	±2%	SOP-20 Pin

Note: 1. Test conditions are $V_{DD} = 3.3V$, $T_A = 25^{\circ}C$

Table 3-1: Lead Free (RoHS) Parts information list

4. PIN CONFIGURATION

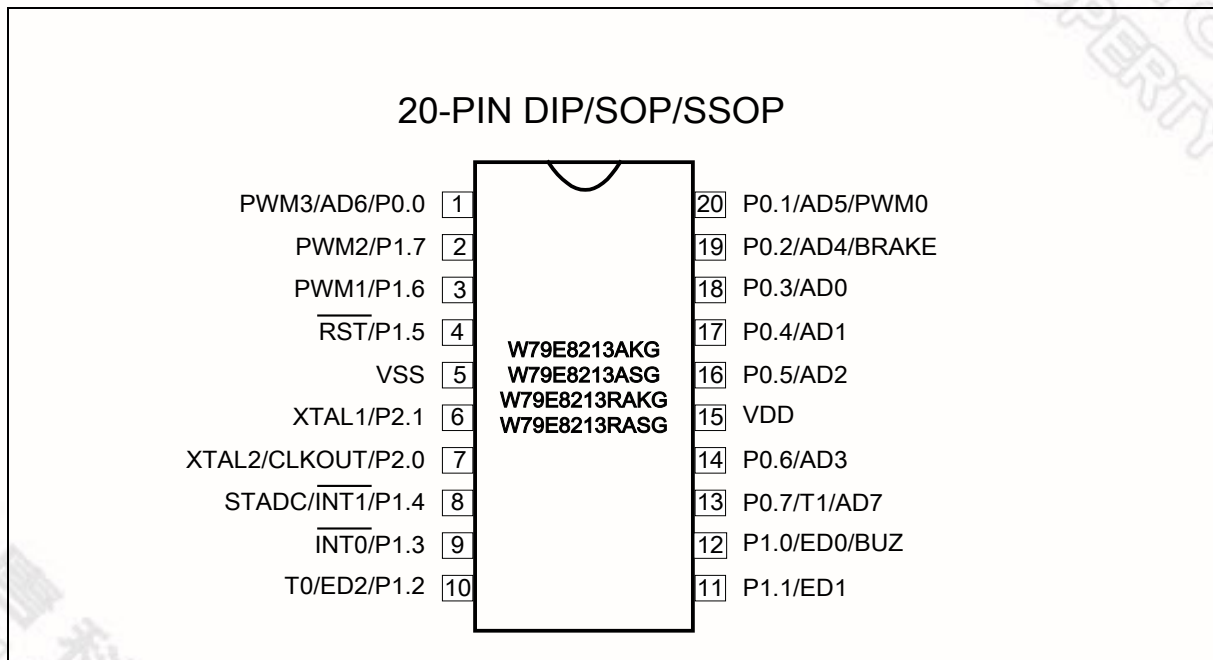


Figure 4-1: Pin Configuration



5. PIN DESCRIPTIONS

SYMBOL	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2	ALTERNATE FUNCTION 3	ALTERNATE FUNCTION 4 (ICP MODE)	TYPE	DESCRIPTION
VDD					P	POWER SUPPLY: Supply voltage for operation.
VSS					P	GROUND: Ground potential.
P0.0	AD6		PWM3		I/O	Port0: Support 4 output modes and TTL/Schmitt trigger. Multifunction pins for T1, PWM0, PWM3, BRAKE, AD0-7, Data and Clock (for ICP).
P0.1	AD5		PWM0		I/O	
P0.2	AD4		BRAKE		I/O	
P0.3	AD0				I/O	
P0.4	AD1			Data	I/O	
P0.5	AD2			Clock	I/O	
P0.6	AD3				I/O	
P0.7	AD7		T1		I/O	
P1.0	BUZ	ED0			I/O	Port1: Support 4 output modes and TTL/Schmitt trigger (except for P1.5 input only).
P1.1		ED1			I/O	
P1.2		ED2	T0		I/O	
P1.3		/INT0			I/O	
P1.4	STADC	/INT1			I/O	Multifunction pins for /RST, T0, /INT0-1, BUZ, PWM1-2, ED0-2, STADC, and HV (for ICP).
P1.5	$\overline{\text{RST}}$			HV	I	
P1.6	PWM1				I/O	
P1.7	PWM2				I/O	P1.0-P1.7 have 40mA high sink capability.
P2.0	XTAL2/CLKOUT				I/O	CRYSTAL2: This is the crystal oscillator output. It is the inversion of XTAL1. Also a configurable i/o pin. When operating as I/O, it supports 4 output modes and TTL/Schmitt trigger.
P2.1	XTAL1				I/O	CRYSTAL1: This is the crystal oscillator input. This pin may be driven by an external clock or configurable I/O pin. When operating as I/O, it supports 4 output modes and TTL/Schmitt trigger.

* **TYPE:** P: power, I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open-drain.

Table 5-1: Pin Description

Note:

On power-on-reset, all port pins will be tri-stated.

After power-on-reset, all port pins state will follow CONFIG0.PRHI bit definition.

6. FUNCTIONAL DESCRIPTION

The W79E8213 series architecture consist of a 4T 8051 core controller surrounded by various registers, 4K bytes Flash EPROM, 128 bytes of RAM, up to 18 general purpose I/O ports, two timer/counters, 3 edge detector inputs, 4-channel PWM with 10-bits counter, 8-channel multiplexed with 10-bit ADC analog input, Flash EPROM program by Writer and ICP. W79E8213 series supported 128 bytes NVM Data Flash EPROM.

6.1 On-Chip Flash EPROM

The W79E8213 series include one 4K bytes of main Flash EPROM for application program. A Writer or ICP programming board is required to program the Flash EPROM or NVM Data Flash EPROM. This ICP (In-Circuit Programming) feature makes the job easy and efficient when the application's firmware needs to be updated frequently. In some applications, the in-circuit programming feature makes it possible for the end-user to easily update the system firmware without opening the chassis.

6.2 I/O Ports

The W79E8213 series have up to 18 I/O pins using internal RC oscillator & /RST is input only by reset options. All ports can be used as four outputs mode when it may set by PxM1.y and PxM2.y SFR's registers, it has strong pull-ups and pull-downs, and does not need any external pull-ups. Otherwise it can be used as general I/O port as open drain circuit. All ports can be used bi-directional and these are as I/O ports. These ports are not true I/O, but rather are pseudo-I/O ports. This is because these ports have strong pull-downs and weak pull-ups.

6.3 Timers

The W79E8213 series have two 16-bit timers that are functionally and similar to the timers of the 8052 family. When used as timers, the user has a choice of 12 or 4 clocks per count that emulates the timing of the original 8052.

6.4 Interrupts

The Interrupt structure in the W79E8213 series is slightly different from that of the standard 8052. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased.

6.5 Data Pointer

The data pointer of W79E8213 series is same as standard 8052 which have 16-bit Data Pointer (DPTR).

6.6 Architecture

The W79E8213 series are based on the standard 8052 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard 8052 instruction set.

6.6.1 ALU

The ALU is the heart of the W79E8213 series. It is responsible for the arithmetic and logical functions. It is also used in decision making, in case of jump instructions, and is also used in calculating jump addresses. The user cannot directly use the ALU, but the Instruction Decoder reads the op-code,

decodes it, and sequences the data through the ALU and its associated registers to generate the required result. The ALU mainly uses the ACC which is a special function register (SFR) on the chip. Another SFR, namely B register is also used in Multiply and Divide instructions. The ALU generates several status signals which are stored in the Program Status Word register (PSW).

6.6.2 Accumulator

The Accumulator (ACC) is the primary register used in arithmetic, logical and data transfer operations in the W79E8213 series. Since the Accumulator is directly accessible by the CPU, most of the high speed instructions make use of the ACC as one argument.

6.6.3 B Register

This is an 8-bit register that is used as the second argument in the MUL and DIV instructions. For all other instructions it can be used simply as a general purpose register.

6.6.4 Program Status Word

This is an 8-bit SFR that is used to store the status bits of the ALU. It holds the Carry flag, the Auxiliary Carry flag, General purpose flags, the Register Bank Select, the Overflow flag, and the Parity flag.

6.6.5 Scratch-pad RAM

The W79E8213 series have a 128 bytes on-chip scratch-pad RAM. These can be used by the user for temporary storage during program execution. A certain section of this RAM is bit addressable, and can be directly addressed for this purpose.

6.6.6 Stack Pointer

The W79E8213 series have an 8-bit Stack Pointer which points to the top of the Stack. This stack resides in the Scratch Pad RAM in the W79E8213 series. Hence the size of the stack is limited by the size of this RAM.

6.7 Power Management

Power Management like the standard 8052, the W79E8213 series also have the IDLE and POWER DOWN modes of operation. In the IDLE mode, the clock to the CPU is stopped while the timers, serial ports and interrupt block continue to operate. In the POWER DOWN mode, all clocks are stopped and the chip operation is completely stopped. This is the lowest power consumption state.

7. MEMORY ORGANIZATION

The W79E8213 series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

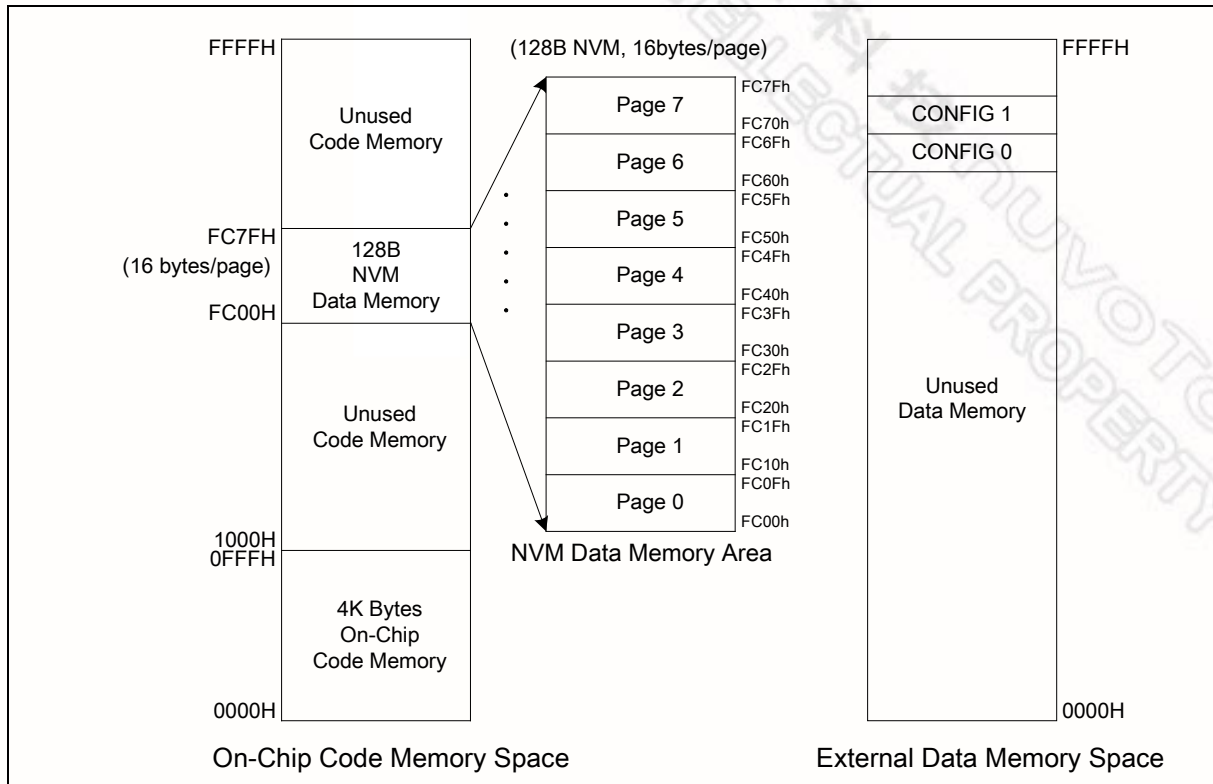


Figure 7-1: W79E8213 series memory map

7.1 Program Memory (on-chip Flash)

The Program Memory on the W79E8213 series can be up to 4K bytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

7.2 Data Flash Memory

The NVM Data Memory of Flash EPROM on the W79E8213 series is 128 bytes long, with page size of 16 bytes, respectively. The W79E8213 series' NVM size is controllable through CONFIG1 register. The W79E8213 series read the content of data memory by using "MOVC A, @A+DPTR". To write data is by NVMADDR, NVMDATA and NVMCON SFR's registers.

7.3 Data Memory (accessed by MOVX)

Not available in this product series.

7.4 Scratch-pad RAM and Register Map

As mentioned before the W79E8213 series have separate Program and Data Memory areas. The on-chip 128 bytes scratch pad RAM is in addition to the external memory. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.

FFH	Unused Indirect RAM	SFR Direct Addressing Only
80H 7FH 00H	Direct & Indirect RAM Addressing	

Figure 7-2: W79E8213 RAM and SFR memory map

Since the scratch-pad RAM is only 128 bytes it can be used only when data contents are small. There are several other special purpose areas within the scratch-pad RAM. These are described as following.

FFH	Indirect RAM							
80H 7FH								
Direct RAM								
30H								
2FH	7F	7E	7D	7C	7B	7A	79	78
2EH	77	76	75	74	73	72	71	70
2DH	6F	6E	6D	6C	6B	6A	69	68
2CH	67	66	65	64	63	62	61	60
2BH	5F	5E	5D	5C	5B	5A	59	58
2AH	57	56	55	54	53	52	51	50
29H	4F	4E	4D	4C	4B	4A	49	48
28H	47	46	45	44	43	42	41	40
27H	3F	3E	3D	3C	3B	3A	39	38
26H	37	36	35	34	33	32	31	30
25H	2F	2E	2D	2C	2B	2A	29	28
24H	27	26	25	24	23	22	21	20
23H	1F	1E	1D	1C	1B	1A	19	18
22H	17	16	15	14	13	12	11	10
21H	0F	0E	0D	0C	0B	0A	09	08
20H	07	06	05	04	03	02	01	00
1FH	Bank 3							
18H 17H	Bank 2							
10H 0FH	Bank 1							
08H 07H	Bank 0							
00H								

Figure 7-3: Scratch pad RAM

7.4.1 Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed as Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at one time the W79E8213 series can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

7.4.2 Bit addressable Locations

The Scratch-pad RAM area from location 20h to 2Fh is byte as well as bit addressable. This means that a bit in this area can be individually addressed. In addition some of the SFRs are also bit addressable. The instruction decoder is able to distinguish a bit access from a byte access by the type of the instruction itself. In the SFR area, any existing SFR whose address ends in a 0 or 8 is bit addressable.

7.4.3 Stack

The scratch-pad RAM can be used for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a jump, call or interrupt is invoked the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07h at reset. The user can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, and then the SP is decreased.



8. SPECIAL FUNCTION REGISTERS

The W79E8213 series uses Special Function Registers (SFRs) to control and monitor peripherals and their Modes. The SFRs reside in the register locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where users wish to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. The W79E8213 series contain all the SFRs present in the standard 8052. However some additional SFRs are added. In some cases the unused bits in the original 8052, have been given new functions. The list of the SFRs is as following.

F8	IP1	BUZCON						
F0	B						PADIDS	IP1H
E8	EIE							
E0	ACC	ADCCON	ADCH	ADCCON1				
D8	WDCON	PWMPL	PWM0L	PWM1L	PWMCON1	PWM2L	PWM3L	PWMCON2
D0	PSW	PWMPH	PWM0H	PWM1H		PWM2H	PWM3H	PWMCON3
C8							NVMCON	NVMDATA
C0							NVMADDR1	TA
B8	IP0							
B0		P0M1	P0M2	P1M1	P1M2	P2M1	P2M2	IP0H
A8	IE							
A0	P2		AUXR1	EDIC				
98								
90	P1							
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	
80	P0	SP	DPL	DPH				PCON

Table 8-1: Special Function Register Location Table

- Note:**
1. The SFRs in the column with dark borders are bit-addressable
 2. The table is condensed with eight locations per row. Empty locations indicate that these are no registers at these addresses. When a bit or register is not implemented, it will read high.

W79E8213/W79E8213R Data Sheet



SYMBOL	DEFINITION	ADD RESS	BIT_ADDRESS, SYMBOL								RESET
			MSB	LSB							
BUZCON	Square wave control register	F9H	-	-	BUZDIV. 5	BUZDIV. 4	BUZDIV. 3	BUZDIV. 2	BUZDIV. 1	BUZDIV. 0	xx00 0000B
IP1	Interrupt priority 1	F8H	(FF) PED	(FE) PPWM	(FD) PBK	(FC) PWDI	(FB) -	(FA) -	(F9) -	(F8) -	0000xxxxB
IP1H	Interrupt high priority 1	F7H	PEDH	PPWMH	PBKH	PWDIH	-	-	-	-	0000xxxxB
PADIDS	Port ADC digital input disable	F6H									00000000B
B	B register	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	00000000B
EIE	Interrupt enable 1	E8H	(EF) EED	(EE) EPWMU F	(ED) EPWM	(EC) EWDI	(EB) -	(EA) -	(E9) -	(E8) -	0000xxxxB
ADCCON1	ADC control register 1	E3H	ADCLK. 1	ADCLK. 0	-	-	-	AADR2	-	-	10xxx0xxB
ADCH	ADC converter result high register	E2H	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2	00000000B
ADCCON	ADC control register	E1H	ADC.1	ADC.0	ADCEX	ADCI	ADCS	RCCLK	AADR1	AADR0	00000000B
ACC	Accumulator	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	00000000B
PWMCON2	PWM control register 2	DFH	BKCH	BKPS	BPEN	BKEN	PWM3B	PWM2B	PWM1B	PWM0B	00000000B
PWM3L	PWM 3 low bits register	DEH	PWM3.7	PWM3.6	PWM3.5	PWM3.4	PWM3.3	PWM3.2	PWM3.1	PWM3.0	00000000B
PWM2L	PWM 2 low bits register	DDH	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0	00000000B
PWMCON1	PWM control register 1	DCH	PWMRU N	load	PWMF	CLRPW M	PWM3I	PWM2I	PWM1I	PWM0I	00000000B
PWM1L	PWM 1 low bits register	DBH	PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0	00000000B
PWM0L	PWM 0 low bits register	DAH	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0	00000000B
PWMP0L	PWM counter low register	D9H	PWMP0. 7	PWMP0. 6	PWMP0. 5	PWMP0. 4	PWMP0. 3	PWMP0. 2	PWMP0. 1	PWMP0. 0	00000000B
WDCON	Watch-Dog control	D8H	(DF) WDRUN	(DE) -	(DD) WD1	(DC) WD0	(DB) WDIF	(DA) WTRF	(D9) EWRST	(D8) WDCLR	External reset: 0x00 0000B Watchdog reset: 0x00 0100B Power on reset 0x000000B
PWMCON3	PWM control register 3	D7H	-	-	-	-	FP1	FP0	-	BKF	xxxx00x0B
PWM3H	PWM 3 high bits register	D6H	-	-	-	-	-	-	PWM3.9	PWM3.8	xxxxxx00B
PWM2H	PWM 2 high bits register	D5H	-	-	-	-	-	-	PWM2.9	PWM2.8	xxxxxx00B
PWM1H	PWM 1 high bits register	D3H	-	-	-	-	-	-	PWM1.9	PWM1.8	xxxxxx00B
PWM0H	PWM 0 high bits register	D2H	-	-	-	-	-	-	PWM0.9	PWM0.8	xxxxxx00B
PWMPH	PWM counter high register	D1H	-	-	-	-	-	-	PWMP0. 9	PWMP0. 8	00000000B
PSW	Program status word	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P	00000000B
NVMDATA	NVM Data	CFH									00000000B
NVMCON	NVM Control	CEH	EER	EWR	-	-	-	-	-	-	00xxxxxB
TA	Timed Access Protection	C7H	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0	11111111B
NVMADDR0L	NVM low byte address	C6H	-	NVMAD DR.6	NVMAD DR.5	NVMAD DR.4	NVMAD DR.3	NVMAD DR.2	NVMAD DR.1	NVMAD DR.0	00000000B
IP0	Interrupt priority	B8H	(BF) -	(BE) PADC	(BD) PBO	(BC) -	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	x00x0000B

W79E8213/W79E8213R Data Sheet



Continued

SYMBOL	DEFINITION	ADD RESS	BIT_ADDRESS, SYMBOL								RESET
			MSB LSB								
IP0H	Interrupt high priority	B7H	-	PADCH	PBOH	-	PT1H	PX1H	PT0H	PX0H	x00x0000B
P2M2	Port 2 output mode 2	B6H	-	-	-	-	-	-	P2M2.1	P2M2.0	xxxxxx 00B
P2M1	Port 2 output mode 1	B5H	P2S	P1S	P0S	ENCLK	T1OE	T0OE	P2M2.1	P2M2.0	00000000B
P1M2	Port 1 output mode 2	B4H	P1M2.7	P1M2.6	-	P1M2.4	P1M2.3	P1M2.2	P1M2.1	P1M2.0	00x00000B
P1M1	Port 1 output mode 1	B3H	P1M1.7	P1M1.6	-	P1M1.4	P1M1.3	P1M1.2	P1M1.1	P1M1.0	00x00000B
P0M2	Port 0 output mode 2	B2H	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0	00000000B
P0M1	Port 0 output mode 1	B1H	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0	00000000B
IE	Interrupt enable	A8H	(AF) EA	(AE) EADC	(AD) EBO	(AC) -	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	000x0000B
EDIC	Edge detect control register	A3H	EDFLT.1	EDFLT.0	ED2TRG	ED2EN	ED1TRG	ED1EN	ED0TRG	ED0EN	00000000B
AUXR1	AUX function register	A2H	EDF	BOD	BOI	LPBOV	SRST	ADCEN	BUZE	-	000X000xB
P2	Port 2	A0H	(A7) -	(A6) -	(A5) -	(A4) -	(A3)	(A2)	(A1) P2.1 XTAL1	(A0) P2.0 XTAL2 CLKOUT	xxxxxxxxxB
P1	Port 1	90H	(97) P1.7 PWM2	(96) P1.6 PWM1	(95) P1.5 /RST	(94) P1.4 /INT1 STADC	(93) P1.3 /INT0	(92) P1.2 ED2 T0	(91) P1.1 ED1	(90) P1.0 ED0 BUZ	11111111B
CKCON	Clock control	8EH	-	-	-	T1M	T0M	-	-	-	xxx00xxxB
TH1	Timer high 1	8DH									00000000B
TH0	Timer high 0	8CH									00000000B
TL1	Timer low 1	8BH									00000000B
TL0	Timer low 0	8AH									00000000B
TMOD	Timer mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00000000B
TCON	Timer control	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	00000000B
PCON	Power control	87H	-	-	BOF	POR	GF1	GF0	PD	IDL	xxxx0000B
DPH	Data pointer high	83H									00000000B
DPL	Data pointer low	82H									00000000B
SP	Stack pointer	81H									00000111B
P0	Port 0	80H	(87) P0.7 AD7 T1	(86) P0.6 AD3	(85) P0.5 AD2	(84) P0.4 AD1	(83) P0.3 AD0	(82) P0.2 AD4 BRAKE	(81) P0.1 AD5 PWM0	(80) P0.0 AD6 PWM3	11111111B

Table 8-2: Special Function Registers

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PORT 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0

Address: 80h

P0.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
7	P0.7	AD7 pin or Timer 1 pin by alternative.
6	P0.6	AD3 pin by alternative.
5	P0.5	AD2 pin by alternative.
4	P0.4	AD1 pin by alternative.
3	P0.3	AD0 pin by alternative.
2	P0.2	AD4 pin or BRAKE pin by alternative.
1	P0.1	AD5 pin or PWM0 pin by alternative.
0	P0.0	AD6 pin or PWM3 pin by alternative.

Note: During power-on-reset, the port pins are tri-stated. After power-on-reset, the value of the port is set by CONFIG0.PRHI bit. The default setting for CONFIG0.PRHI =1 which the alternative function output is turned on upon reset. If CONFIG0.PRHI is set to 0, the user has to write a 1 to port SFR to turn on the alternative function output.

STACK POINTER

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP

Address: 81h

BIT	NAME	FUNCTION
7-0	SP.[7:0]	The Stack Pointer stores the Scratch-pad RAM address where the stack begins. In other words it always points to the top of the stack.

DATA POINTER LOW

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL

Address: 82h

BIT	NAME	FUNCTION
7-0	DPL.[7:0]	This is the low byte of the standard 8052 16-bit data pointer.

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DATA POINTER HIGH

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH

Address: 83h

BIT	NAME	FUNCTION
7-0	DPH.[7:0]	This is the high byte of the standard 8052 16-bit data pointer. This is the high byte of the DPTR 16-bit data pointer.

POWER CONTROL

Bit:	7	6	5	4	3	2	1	0
	-	-	BOF	POR	GF1	GF0	PD	IDL

Mnemonic: PCON

Address: 87h

BIT	NAME	FUNCTION
7	-	Reserved.
6	-	Reserved.
5	BOF	0: Cleared by software. 1: Set automatically when a brownout reset or interrupt has occurred. Also set at power on.
4	POR	0: Cleared by software. 1: Set automatically when a power-on reset has occurred.
3	GF1	General purpose user flags.
2	GF0	General purpose user flags.
1	PD	1: The CPU goes into the POWER DOWN mode. In this mode, all the clocks are stopped and program execution is frozen.
0	IDL	1: The CPU goes into the IDLE mode. In this mode, the clocks CPU clock stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating.

TIMER CONTROL

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON

Address: 88h



BIT	NAME	FUNCTION
7	TF1	Timer 1 Overflow Flag. This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
5	TF0	Timer 0 Overflow Flag. This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
3	IE1	Interrupt 1 Edge Detect Flag: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
2	IT1	Interrupt 1 Type Control. Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect Flag. Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
0	IT0	Interrupt 0 Type Control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL

Bit:	7	6	5	4	3	2	1	0
	GATE	C/ \overline{T}	M1	M0	GATE	C/ \overline{T}	M1	M0
	TIMER1				TIMER0			

Mnemonic: TMOD

Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 control bit is set.
6	C/ \overline{T}	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.
5	M1	Timer 1 mode select bit 1. See table below.
4	M0	Timer 1 mode select bit 0. See table below.
3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 control bit is set.
2	C/ \overline{T}	Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the T0 pin.
1	M1	Timer 0 mode select bit 1. See table below.
0	M0	Timer 0 mode select bit 0. See table below.

M1, M0: Mode Select bits:

M1	M0	MODE
0	0	Mode 0: 13-bits timer/counter; THx 8 bits and TLx 5 bits which serve as pre-scalar.



0	1	Mode 1: 16-bit timer/counter, no pre-scale.
1	0	Mode 2: 8-bit timer/counter with auto-reload from THx.
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer0 control bits. TH0 is an 8-bit timer only controlled by Timer1 control bits. (Timer 1) Timer/Counter 1 is stopped.

TIMER 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0

Address: 8Ah

BIT	NAME	FUNCTION
7-0	TL0.[7:0]	Timer 0 LSB.

TIMER 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1

Address: 8Bh

BIT	NAME	FUNCTION
7-0	TL1.[7:0]	Timer 1 LSB.

TIMER 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0

Address: 8Ch

BIT	NAME	FUNCTION
7-0	TH0.[7:0]	Timer 0 MSB.

TIMER 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1

Address: 8Dh

BIT	NAME	FUNCTION
7-0	TH1.[7:0]	Timer 1 MSB.

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CLOCK CONTROL

Bit:	7	6	5	4	3	2	1	0
	-	-	-	T1M	T0M	-	-	-

Mnemonic: CKCON

Address: 8Eh

BIT	NAME	FUNCTION
7-5	-	Reserved.
4	T1M	Timer 1 clock select: 0: Timer 1 uses a divide by 12 clocks. 1: Timer 1 uses a divide by 4 clocks.
3	T0M	Timer 0 clock select: 0: Timer 0 uses a divide by 12 clocks. 1: Timer 0 uses a divide by 4 clocks.
2-0	-	Reserved.

PORT 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1

Address: 90h

P1.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
7	P1.7	PWM2 pin by alternative.
6	P1.6	PWM1 pin by alternative.
5	P1.5	/RST pin or input pin by alternative.
4	P1.4	STADC pin or /INT1 interrupt pin by alternative.
3	P1.3	/INT0 interrupt pin by alternative.
2	P1.2	Timer 0 pin or ED2 pin by alternative.
1	P1.1	ED1 pin by alternative.
0	P1.0	BUZ pin or ED0 pin by alternative.

Note: During power-on-reset, the port pins are tri-stated. After power-on-reset, the value of the port is set by CONFIG0.PRHI bit. The default setting for CONFIG0.PRHI =1 which the alternative function output is turned on upon reset. If CONFIG0.PRHI is set to 0, the user has to write a 1 to port SFR to turn on the alternative function output.

PORT 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	P2.1	P2.0

Mnemonic: P2

Address: A0h

BIT	NAME	FUNCTION
7-2	-	Reserved.

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1	P2.1	XTAL1 clock input pin.
0	P2.0	XTAL2 or CLKOUT pin by alternative.

Note: During power-on-reset, the port pins are tri-stated. After power-on-reset, the value of the port is set by CONFIG0.PRHI bit. The default setting for CONFIG0.PRHI =1 which the alternative function output is turned on upon reset. If CONFIG0.PRHI is set to 0, the user has to write a 1 to port SFR to turn on the alternative function output.

AUX FUNCTION REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	EDF	BOD	BOI	LPBOV	SRST	ADCEN	BUZE	-

Mnemonic: AUXR1

Address: A2h

BIT	NAME	FUNCTION
7	EDF	Edge detect Interrupt Flag: 1: When any pin of port 1.0-1.2 that is enabled for the Edge Detect Interrupt function trigger (falling/rising edge trigger configurable). Must be cleared by software.
6	BOD	Brown Out Disable: 0: Enable Brownout Detect function. 1: Disable Brownout Detect function and save power.
5	BOI	Brown Out Interrupt: 0: Disable Brownout Detect Interrupt function and it will cause chip reset when BOF is set. 1: This prevents Brownout Detection from causing a chip reset and allows the Brownout Detect function to be used as an interrupt.
4	LPBOV	Low Power Brown Out Detect control: 0: When BOD is enable, the Brown Out detect is always turned on by normal run or Power-down mode. 1: When BOD is enable, the Brown Out detect circuit is turned on by Power-down mode. This control can help save 15/16 of the Brownout circuit power. When uC is in Power-down mode, the BOD will enable internal RC OSC (600KHz+/- 50%)
3	SRST	Software reset: 1: reset the chip as if a hardware reset occurred.
2	ADCEN	0: Disable ADC circuit. 1: Enable ADC circuit.
1	BUZE	Square-wave enable bit: 0: Disable square wave output. 1: The square wave is output to the BUZ (P1.0) pin.
0	-	Reserved.

EDGE DETECT CONTROL REGISTER

Bit:	7	6	5	4	3	2	1	0
	EDFILT.1	EDFILT.0	ED2TRG	ED2EN	ED1TRG	ED1EN	ED0TRG	ED0EN

Mnemonic: EDIC

Address: A3h

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BIT	NAME	FUNCTION
7-6		Edge detect filter type bits: 00 – Filter clock = Fosc. 01 – Filter clock = Fosc/2. 10 – Filter clock = Fosc/4. 11 – Filter clock = Fosc/8.
5	ED2TRG	Edge detect 2 (ED2) trigger type bit: 0 – Falling edge on ED2 pin will cause EDF to be set (if ED2EN is enabled). 1 – Either falling or rising edge on ED2 pin will cause EDF to be set (if ED2EN is enabled).
4	ED2EN	Edge detect 2 (ED2) enable bit: 0 – Disabled. 1 – Enable ED2 (P1.2 pin) as a cause of an edge detect interrupt.
3	ED1TRG	Edge detect 1 (ED1) trigger type bit: 0 – Falling edge on ED1 pin will cause EDF to be set (if ED1EN is enabled). 1 – Either falling or rising edge on ED1 pin will cause EDF to be set (if ED1EN is enabled).
2	ED1EN	Edge detect 1 (ED1) enable bit: 0 – Disabled. 1 – Enable ED1 (P1.1 pin) as a cause of an edge detect interrupt.
1	ED0TRG	Edge detect 0 (ED0) trigger type bit: 0 – Falling edge on ED0 pin will cause EDF to be set (if ED0EN is enabled). 1 – Either falling or rising edge on ED0 pin will cause EDF to be set (if ED0EN is enabled).
0	ED0EN	Edge detect 0 (ED0) enable bit: 0 – Disabled. 1 – Enable ED0 (P1.0 pin) as a cause of an edge detect interrupt.

INTERRUPT ENABLE

Bit:	7	6	5	4	3	2	1	0
	EA	EADC	EBO	-	ET1	EX1	ET0	EX0

Mnemonic: IE

Address: A8h



BIT	NAME	FUNCTION
7	EA	Global enable. Enable/Disable all interrupts.
6	EADC	Enable ADC interrupt.
5	EBO	Enable Brown Out interrupt.
4	-	Reserved.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt 1.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt 0.

PORT 0 OUTPUT MODE 1

Bit:	7	6	5	4	3	2	1	0
	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0

Mnemonic: P0M1

Address: B1h

BIT	NAME	FUNCTION
7-0	P0M1.[7:0]	To control the output configuration of P0 bits [7:0]

PORT 0 OUTPUT MODE 2

Bit:	7	6	5	4	3	2	1	0
	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0

Mnemonic: P0M2

Address: B2h

BIT	NAME	FUNCTION
7-0	P0M2.[7:0]	To control the output configuration of P0 bits [7:0]

PORT 1 OUTPUT MODE 1

Bit:	7	6	5	4	3	2	1	0
	P1M1.7	P1M1.6	-	P1M1.4	P1M1.3	P1M1.2	P1M1.1	P1M1.0

Mnemonic: P1M1

Address: B3h

BIT	NAME	FUNCTION
7-0	P1M1.[7:0]	To control the output configuration of P1 bits [7:0]

PORT 1 OUTPUT MODE 2

Bit:	7	6	5	4	3	2	1	0
	P1M2.7	P1M2.6	-	P1M2.4	P1M2.3	P1M2.2	P1M2.1	P1M2.0

Mnemonic: P1M2

Address: B4h

BIT	NAME	FUNCTION
7-0	P1M2.[7:0]	To control the output configuration of P1 bits [7:0]

PORT 2 OUTPUT MODE 1

Bit:	7	6	5	4	3	2	1	0
------	---	---	---	---	---	---	---	---

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P2S	P1S	P0S	ENCLK	T1OE	T0OE	P2M1.1	P2M1.0
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Mnemonic: P2M1

Address: B5h

BIT	NAME	FUNCTION
7	P2S	0: Disable Schmitt trigger inputs on port 2 and enable TTL inputs on port 2. 1: Enables Schmitt trigger inputs on Port 2.
6	P1S	0: Disable Schmitt trigger inputs on port 1 and enable TTL inputs on port 1. 1: Enables Schmitt trigger inputs on Port 1.
5	P0S	0: Disable Schmitt trigger inputs on port 0 and enable TTL inputs on port 0 1: Enables Schmitt trigger inputs on Port 0.
4	ENCLK	1: Enabled clock output to XTAL2 pin (P2.0).
3	T1OE	1: The P0.7 pin is toggled whenever Timer 1 overflows. The output frequency is therefore one half of the Timer 1 overflow rate.
2	T0OE	1: The P1.2 pin is toggled whenever Timer 0 overflows. The output frequency is therefore one half of the Timer 0 overflow rate.
1	P2M1.1	To control the output configuration of P2.1.
0	P2M1.0	To control the output configuration of P2.0.

PORT 2 OUTPUT MODE 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	P2M2.1	P2M2.0

Mnemonic: P2M2

Address: B6h

BIT	NAME	FUNCTION
7-2	-	Reserved.
1-0	P2M2.[1:0]	To control the output configuration of P2 bits [1:0]

Port Output Configuration Settings:

PXM1.Y (SEE NOTE)	PXM2.Y	PORT INPUT/OUTPUT MODE
0	0	Quasi-bidirectional
0	1	Push-Pull
1	0	Input Only (High Impedance) P2M1.PxS=0, TTL input P2M1.PxS=1, Schmitt input
1	1	Open Drain