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Winbond Electronics Corp.

8-BIT MICROCONTROLLER

Table of Contents-

1. GENERAL DESCRIPTION

The W79E82X series are an 8-bit Turbo 51 microcontroller which has an in-system programmable Flash EPROM which Flash EPROM can program by ICP (In Circuit Program) or by writer. The instruction set of the W79E82X series are fully compatible with the standard 8052. The W79E82X series contain a **16K/8K/4K/2K/1K** bytes of main Flash EPROM; a **256/128** bytes of RAM; **256/128** bytes NVM Data Flash EPROM; two 8-bit bi-directional, one 2-bit bi-directional and bit-addressable I/O ports; two 16-bit timer/counters; 4-channel multiplexed 10-bit A/D convert; 4-channel 10-bit PWM; two serial ports that include a I2C and an enhanced full duplex serial port. These peripherals are supported by 13 sources four-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W79E82X series allow the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

2. FEATURES

- Fully static design 8-bit Turbo 51 CMOS microcontroller up to 20MHz when VDD=4.5V to 5.5V, 12MHz when VDD=2.7V to 5.5V
- **16K/8K/4K/2K/1K** bytes of AP Flash ROM, with ICP and external writer programmable mode.
- **256/128** bytes of on-chip RAM
- **256/128** bytes NVM Data Flash EPROM for customer data storage used and 10K writer cycles
- Instruction-set compatible with MSC-51
- Two 8-bit bi-directional and one 2-bit bi-directional ports
- Two 16-bit timer/counters
- 13 interrupts source with four levels of priority
- One enhanced full duplex serial port with framing error detection and automatic address recognition
- The 4 outputs mode and TTL/Schmitt trigger selectable Port
- Programmable Watchdog Timer
- Four -channel 10-bit PWM (Pulse Width Modulator)
- Four-channel multiplexed with 10-bits A/D convert
- One I2C communication port (Master / Slave)
- Eight keypad interrupt inputs
- Two analog comparators
- Configurable on-chip oscillator
- LED drive capability (20mA) on all port pins
- Low Voltage Detect interrupt and reset
- Development Tools:
  - JTAG ICE(In Circuit Emulation) tool
  - ICP(In Circuit Programming) writer
- Packages:
  - Lead Free (RoHS) DIP 20: W79E825ADG

- Lead Free (RoHS) SOP 20: W79E825ASG
- Lead Free (RoHS) DIP 20: W79E824ADG
- Lead Free (RoHS) SOP 20: W79E824ASG
- Lead Free (RoHS) DIP 20: W79E823ADG
- Lead Free (RoHS) SOP 20: W79E823ASG
- Lead Free (RoHS) DIP 20: W79E822ADG
- Lead Free (RoHS) SOP 20: W79E822ASG
- Lead Free (RoHS) DIP 20: W79E821ADG
- Lead Free (RoHS) SOP 20: W79E821ASG

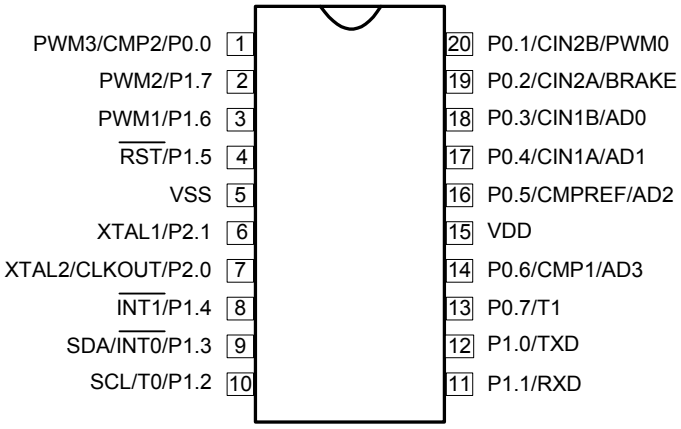
3. PARTS INFORMATION LIST

3.1 Lead Free (RoHS) Parts information list

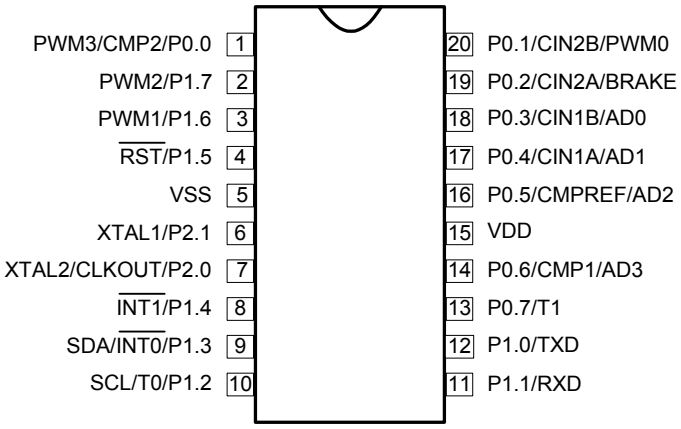
PART NO.	EPROM FLASH SIZE	RAM	NVM FLASH EPROM	ADC	PWM	PACKAGE	REMARK
W79E825ADG	16KB	256B	256B	4x10Bit	4x10Bit	DIP-20 Pin	
W79E825ASG	16KB	256B	256B	4x10Bit	4x10Bit	SOP-20 Pin	
W79E824ADG	8KB	256B	256B	4x10Bit	4x10Bit	DIP-20 Pin	
W79E824ASG	8KB	256B	256B	4x10Bit	4x10Bit	SOP-20 Pin	
W79E823ADG	4KB	128B	128B	4x10Bit	4x10Bit	DIP-20 Pin	
W79E823ASG	4KB	128B	128B	4x10Bit	4x10Bit	SOP-20 Pin	
W79E822ADG	2KB	128B	128B	4x10Bit	4x10Bit	DIP-20 Pin	
W79E822ASG	2KB	128B	128B	4x10Bit	4x10Bit	SOP-20 Pin	
W79E821ADG	1KB	128B	128B	4x10Bit	4x10Bit	DIP-20 Pin	
W79E821ASG	1KB	128B	128B	4x10Bit	4x10Bit	SOP-20 Pin	

4. PIN CONFIGURATION

20 PIN DIP



20 PIN SOP



5. PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTIONS
$\overline{\text{RST}}$ (P1.5)	I	RESET: A low on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1(P2.1)	I/O	CRYSTAL1: This is the crystal oscillator input. This pin may be driven by an external clock or configurable I/O pin.
XTAL2(P2.0)	I/O	CRYSTAL2: This is the crystal oscillator output. It is the inversion of XTAL1 or configurable I/O pin.
VSS	P	GROUND: Ground potential
VDD	P	POWER: SUPPLY: Supply voltage for operation.
P0.0–P0.7	I/O	PORT 0: Port 0 is four mode output pin and two mode input. The P0.3~P0.6 are 4-channel input ports (ADC0-ADC3) for ADC used.
P1.0–P1.7	I/O	PORT 1: Port 1 is four mode output pin and two mode input. The P1.2(SCL) and P1.3(SDA) is only open drain circuit, and P1.5 only input pin.

* **TYPE:** P: power, I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open-drain.

6. FUNCTIONAL DESCRIPTION

The W79E82X series architecture consist of a 4T 8051 core controller surrounded by various registers, **16K/8K/4K/2K/1K** bytes Flash EPROM, **256/128** bytes of RAM, **256/128** bytes NVM Data Flash EPROM, three general purpose I/O ports, two timer/counters, one serial port, one I2C serial I/O, 4 channel PWM with 10-bit counter, 4-channel multiplexed with 10-bit ADC analog input, Flash EPROM program by Writer and ICP.

6.1 On-Chip Flash EPROM

The W79E82X series include one **16K/8K/4K/2K/1K** bytes of main Flash EPROM for application program when operating the in-circuit programming features by the Flash EPROM itself which need Writer or ICP program board to program the Flash EPROM. This ICP(In-Circuit Programming) feature makes the job easy and efficient in which the application needs to update firmware frequently. In some applications, the in-circuit programming feature makes it possible that the end-user is able to easily update the system firmware by themselves without opening the chassis.

6.2 I/O Ports

The W79E82X series have two 8-bit and one 2-bit port, up to 18 I/O pins using on-chip oscillator & /RST is input only by reset options. All ports can be used as four outputs mode when it may set by PxM1.y and PxM2.y registers, it has strong pull-ups and pull-downs, and does not need any external pull-ups. Otherwise it can be used as general I/O port as open drain circuit. All ports can be used bi-directional and these are as I/O ports. These ports are not true I/O, but rather are pseudo-I/O ports. This is because these ports have strong pull-downs and weak pull-ups.

6.3 Serial I/O

The W79E82X series have one serial port that is functionally similar to the serial port of the original 8032 family. However the serial port on the W79E82X series can operate in different modes in order to obtain timing similarity as well. The Serial port has the enhanced features of Automatic Address recognition and Frame Error detection.

6.4 Timers

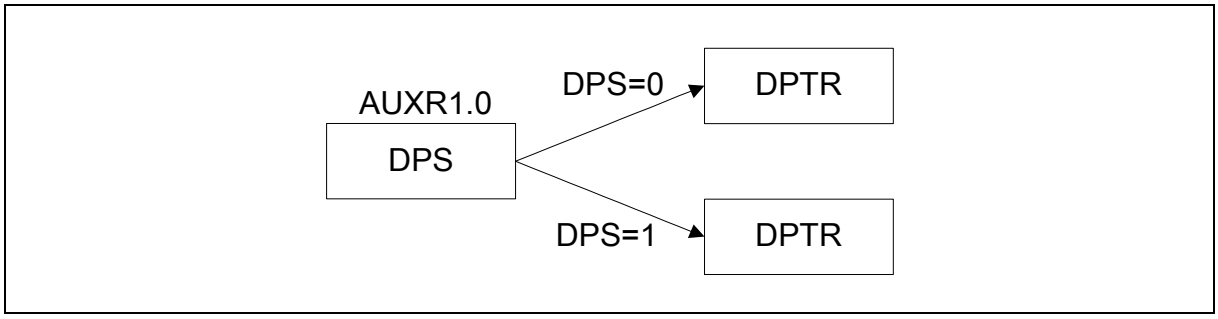
The W79E82X series have two 16-bit timers that are functionally and similar to the timers of the 8052 family. When used as timers, they are set 12 or 4 clocks per count that emulates the timing of the original 8052.

6.5 Interrupts

The Interrupt structure in the W79E82X series is slightly different from that of the standard 8052. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased.

6.6 Data Pointers

The data pointers of W79E82X series are same as 8052 that has dual 16-bit Data Pointers (DPTR) by setting DPS of AUXR1.0. The figure of dual DPTR is as below diagram.



6.7 Architecture

The W79E82X series are based on the standard 8052 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard 8052 instruction set.

6.7.1 ALU

The ALU is the heart of the W79E82X series. It is responsible for the arithmetic and logical functions. It is also used in decision making, in case of jump instructions, and is also used in calculating jump addresses. The user cannot directly use the ALU, but the Instruction Decoder reads the op-code, decodes it, and sequences the data through the ALU and its associated registers to generate the required result. The ALU mainly uses the ACC which is a special function register (SFR) on the chip. Another SFR, namely B register is also used in Multiply and Divide instructions. The ALU generates several status signals which are stored in the Program Status Word register (PSW).

6.7.2 Accumulator

The Accumulator (ACC) is the primary register used in arithmetic, logical and data transfer operations in the W79E82X series. Since the Accumulator is directly accessible by the CPU, most of the high speed instructions make use of the ACC as one argument.

6.7.3 B Register

This is an 8-bit register that is used as the second argument in the MUL and DIV instructions. For all other instructions it can be used simply as a general purpose register.

6.7.4 Program Status Word:

This is an 8-bit SFR that is used to store the status bits of the ALU. It holds the Carry flag, the Auxiliary Carry flag, General purpose flags, the Register Bank Select, the Overflow flag, and the Parity flag.

6.7.5 Scratch-pad RAM

The W79E82X series have a **256/128** bytes on-chip scratch-pad RAM. These can be used by the user for temporary storage during program execution. A certain section of this RAM is bit addressable, and can be directly addressed for this purpose.

6.7.6 Stack Pointer

The W79E82X series have an 8-bit Stack Pointer which points to the top of the Stack. This stack resides in the Scratch Pad RAM in the W79E82X series. Hence the size of the stack is limited by the size of this RAM.

6.8 Power Management

Power Management like the standard 8052, the W79E82X series also have the IDLE and POWER DOWN modes of operation. In the IDLE mode, the clock to the CPU is stopped while the timers, serial ports and interrupt lock continue to operate. In the POWER DOWN mode, all clocks are stopped and the chip operation is completely stopped. This is the lowest power consumption state.

7. MEMORY ORGANIZATION

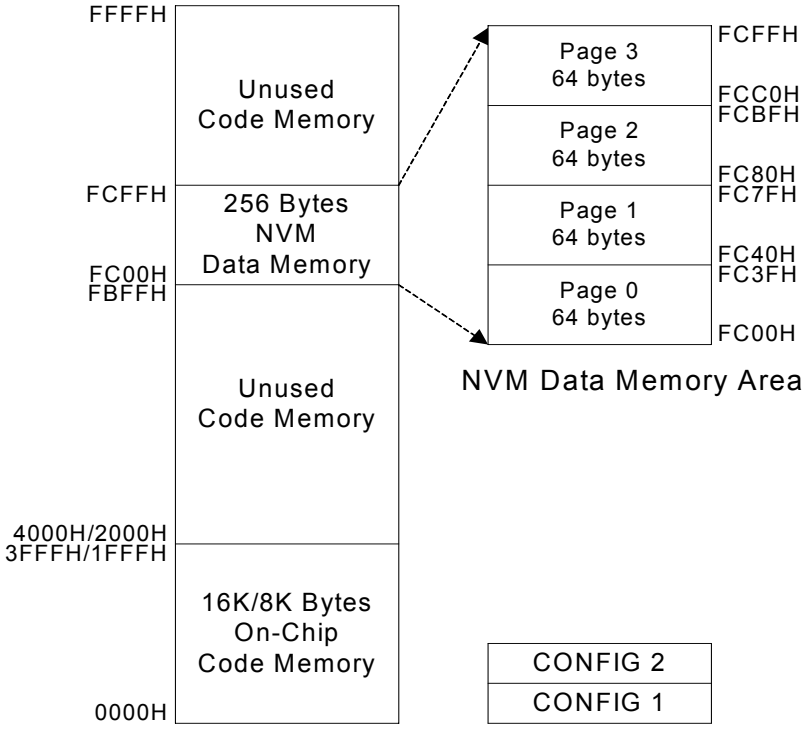
The W79E82X series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

Program Memory

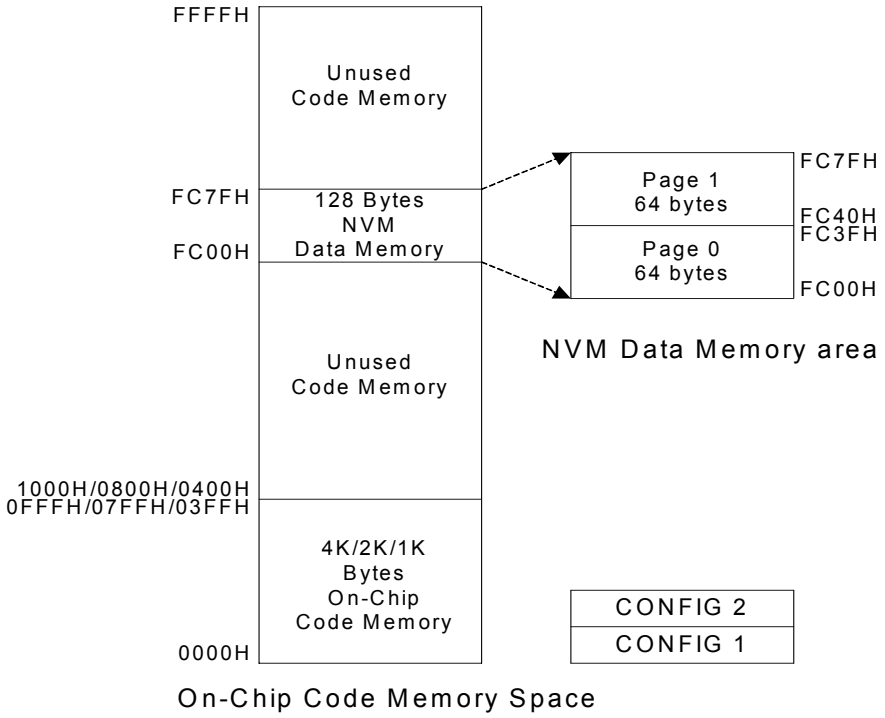
The Program Memory on the W79E82X series can be up to **16K/8K/4K/2K/1K** bytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

Data Memory

The NVM Data Memory of Flash EPROM on the W79E82X series can be up to **256/128** bytes long. The W79E82X series read the content of data memory by using "MOVC A,@A+DPTR". To write data is by NVMADDR, NVMDAT and NVMCON SFR's registers.



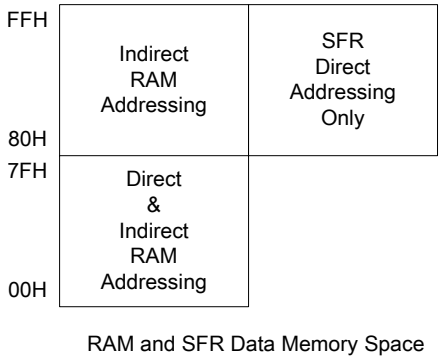
W79E825/W79E824 Memory Map



W79E823/W79E822/W79E821 Memory Map

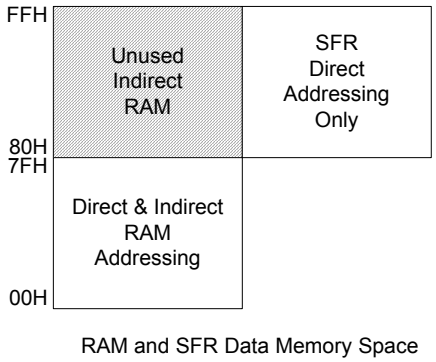
Register Map

As mentioned before the W79E82X series have separate Program and Data Memory areas. The on-chip **256/128** bytes scratch pad RAM is in addition to the external memory. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.



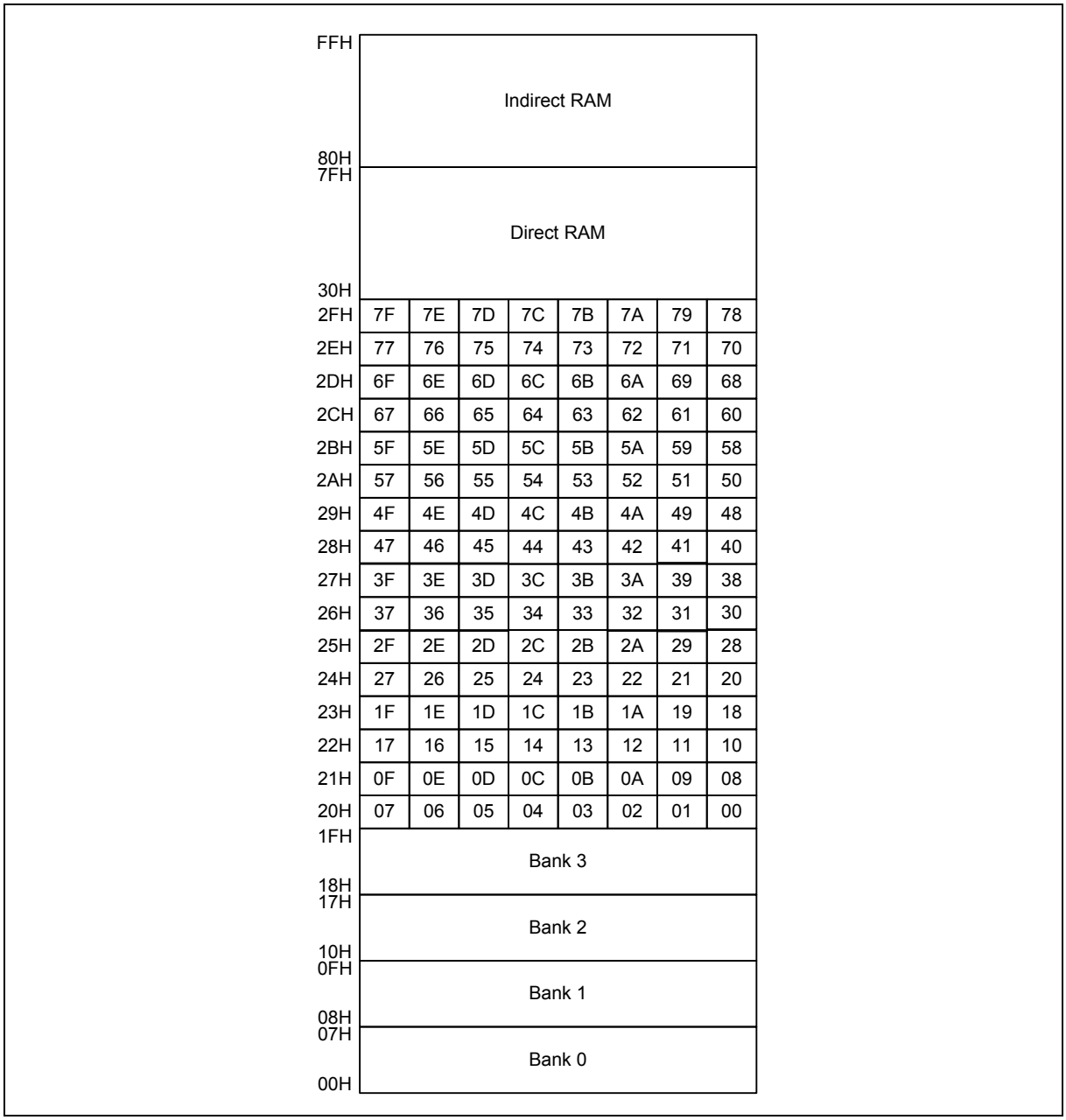
W79E825/W79E824 RAM and SFR Memory Map

The W79E823, W79E822 and W79E821 RAM and SFR memory map as below figure:



W79E823/W79E822/W79E821 RAM and SFR Memory Map

Since the scratch-pad RAM is only **256/128** bytes it can be used only when data contents are small. There are several other special purpose areas within the scratch-pad RAM. These are described as follows.



Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed ads Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at one time the W79E82X series can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

Bit addressable Locations

The Scratch-pad RAM area from location 20h to 2Fh is byte as well as bit addressable. This means that a bit in this area can be individually addressed. In addition some of the SFRs are also bit addressable. The instruction decoder is able to distinguish a bit access from a byte access by the type of the instruction itself. In the SFR area, any existing SFR whose address ends in a 0 or 8 is bit addressable.

Stack

The scratch-pad RAM can be used for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a jump, call or interrupt is invoked the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07h at reset. The user can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, then the SP is decreased.

8. SPECIAL FUNCTION REGISTERS

The W79E82X series uses Special Function Registers (SFRs) to control and monitor peripherals and their Modes. The SFRs reside in the register locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where we wish to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. The W79E82X series contain all the SFRs present in the standard 8052. However some additional SFRs are added. In some cases the unused bits in the original 8052, have been given new functions. The list of the SFRs is as follows.

Table 1 Special Function Register Location Table

F8	IP1							
F0	B						P0ID	IP1H
E8	IE1							
E0	ACC	ADCCON	ADCH					
D8	WDCON	PWMPL	PWM0L	PWM1L	PWMCON1	PWM2L	PWM3L	PWMCON2
D0	PSW	PWMPH	PWM0H	PWM1H		PWM2H	PWM3H	PWMCON3
C8							NVMCON	NVMDAT
C0	I2CON	I2ADDR					NVMADDR	TA
B8	IP0	SADEN			I2DAT	I2STATUS	I2CLK	I2TIMER
B0		P0M1	P0M2	P1M1	P1M2	P2M1	P2M2	IP0H
A8	IE	SADDR			CMP1	CMP2		
A0	P2	KBI	AUXR1					
98	SCON	SBUF						
90	P1					DIVM		
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	
80	P0	SP	DPL	DPH				PCON

Note: 1. The SFRs in the column with dark borders are bit-addressable

2. The table is condensed with eight locations per row. Empty locations indicate that these are no registers at these addresses. When a bit or register is not implemented, it will read high.

PORT 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

P0.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
7	P0.7	Timer 1 pin or KBI.7 pin of keypad input.
6	P0.6	CMP1 pin of analog comparator or KBI.6 pin of keypad input.
5	P0.5	CMPREF pin of analog comparator or KBI.5 pin of keypad input.
4	P0.4	CIN1A pin of analog comparator or KBI.4 pin of keypad input.
3	P0.3	CIN1B pin of analog comparator or KBI.3 pin of keypad input.
2	P0.2	BRAKE pin of PWM or CIN2A pin of analog comparator or KBI.2 pin of keypad input.
1	P0.1	PWM0 pin or CIN2B pin of analog comparator or KBI.1 pin of keypad input.
0	P0.0	PWM3 pin or CMP2 pin of analog comparator or KBI.0 pin of keypad input.

Note: The initial value of the port is set by CONFIG1.PRHI bit. The default setting for CONFIG1.PRHI =1 which the alternative function output is turned on upon reset. If CONFIG1.PRHI is set to 0, the user has to write a 1 to port SFR to turn on the alternative function output.

STACK POINTER

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

The Stack Pointer stores the Scratchpad RAM address where the stack begins. In other words, it always points to the top of the stack.

DATA POINTER LOW

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

This is the low byte of the standard 8052 16-bit data pointer.

DATA POINTER HIGH

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

This is the high byte of the standard 8052 16-bit data pointer.

This is the high byte of the DPTR 16-bit data pointer.

POWER CONTROL

Bit:	7	6	5	4	3	2	1	0
	SMOD	SMOD0	BOF	POR	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: This bit doubles the serial port baud rate in mode 1, 2, and 3.
6	SMOD0	0: Framing Error Detection Disable. SCON.7 acts as per the standard 8052 function. 1: Framing Error Detection Enable, then and SCON.7 indicates a Frame Error and acts as the FE flag.
5	BOF	0: Cleared by software. 1: Set automatically when a brownout reset or interrupt has occurred. Also set at power on.
4	POR	0: Cleared by software. 1: Set automatically when a power-on reset has occurred.
3	GF1	General purpose user flags.
2	GF0	General purpose user flags.
1	PD	1: the CPU goes into the POWER DOWN mode. In this mode, all the clocks are stopped and program execution is frozen.
0	IDL	1: The CPU goes into the IDLE mode. In this mode, the clocks CPU clock stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating.

TIMER CONTROL

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 overflow flag: This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 run control: This bit is set or cleared by software to turn timer/counter on or off.
5	TF0	Timer 0 overflow flag: This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 run control: This bit is set or cleared by software to turn timer/counter on or off.

Continued.

BIT	NAME	FUNCTION
3	IE1	Interrupt 1 Edge Detect: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the pin.
2	IT1	Interrupt 1 type control: Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect: Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the pin.
0	IT0	Interrupt 0 type control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while $\overline{INT1}$ pin is high and TR1 control bit is set. When cleared, Timer 1 is enabled whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Select: When cleared, the timer is incremented by internal clocks. When set, the timer counts high-to-low edges of the T1 pin.
5	M1	Timer1 Mode Select bit1: See table below.
4	M0	Timer1 Mode Select bit0: See table below.
3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while $\overline{INT0}$ pin is high and TR0 control bit is set. When cleared, Timer 0 is enabled whenever TR0 control bit is set.
2	C/$\overline{T}$	Timer or Counter Select: When cleared, the timer is incremented by internal clocks. When set, the timer counts high-to-low edges of the T0 pin.
1	M1	Timer0 Mode Select bit1: See table below.
0	M0	Timer0 Mode Select bit0: See table below.

M1, M0: Mode Select bits:

M1	M0	MODE
0	0	Mode 0: 8-bits with 5-bit prescale.
0	1	Mode 1: 16-bits, no prescale.
1	0	Mode 2: 8-bits with auto-reload from THx
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer 0 control bits. TH0 is a 8-bit timer only controlled by Timer 1 control bits. (Timer 1) Timer/counter is stopped.

TIMER 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

TL0.7-0: Timer 0 LSB

TIMER 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

TL1.7-0: Timer 1 LSB

TIMER 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

TH0.7-0: Timer 0 MSB

TIMER 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

TH1.7-0: Timer 1 MSB

Clock Control

Bit:	7	6	5	4	3	2	1	0
	-	-	-	T1M	T0M	-	-	-

Mnemonic: CKCON Address: 8Eh

BIT	NAME	FUNCTION
7~5	-	Reserved
4	T1M	Timer 1 clock select: 0: Timer 1 uses a divide by 12 clocks. 1: Timer 1 uses a divide by 4 clocks.
3	T0M	Timer 0 clock select: 0: Timer 0 uses a divide by 12 clocks. 1: Timer 0 uses a divide by 4 clocks.
2~0	-	Reserved

PORT 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
7	P1.7	PWM 2 Pin
6	P1.6	PWM 1 Pin
5	P1.5	RST Pin or Input Pin by alternative
4	P1.4	INT1 interrupt
3	P1.3	INT0 interrupt or SDA of I^2C
2	P1.2	Timer 0 or SCL of I^2C
1	P1.1	RXD of Serial port
0	P1.0	TXD of Serial port

Divider Clock

Bit:	7	6	5	4	3	2	1	0
	DIVM.7	DIVM.6	DIVM.5	DIVM.4	DIVM.3	DIVM.2	DIVM.1	DIVM.0

Mnemonic: DIVM Address: 95h

The DIVM register is clock divider of uC. Refer OSCILLATOR chapter.

SERIAL PORT CONTROL

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial port mode select bit 0 or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.
6	SM1	Serial port Mode bit 1: **Mode: SM0 SM1 Description Length Baud rate** 0 0 0 Synchronous 8 4/12 Tclk 1 0 1 Asynchronous 10 Variable 2 1 0 Asynchronous 11 64/32 Tclk 3 1 1 Asynchronous 11 Variable
5	SM2	Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1, then RI will not be activated if a valid stop bit was not received. In mode 0, the SM2 bit controls the serial port clock. If set to 0, then the serial port runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052. When set to 1, the serial clock become divide by 4 of the oscillator clock. This results in faster synchronous serial communication.
4	REN	Receive enable: When set to 1 serial reception is enabled, otherwise reception is disabled.
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2 apply to this bit. This bit can be cleared only by software.

SERIAL DATA BUFFER

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

BIT	NAME	FUNCTION
7~0	SBUF	Serial data on the serial port is read from or written to this location. It actually consists of two separate internal 8-bit registers. One is the receive resister, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

PORT 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	P2.1	P2.0

Mnemonic: P2 Address: A0h

BIT	NAME	FUNCTION
7~2	-	Reserved
1	P2.1	XTAL2 or CLKOUT pin by alternative.
0	P2.0	XTAL1 clock input pin.

Keyboard Interrupt

Bit:	7	6	5	4	3	2	1	0
	KBI.7	KBI.6	KBI.5	KBI.4	KBI.3	KBI.2	KBI.1	KBI.0

Mnemonic: KBI Address: A1h

Keyboard interrupt enable.

BIT	NAME	FUNCTION
7	KBI.7	1: Enable P0.7 as a cause of a Keyboard interrupt.
6	KBI.6	1: Enable P0.6 as a cause of a Keyboard interrupt.
5	KBI.5	1: Enable P0.5 as a cause of a Keyboard interrupt.
4	KBI.4	1: Enable P0.4 as a cause of a Keyboard interrupt.
3	KBI.3	1: Enable P0.3 as a cause of a Keyboard interrupt.
2	KBI.2	1: Enable P0.2 as a cause of a Keyboard interrupt.
1	KBI.1	1: Enable P0.1 as a cause of a Keyboard interrupt.
0	KBI.0	1: Enable P0.0 as a cause of a Keyboard interrupt.

AUX Function Register 1

Bit:	7	6	5	4	3	2	1	0
	KBF	BOD	BOI	LPBOV	SRST	ADCEN	0	DPS

Mnemonic: AUXR1 Address: A2h

BIT	NAME	FUNCTION
7	KBF	Keyboard Interrupt Flag: 1: When any pin of port 0 that is enabled for the Keyboard Interrupt function goes low. Must be cleared by software.
6	BOD	Brown Out Disable: 0: Enable Brownout Detect function. 1: Disable Brownout Detect function and save power.

Continued.

BIT	NAME	FUNCTION
5	BOI	Brown Out Interrupt: 0: Disable Brownout Detect Interrupt function and it will cause chip reset when BOF is set. 1: This prevents Brownout Detection from causing a chip reset and allows the Brownout Detect function to be used as an interrupt.
4	LPBOV	Low Power Brown Out Detect control: 0: When BOD is enable, the Brown Out detect is always turned on by normal run or Power Down mode. 1: When BOD is enable, the 1/16 time will be turned on Brown Out detect circuit by Power Down mode. When uC is in Power Down mode, the BOD will enable internal RC OSC(2MHz~0.5MHZ)
3	SRST	Software reset: 1: reset the chip as if a hardware reset occurred.
2	ADCEN	0: Disable ADC circuit. 1: Enable ADC circuit.
1	0	Reserved
0	DPS	Dual Data Pointer Select 0: To select DPTR of standard 8051. 1: To select DPTR1

INTERRUPT ENABLE

Bit:	7	6	5	4	3	2	1	0
	EA	EADC	EBO	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

BIT	NAME	FUNCTION
7	EA	Global enable. Enable/Disable all interrupts.
6	EADC	Enable ADC interrupt.
5	EBO	Enable Brown Out interrupt.
4	ES	Enable Serial Port interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt 1.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt 0.

SLAVE ADDRESS

Bit:	7	6	5	4	3	2	1	0
	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0

Mnemonic: SADDR Address: A9h

BIT	NAME	FUNCTION
7	SADDR	The SADDR should be programmed to the given or broadcast address for serial port 0 to which the slave processor is designated.

Comparator 1 Control Register

Bit:	7	6	5	4	3	2	1	0
	-	-	CE1	CP1	CN1	OE1	CO1	CMF1

Mnemonic: CMP1 Address: Ach

BIT	NAME	FUNCTION
7	-	Reserved
6	-	Reserved
5	CE1	Comparator enable: 0: Disable Comparator. 1: Enabled Comparator. Comparator output need wait stable 10 us after CE1 is first set.
4	CP1	Comparator positive input select: 0: CIN1A is selected as the positive comparator input. 1: CIN1B is selected as the positive comparator input.
3	CN1	Comparator negative input select: 0: The comparator reference pin CMPREF is selected as the negative comparator input. 1: The internal comparator reference Vref is selected as the negative comparator input.
2	OE1	Output enable: 1: The comparator output is connected to the CMP1 pin if the comparator is enabled (CE1 = 1). This output is asynchronous to the CPU clock.
1	CO1	Comparator output: Synchronized to the CPU clock to allow reading by software. Cleared when the comparator is disabled (CE1 = 0).
0	CMF1	Comparator interrupt flag: This bit is set by hardware whenever the comparator output CO1 changes state. This bit will cause a hardware interrupt if enabled and of sufficient priority. Cleared by software and when the comparator is disabled (CE1 = 0).

Comparator 2 Control Register

Bit:	7	6	5	4	3	2	1	0
	-	-	CE2	CP2	CN2	OE2	CO2	CMF2

Mnemonic: CMP2 Address: ADh