Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

CompactFlash™ Card
INDUSTRIAL GRADE
W7CFxxxA-H4 / W8CFxxxA-H4
Series

INFORMATION IN THIS DOCUMENT IS PROVIDED IN RELATION TO WINTEC INDUSTRIES PRODUCTS, AND IS SUBJECT TO CHANGE WITHOUT NOTICE.

NOTHING IN THIS DOCUMENT SHALL BE CONTRUED AS GRANTING ANY LICENSE, EXPRESS OR IMPLIED.

ALL INFORMATION IN THIS DOCUMENT IS PROVIDED ON AN "AS-IS" BASIS WITHOUT GUARANTEE OR WARRANTY OF ANY KIND.

- Please contact your nearest Wintec representative for the latest updates or additional product information.

August 2013 © Wintec Industries, Inc.

Table of Contents

August 2013 © Wintec Industries, Inc.

Revision History

Revision	Month	Year	History
1.00	September	2009	Initial Release (Preliminary)
1.01	October	2009	Add firmware revision 090904 as option
1.02	January	2010	Add firmware revision 091110a as option
1.03	February	2010	Add Dual ID mode as option
1.04	October	2011	Update Ordering Guide Remove 128MB option
1.05	March	2012	Added Support for Micron Flash
1.06	July	2012	Updated Ordering Guide
1.07	May	2013	Corrected Typo's

FEATURES

Wintec Type I Compact Flash
(Industrial Grade H4 Series)

GENERAL

- Density up to 32GB
- 32-bit RISC/DSP controller
- Large internal SRAM provides firmware flexibility
- Dual voltage support at 3.3V / 5V
- Internal voltage detector
- 20 Kbyte internal Boot ROM and 32 Kbyte internal SRAM
- Specialized for high-reliability
- RoHS 6/6 compliant

RELIABILITY

- > 2,000,000 Program/Erase Cycles
- Industrial Wear Leveling
  - Includes Static Block Management
- Spares & Bad Block Management
- On-Board ECC capable of correcting 4 random bytes per 512 bytes sector with additional CRC for dynamic error checking
- High Environmental Tolerance
- 10-Year Data Retention
- Unlimited Reads

COMPATIBILITY

- Fully compliance to CompactFlash ™ 3.0 and compatible to 4.1 specifications
- ATA-6 standard compatible in True-IDE mode
- PCMCIA specification 2.1
- Fast ATA supporting PIO mode 6, MDMA mode 4, UDMA mode 4 in True-IDE mode
- Four integrated 8Kbyte Sector Buffers and 256 Byte PCMCIA Attribute Memory

PERFORMANCE

- True IDE Mode Capable
  - Host data transfer in PIO mode 6 or MDMA mode 4 up to 25 MByte/second
  - Host data transfer in UDMA mode 4 up to 66 MByte/second
- High Performance
  - Two Direct Flash Access (DFA) Channels including two sector buffers support interleaving operation
- Low Power Consumption:
  - Maximum operation current is 130 mA (32 GB)
  - Sleep mode current < 4 mA. (32 GB)

August 2013 © Wintec Industries, Inc.

DESCRIPTION

Wintec's Compact Flash card is based on industrial leading Hyperstone F4 controller chip, which is a 32-bit RISC processor with instruction set extension optimized for Flash handling. The superior wear leveling done by the controller chip involves all physical blocks including the ones containing static data to meet the most demanding requirements from users in a data traffic intensive environment.

The card contains a 50-pin connector consisting of two rows of 25 female contacts each on 50 mils (1.27mm) centers. The Industrial Grade CompactFlash™ Memory Cards are constructed with Samsung or Micron single-level-cell (SLC) NAND flash memory devices. It employs a variety of sophisticated functions, such as the Reed-Solomon error correction code which is capable of correcting up to 4 symbols in a 512 bytes sector with additional CRC for dynamic error checking. The wear-leveling methods ensure even wear of flash blocks across the entire card capacity. With background operations to track erase counts, the card prioritizes new writes to blocks with lower wear, and relocates static data to blocks with higher wear. Bad-block Management routines replace worn blocks with spare blocks reserved by the controller on card initialization. All Flash management utilities allow for maximum levels of data reliability and card endurance for prolong life cycle.

August 2013 © Wintec Industries, Inc.

1.0 General Product Specification

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

Table 1: Performance Specifications

Parameter	Performance	
	PIO Mode 6	**UDMA Mode (Mode 4)**
Burst Transfer Rate To/From Host	25 MB/s	66 MB/s
Burst Transfer Rate Internally To/From Flash	80 MB/s	80 MB/s
Sustained Sequential Read (Typical)	18 MB/s	42 MB/s
Sustained Sequential Write (Typical)	7.5 MB/s	20 MB/s
Random Read (Typical)	TBD	38MB/s
Random Write (Typical)	TBD	8MB/s

Table 2: Card Endurance

Parameter	Spec
Program/Erase Cycles	> 2,000,000 Cycles
Read Cycles	Unlimited
Data Retention	10 Years (Min.)
MTBF	> 4,000,000 Hours

Table 3: Card Data Reliability

Parameter	Spec
Non-Recoverable Errors	< 1 in 10^{14} Bytes Read
Erroneous Correction	< 1 in 10^{20} Bytes Read
ECC Correctability	4 Bytes/Sector

Table 4: Environmental Specifications

Parameters		Operating	Non-Operating
Temperature	**Standard Temp.**	0°C to 70°C	-55°C to 95°C
	Industrial Temp.	-40°C to 85°C	-55°C to 95°C
Humidity		8% to 95% (Non-Condensing)	8% to 95% (Non-Condensing)
Vibration		16.3 G rms	N/A
Altitude		80,000 ft. (Max.)	
Shock		2,000 G (Max.)	
Acoustic		0 db	

August 2013 © Wintec Industries, Inc.

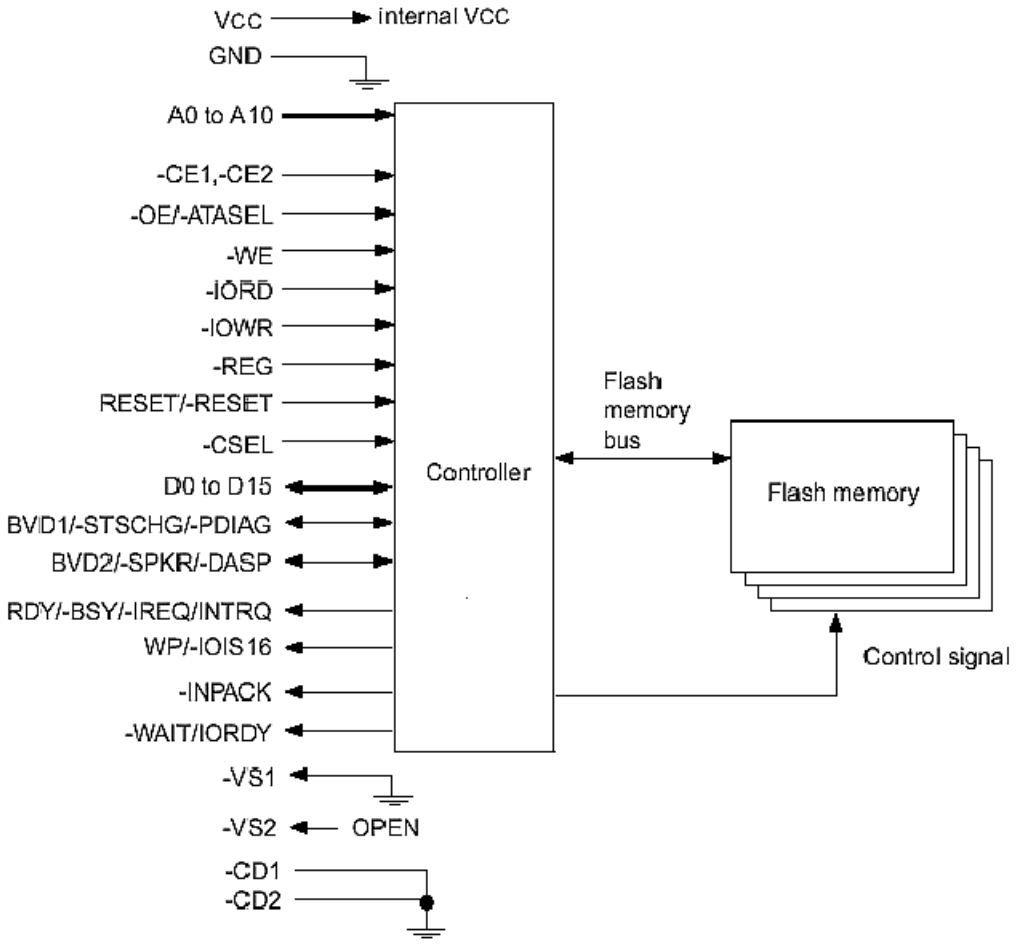

Figure 1: Card Block Diagram

NOTE: -CE1, -CE2, -OE, -WE –IORD, -IOWR, -REG, -RESET, -CSEL, -PDIAG, -DASP pins are pulled up in card. –CE1, -CE2, -OE, -WE, -IORD, -IOWR, -REG pins are Schmitt trigger type input buffer.

Table 5: Card Pin Assignment

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin	**Signal**	**Type**	**Pin**	**Signal**	**Type**	**Pin**	**Signal**	**Type**
1	GND	Ground	**1**	GND	Ground	**1**	GND	Ground
2	D03	I/O	**2**	D03	I/O	**2**	D03	I/O
3	D04	I/O	**3**	D04	I/O	**3**	D04	I/O
4	D05	I/O	**4**	D05	I/O	**4**	D05	I/O
5	D06	I/O	**5**	D06	I/O	**5**	D06	I/O
6	D07	I/O	**6**	D07	I/O	**6**	D07	I/O
7	-CE1	I	**7**	-CE1	I	**7**	-CS0	I
8	A10	I	**8**	A10	I	**8**	A10[2]	I
9	-OE	I	**9**	-OE	I	**9**	-ATA SEL	I
10	A09	I	**10**	A09	I	**10**	A09[2]	I
11	A08	I	**11**	A08	I	**11**	A08[2]	I
12	A07	I	**12**	A07	I	**12**	A07[2]	I
13	VCC	Power	**13**	VCC	Power	**13**	VCC	Power
14	A06	I	**14**	A06	I	**14**	A06[2]	I
15	A05	I	**15**	A05	I	**15**	A05[2]	I
16	A04	I	**16**	A04	I	**16**	A04[2]	I
17	A03	I	**17**	A03	I	**17**	A03[2]	I
18	A02	I	**18**	A02	I	**18**	A02	I
19	A01	I	**19**	A01	I	**19**	A01	I
20	A00	I	**20**	A00	I	**20**	A00	I
21	D00	I/O	**21**	D00	I/O	**21**	D00	I/O
22	D01	I/O	**22**	D01	I/O	**22**	D01	I/O
23	D02	I/O	**23**	D02	I/O	**23**	D02	I/O
24	WP	O	**24**	-IOIS16	O	**24**	-IOCS16	O
25	-CD2	O	**25**	-CD2	O	**25**	-CD2	O
26	-CD1	O	**26**	-CD1	O	**26**	-CD1	O
27	D11[1]	I/O	**27**	D11[1]	I/O	**27**	D11[1]	I/O
28	D12[1]	I/O	**28**	D12[1]	I/O	**28**	D12[1]	I/O
29	D13[1]	I/O	**29**	D13[1]	I/O	**29**	D13[1]	I/O
30	D14[1]	I/O	**30**	D14[1]	I/O	**30**	D14[1]	I/O
31	D15[1]	I/O	**31**	D15[1]	I/O	**31**	D15[1]	I/O
32	-CE2[1]	I	**32**	-CE2[1]	I	**32**	-CS1[1]	I
33	-VS1	O	**33**	-VS1	O	**33**	-VS1	O
34	-IORD	I	**34**	-IORD	I	**34**	-IORD	I
35	-IOWR	I	**35**	-IOWR	I	**35**	-IOWR	I
36	-WE	I	**36**	-WE	I	**36**	-WE[3]	I
37	RDY/BSY	O	**37**	IREQ	O	**37**	INTRQ	O
38	VCC	Power	**38**	VCC	Power	**38**	VCC	Power
39	-CSEL	I	**39**	-CSEL	I	**39**	-CSEL	I
40	-VS2	O	**40**	-VS2	O	**40**	-VS2	O
41	RESET	I	**41**	RESET	I	**41**	RESET	I
42	-WAIT	O	**42**	-WAIT	O	**42**	IORDY	O
43	-INPACK	O	**43**	-INPACK	O	**43**	DMARQ	O
44	-REG	I	**44**	-REG	I	**44**	-DMACK	I
45	BVD2	I/O	**45**	-SPKR	I/O	**45**	-DASP	I/O
46	BVD1	I/O	**46**	-STSCHG	I/O	**46**	-PDIAG	I/O
47	D08[1]	I/O	**47**	D08[1]	I/O	**47**	D08[1]	I/O
48	D09[1]	I/O	**48**	D09[1]	I/O	**48**	D09[1]	I/O
49	D10[1]	I/O	**49**	D10[1]	I/O	**49**	D10[1]	I/O
50	GND	Ground	**50**	GND	Ground	**50**	GND	Ground

NOTE:

1. These signals are required only for 16-bit access and not required when installed in 8-bit systems. For lowest power dissipation, leave these signals open.
2. Should be grounded by the host.

3. Should be tied to VCC by the host.

Table 6: Card Pin Explanation

Signal Name	Type	Pin #	Description
A10 - A0 (PC Card Memory Mode)	I	8, 10, 11, 12, 14 -20	These address lines along with the –REG signal are used to select the following: The I/O port address registers within the Compact Flash Card, the memory mapped port address registers within the card, a byte in the card's information structure and its configuration control and status registers.
A10 - A0 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
A2 - A0 (True IDE Mode) A10 - A3 (True IDE Mode)		18, 19, 20	In True IDE Mode only A [2:0] is used to select the one of eight registers in the Task File. In True IDE Mode these remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	46	This signal is asserted high as the BVD1 signal since a battery is not used with this product.
-STSCHG (PC Card I/O Mode) Status Changed			This signal is asserted low to alert the host to changes in the RDY/ -BSY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
-PDIAG (True IDE Mode)			In the True IDE Mode, this input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	45	This output line is always driven to a high state in Memory Mode since a battery is not required for this product.
-SPKR (PC Card I/O Mode)			This output line is always driven to a high state in I/O Mode since this product does not support the audio function.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode)	O	25, 26	These Card Detect pins are connected to ground on the Compact Flash Card. They are used by the host to determine if the card is fully inserted into its socket.
-CD1, -CD2 (PC Card I/O Mode)			This signal is the same for all modes.
-CD1, -CD2 (True IDE Mode)			This signal is the same for all modes.

August 2013 © Wintec Industries, Inc.

Table 6: Card Pin Explanation Cont.

Signal Name	Type	Pin #	Description
-CE1, -CE2 (PC Card Memory Mode) Card Enable	I	7, 32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. –CE2 always accesses the odd byte of the word. –CE1 accesses the even byte or the Odd byte of the word depending on A0 and –CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0 -D7.
-CE1, -CE2 (PC Card I/O Mode) Card Enable			This signal is the same as the PC Card Memory Mode signal.
-CS0, -CS1 (True IDE Mode)			In the True IDE Mode –CS0 is the chip select for the task file registers while –CS1 is used to select the Alternate Status Register and the Device Control Register.
-CSEL (PC Card Memory Mode)	I	39	This signal is not used for this mode.
-CSEL (PC Card I/O Mode)			This signal is not used for this mode.
-CSEL (True IDE Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When this pin is open, this device is configured as a Slave.
D15 - D00 (PC Card Memory Mode)	I/O	2-6, 21, 22, 23, 27-31, 47, 48, 49	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
D15 - D00 (PC Card I/O Mode)			These signals are the same as the PC Card Memory Mode signal.
D15 - D00 (True IDE Mode)			In True IDE Mode all Task File operations occur in byte mode on the low order bus D00 -D07 while all data transfers are 16 bits using D00 -D15.
GND (PC Card Memory Mode)	-	1, 50	Ground.
GND (PC Card I/O Mode)			This signal is the same for all modes.
GND (True IDE Mode)			This signal is the same for all modes.

August 2013 © Wintec Industries, Inc.

-INPACK (PC Card Memory Mode)	O	43	This signal is not used in this mode.
-INPACK (PC Card I/O Mode) Input Acknowledge			The Input Acknowledge signal is asserted by the Compact Flash Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the card and the CPU.
DMARQ (True IDE Mode)			This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by DIOR- and DIOW-.This signal is used in a handshake manner with DMACK- before negating DMAREQ, and reasserting DMAREQ if there is more data to transfer. DMAREQ shall not be driven when the device is not selected. While a DMA operation is in progress, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits. If there is no hardware support for DMA mode in the host, this output signal is not used and should not be connected at the host .In this case, the BIOS must report that DMA mode is not supported by the host so that the device driver will not attempt DMA mode. A host that does not support DMA mode and implements both PCMCIA and true-IDE modes of operation need not alter the PCMICIA mode connections while in True-IED mode as long as this does not prevent proper operation in any mode.
-IORD (PC Card Memory Mode)	I	34	This signal is not used in this mode.
-IORD (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the Compact Flash Card when the card is configured to use the I/O interface.
-IORD (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.

Table 6: Card Pin Explanation Cont.

Signal Name	Type	Pin #	Description
-IOWR (PC Card Memory Mode)	I	35	This signal is not used in this mode.
- IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the Compact Flash controller registers when the card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge).
- IOWR (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the Compact Flash Card in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
-ATA SEL (True IDE Mode)			To enable True IDE Mode this input should be grounded by the host.
RDY/-BSY (PC Card Memory Mode)	O	37	In Memory Mode this signal is set high when the Compact Flash Card is ready to accept a new data transfer operation and held low when the card is busy. The host memory card socket must provide a pull-up resistor. At power up and at Reset, the RDY/-BSY signal is held low (busy) until the Compact Flash Card has completed its power up or reset function. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true: The Compact Flash Card has been powered up with +RESET continuously disconnected or asserted.
- IREQ (PC Card I/O Mode)			I/O Operation – After the Compact Flash Card has been configured for I/O operation, this signal is used as – Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
-INTRQ (True IDE Mode)			In True IDE Mode, this signal is the active high Interrupt Request to the host.

Table 6: Card Pin Explanation Cont.

Signal Name	Type	Pin #	Description
-REG (PC Card Memory Mode) Attribute Memory Select	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.
-REG (PC Card I/O Mode)			The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.
-DMACK (True IDE Mode)			This is a DMA Acknowledge signal that is asserted by the host in response to DMAREQ to initiate DMA transfers. While DMA operations are not active, the card shall ignore the –DMACK signal, including a floating condition. If DAM operation is not supported by a True-IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.
RESET (PC Card Memory Mode)	I	41	When the pin is high, this signal resets the Compact Flash Card. The card is Reset only at power up if this pin is left high or open from power-up. The card is also reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
-RESET (True IDE Mode)			In the True IDE Mode this input pin is the active low hardware reset from the host.
VCC (PC Card Memory Mode)	-	13, 38	+5, +3.3V power.
VCC (PC Card I/O Mode)			This signal is the same for all modes.
VCC (True IDE Mode)			This signal is the same for all modes.
-VS1, -VS2 (PC Card Memory Mode)	O	33, 40	Voltage Sense Signals. –VS1 is grounded so that the Compact Flash Card CIS can be read at 3.3 volts and –VS2 is open and reserved by PCMCIA for a secondary voltage.
-VS1, -VS2 (PC Card I/O Mode)			This signal is the same for all modes.
-VS1, -VS2 (True IDE Mode)			This signal is the same for all modes.

August 2013 © Wintec Industries, Inc.

Table 6: Card Pin Explanation Cont.

Signal Name	Type	Pin #	Description
-WAIT (PC Card Memory Mode)	O	42	This signal is not asserted for all modes.
-WAIT (PC Card I/O Mode)			This signal is not asserted for all modes.
-IORDY (True IDE Mode)			This signal is not asserted for all modes.
-WE (PC Card Memory Mode)	I	36	This is a signal driven by the host and used for strobing memory write data to the registers of the Compact Flash Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode this input signal is not used and should be connected to VCC by the host.
-WP (PC Card Memory Mode)	O	24	Memory Mode – The Compact Flash Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O Mode)			I/O Operation – When the Compact Flash Card is configured for I/O Operation, Pin 24 is used for the –I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOCS16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

2.0 Card Function Explanation

2.1 Attribute Access Specifications

When CIS-ROM region or Configuration register region is accessed, read and write operations are executed under the condition of –REG = "L" as follows. That region can be accessed by Byte/Word/Odd-byte modes, which are defined by PC card standard specifications.

Table 7: Attribute Read Access Mode

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	D8 -D15	D0 -D7
Standby mode		H					High-Z	High-Z
Byte access (8-bit)	L	H	L	L	L	H	High-Z	Even byte
	L	H	L	H	L	H	High-Z	Invalid
Word access (16-bit)	L	L	L		L	H	Invalid	Even byte
Odd byte access (8-bit)	L	L	H		L	H	Invalid	High-Z

Table 8: Attribute Write Access Mode

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	D8 -D15	D0 -D7
Standby mode		H					Don't care	Don't care
Byte access (8-bit)	L	H	L	L	H	L	Don't care	Even byte
	L	H	L	H	H	L	Don't care	Don't care
Word access (16-bit)	L	L	L		H	L	Don't care	Even byte
Odd byte access (8-bit)	L	L	H		H	L	Don't care	Don't care

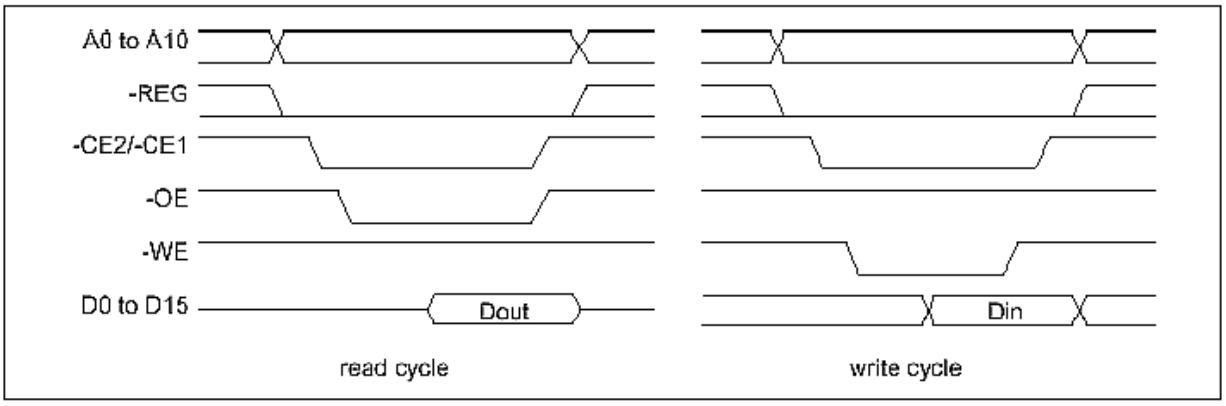

Figure 2: Attribute Access Timing Example

2.2 Task File Register Access Specifications

There are two cases of Task File register mapping, one is mapped I/O address area, and the other is mapped Memory address area. Each case of Task File register read and write operations are executed under the condition as follows. That area can be accessed by Byte/Word/Odd Byte modes, which are defined by PC card standard specifications.

2.2.1 I/O Address Map

Table 9: Task File Register Read Access Mode (i)

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D8 -D15	D0 -D7
Standby mode		H							High-Z	High-Z
Byte access (8-bit)	L	H	L	L	L	H	H	H	High-Z	Even byte
	L	H	L	H	L	H	H	H	High-Z	Odd byte
Word access (16-bit)	L	L	L		L	H	H	H	Odd byte	Even byte
Odd byte access (8-bit)	L	L	H		L	H	H	H	Odd byte	High-Z

Table 10: Task File Register Write Access Mode (i)

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D8 -D15	D0 -D7
Standby mode		H							Don't care	Don't care
Byte access (8-bit)	L	H	L	L	H	L	H	H	Don't care	Even byte
	L	H	L	H	H	L	H	H	Don't care	Odd byte
Word access (16-bit)	L	L	L		H	L	H	H	Odd byte	Even byte
Odd byte access (8-bit)	L	L	H		H	L	H	H	Odd byte	Don't care

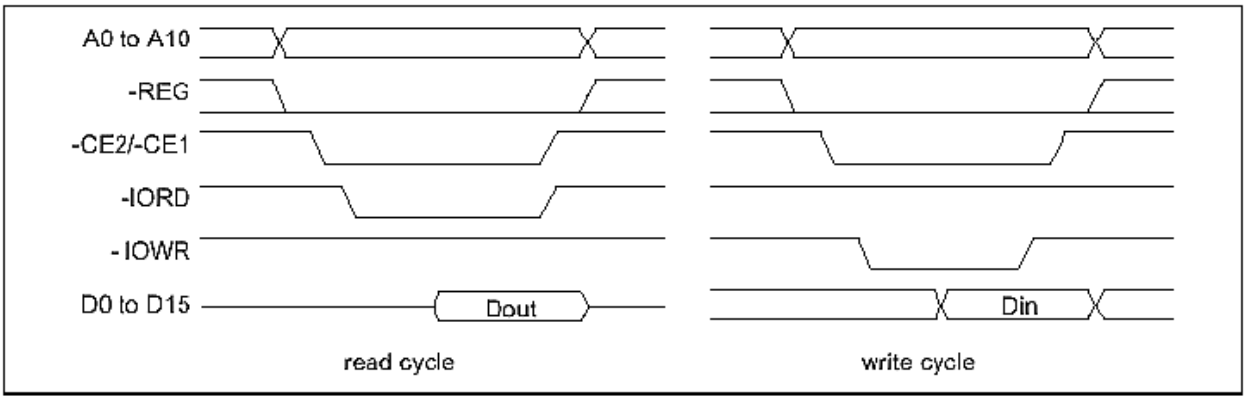

Figure 3: Task File Register Access Timing Example (i)

2.2.2 Memory Address Map

Table 11: Task File Register Read Access Mode (ii)

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D8 -D15	D0 -D7
Standby mode		H							High-Z	High-Z
Byte access (8-bit)	H	H	L	L	L	H	H	H	High-Z	Even byte
	H	H	L	H	L	H	H	H	High-Z	Odd byte
Word access (16-bit)	H	L	L		L	H	H	H	Odd byte	Even byte
Odd byte access (8-bit)	H	L	H		L	H	H	H	Odd byte	High-Z

August 2013 © Wintec Industries, Inc.

Table 12: Task File Register Write Access Mode (ii)

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D8 -D15	D0 -D7
Standby mode		H							Don't care	Don't care
Byte access (8-bit)	H	H	L	L	H	L	H	H	Don't care	Even byte
	H	H	L	H	H	L	H	H	Don't care	Odd byte
Word access (16-bit)	H	L	L		H	L	H	H	Odd byte	Even byte
Odd byte access (8-bit)	H	L	H		H	L	H	H	Odd byte	Don't care

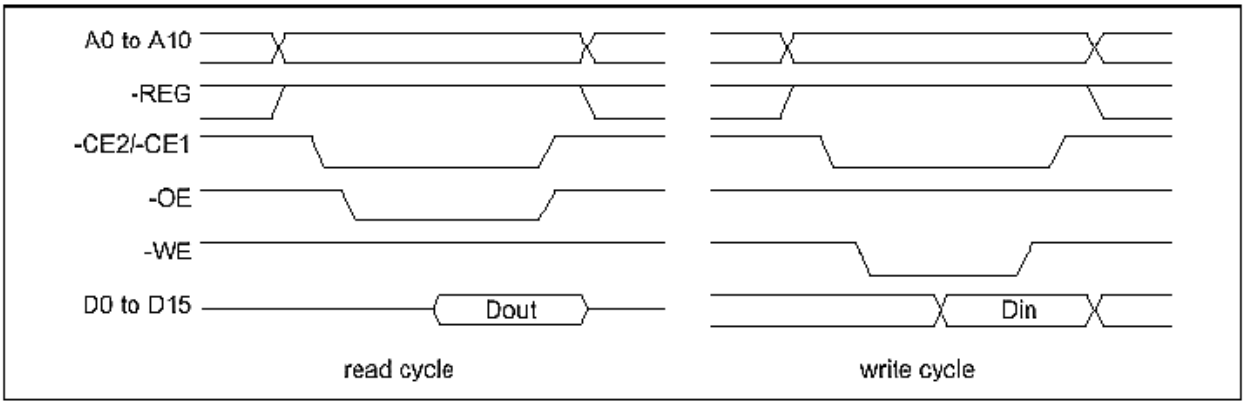

Figure 4: Task File Register Access Timing Example (ii)

2.2.3 True IDE Mode

The card can be configured in a True IDE Mode of operation. This card is configured in this mode only when the –OE input signal is asserted GND by the host. In this True IDE Mode Attribute Registers are not accessible from the host. Only I/O operation to the task files and data registers are allowed. If this card is configured during power on sequence, data registers are accessed in word (16-bit). The card permits 8-bit accesses if the user issues a Set Feature Command to put the device in 8-bit mode.

Table 13: True IDE Mode Read I/O Function

Mode	-CE2	-CE1	A0 -A2	-IORD	-IOWR	D8 -D15	D0 -D7
Invalid mode	L	L				High-Z	High-Z
Standby mode	H	H				High-Z	High-Z
Data register access	H	L	0	L	H	Odd byte	Even byte
Alternate status access	L	H	6H	L	H	High-Z	Status out
Other task file access	H	L	1-7H	L	H	High-Z	Data

Table 14: True IDE Mode Write I/O Function

Mode	-CE2	-CE1	A0 -A2	-IORD	-IOWR	D8 -D15	D0 -D7
Invalid mode	L	L				Don't care	Don't care
Standby mode	H	H				Don't care	Don't care
Data register access	H	L	0	L	H	Odd byte	Even byte
Alternate status access	L	H	6H	L	H	Don't care	Control in
Other task file access	H	L	1-7H	L	H	Don't care	Data

August 2013 © Wintec Industries, Inc.

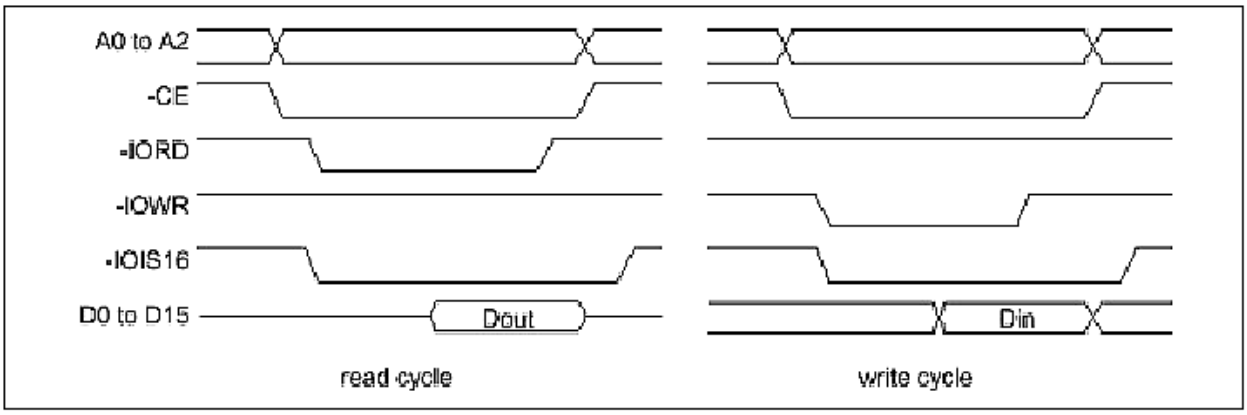

Figure 5: True IDE Mode I/O Access Timing Example

2.3 Configuration Register Specification

This card supports four configuration registers for the purpose of the configuration and observation of this card. These registers can be used in memory card mode and I/O card mode. In True IDE mode, these registers cannot be used.

2.3.1 Configuration Option register (Address 200H)

This register is used for setting the card configuration status and for issuing soft reset to the card.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SRESET	LevlREQ	INDEX					

NOTE:
1. Initial value: 00H

Table 15: Option Register Function

Name	R/W	Function
SRESET (HOST->)	R/W	Setting this bit to "1", places the card in the reset state (Card Hard Reset). This operation is equal to Hard Reset, except this bit is not cleared. Then this bit set to "0", places the card in the reset state of Hard Reset (This bit is set to "0" by Hard Reset). Card configuration status is reset and the card internal initialized operation starts when Card hard Reset is executed, so next access to the card should be the same sequence as the power on sequence.
LevlREQ (HOST->)	R/W	This bit sets to "0" when pulse mode interrupt is selected, and "1" when level mode interrupt is selected.
INDEX (HOST->)	R/W	This bit is used for select operation mode of the card as follows. When Power on, Card Hard Reset and Soft Reset, this data is "000000" for the purpose of Memory card interface recognition.

Table 16: INDEX bit assignment

INDEX Bit						Task File register address	Mapping mode
5	4	3	2	1	0		
0	0	0	0	0	0	0H to FH, 400H to 7FFH	Memory Mapped
0	0	0	0	0	1	xx0H to xxFH	Contiguous I/O Mapped
0	0	0	0	1	0	1F0H to 1F7H, 3F6H to 3F7H	Primary I/O Mapped

August 2013 © Wintec Industries, Inc.

0	0	0	0	1	1	170H to 177H, 376H to 377H	Secondary I/O Mapped

2.3.2 Configuration and Status Register (Address 202H)

This register is used for observing the card state.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CHGED	SIGCHG	IOIS8	0	0	PWD	INTR	0

NOTE:
1. 1nitial value: 00H

Table 17: Configuration and Status Register Function

Name	R/W	Function
CHGED (HOST->)	R	This bit indicates that CRDY/-BSY bit on Pin Replacement register is set to "1". When CHGED bit is set to "1", -STSCHG pin is held "L" at the condition of SIGCHG bit set to "1" and the card configured for the I/O interface.
SIGCHG (HOST->)	R/W	This bit is set or reset by the host for enabling and disabling the status-change signal (-STSCHG pin). When the card is configured I/O card interface and this bit is set to "1", -STSCHG pin is controlled by CHGED bit. If this bit is set to "0", -STSCHG pin is kept "H".
IOIS8 (HOST->)	R/W	The host sets this field to "1" when it can provide I/O cycles only with one 8-bit data bus (D7 to D0).
PWD (HOST->)	R/W	When this bit is set to "1", the card enters sleep stat (Power Down mode). When this bit is reset to "0", the card transfers to idle state (active mode). RRDY/-BSY bit on Pin Replacement Register becomes BUSY when this bit is changed. RRDY/-BSY will not become Ready until the power state requested has been entered. This card automatically powers down when it is idle, and powers back up when it receives a command.
INTR (HOST->)	R	This bit indicates the internal state of the interrupt request. This bit state is available whether I/O card interface has been configured or not. This signal remains true until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the –IEN bit in the Device Control Register, this bit is a zero.

2.3.3 Pin Replacement Register (Address 204H)

This register is used for providing the signal state of –IREQ signal when the card configured I/O card interface.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	CRDY/-BSY	0	1	1	RRDY/-BSY	0

NOTE:
1. Initial value 0CH

Table 18: Pin Replacement Register Function

Name	R/W	Function
CRDY/-BSY (HOST->)	R/W	This bit is set to "1" when the RRDY/-BSY bit changes state. This bit may also be written by the host
RRDY/-BSY (HOST->)	R/W	When read, this bit indicates +READY pin states. When written, this bit is used for CRDY/-BSY bit masking

2.3.4 Socket and Copy Register (Address 206H)

This register is used for identification of the card from the other cards. Host can read and write this register. This register should be set by host before Configuration Option register is set.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	0	DRV#	0	0	0	0

NOTE:
1. Initial value: 00H

Table 19: Socket and Copy Register Function

Name	R/W	Function
DRV# (HOST->)	R/W	This field is used for the configuration of the plural cards. When host configures the plural cards, written the card's copy number in this field. In this way, host can perform the card's master/slave organization.

2.4 Task File Register Specification

These registers are used for reading and writing the storage data in the card. These registers are mapped five types by the configuration of INDEX in Configuration Option register. The decoded addresses are shown as follows.

Table 20: Memory map (INDEX=0)

-REG	A10	A9 -A4	A3	A2	A1	A0	Offset	-OE=L	-WE=L
1	0		0	0	0	0	0H	Data register	Data register
1	0		0	0	0	1	1H	Error register	Feature register
1	0		0	0	0	0	2H	Sector count register	Sector count register
1	0		0	0	0	1	3H	Sector number register	Sector number register
1	0		0	1	1	0	4H	Cylinder low register	Cylinder low register
1	0		0	1	1	1	5H	Cylinder high register	Cylinder high register
1	0		0	1	1	0	6H	Drive head register	Drive head register
1	0		1	1	1	1	7H	Status register	Command register
1	0		1	0	0	0	8H	Dup. even data register	Dup. even data register
1	0		1	0	0	1	9H	Dup. odd data register	Dup. odd data register
1	0		1	1	1	1	DH	Dup. error register	Dup. feature register
1	0		1	1	1	0	EH	Alt. status register	Device control register
1	0		1	1	1	1	FH	Drive address register	Reserved
1	1					0	8H	Even data register	Even data register
1	1					1	9H	Odd data register	Odd data register

Table 21: Contiguous I/O map (INDEX=1)

-REG	A10 -A4	A3	A2	A1	A0	Offset	-IORD=L	-IOWR=L
0		0	0	0	0	0H	Data register	Data register
0		0	0	0	1	1H	Error register	Feature register
0		0	0	1	0	2H	Sector count register	Sector count register
0		0	0	1	1	3H	Sector number register	Sector number register
0		0	1	0	0	4H	Cylinder low register	Cylinder low register
0		0	1	0	1	5H	Cylinder high register	Cylinder high register
0		0	1	1	0	6H	Drive head register	Drive head register
0		0	1	1	1	7H	Status register	Command register
0		1	0	0	0	8H	Dup. even data register	Dup. even data register
0		1	0	0	1	9H	Dup. odd data register	Dup. odd data register
0		1	1	0	1	DH	Dup. error register	Dup. feature register

August 2013 © Wintec Industries, Inc.

0		1	1	1	0	EH	Alt. status register	Device control register
0		1	1	1	1	FH	Drive address register	Reserved

Table 22: Primary I/O Map (INDEX=2)

-REG	A10	A9 -A4	A3	A2	A1	A0	-IORD=L	-IOWR=L
0		1FH	0	0	0	0	Data register	Data register
0		1FH	0	0	0	1	Error register	Feature register
0		1FH	0	0	1	0	Sector count register	Sector count register
0		1FH	0	0	1	1	Sector number register	Sector number register
0		1FH	0	1	0	0	Cylinder low register	Cylinder low register
0		1FH	0	1	0	1	Cylinder high register	Cylinder high register
0		1FH	0	1	1	0	Drive head register	Drive head register
0		1FH	0	1	1	1	Status register	Command register
0		3FH	0	1	1	0	Alt. status register	Device control register
0		3FH	0	1	1	1	Drive address register	Reserved

Table 23: Secondary I/O Map (INDEX=3)

-REG	A10	A9 -A4	A3	A2	A1	A0	-IORD=L	-IOWR=L
0		17H	0	0	0	0	Data register	Data register
0		17H	0	0	0	1	Error register	Feature register
0		17H	0	0	1	0	Sector count register	Sector count register
0		17H	0	0	1	1	Sector number register	Sector number register
0		17H	0	1	0	0	Cylinder low register	Cylinder low register
0		17H	0	1	0	1	Cylinder high register	Cylinder high register
0		17H	0	1	1	0	Drive head register	Drive head register
0		17H	0	1	1	1	Status register	Command register
0		37H	0	1	1	0	Alt. status register	Device control register
0		37H	0	1	1	1	Drive address register	Reserved

Table 24: True IDE Mode I/O Map

-CE2	-CE1	A2	A1	A0	-IORD=L	-IOWR=L
1	0	0	0	0	Data register	Data register
1	0	0	0	1	Error register	Feature register
1	0	0	1	0	Sector count register	Sector count register
1	0	0	1	1	Sector number register	Sector number register
1	0	1	0	0	Cylinder low register	Cylinder low register
1	0	1	0	1	Cylinder high register	Cylinder high register
1	0	1	1	0	Drive head register	Drive head register
1	0	1	1	1	Status register	Command register
0	1	1	1	0	Alt. status register	Device control register
0	1	1	1	1	Drive address register	Reserved

2.4.1 Data Register

This register is a 16-bit register that has read/write ability, and it is used for transferring 1 sector data between the card and the host. This register can be accessed in word mode and byte mode. This register overlaps the Error and Feature register.

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
D0 to D15															

2.4.2 Error Register

This register is a read only register, and is used for analyzing the error content during card accessing. This register is valid when the BSY bit in Status Register and Alternate Status Register are set to "0" (Ready).

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BBK	UNC	"0"	IDNF	"0"	ABRT	'0'	AMNF

Table 25: Error Register Function

bit	Name	Function
7	BBK (Bad BlocK detected)	This bit is set when a Bad Block is detected in requested ID field.
6	UNC (Data ECC error)	This bit is set when Uncorrectable error is occurred at reading the card.
4	IDNF (ID Not Found)	The requested sector ID is in error or cannot be found.
2	ABRT (AboRTed command)	This bit is set if the command has been aborted because of the card status condition. (Not ready, Write fault, Invalid command, etc.)
0	AMNF (Address Mark Not Found)	This bit is set in case of a general error.

2.4.3 Feature Register

This register is a write only register, and provides information regarding features of the drive, which the host wishes to utilize.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Feature byte							

2.4.4 Sector Count Register

This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the card. If the value of this register is zero, a count of 256 sectors is specified. In plural sector transfer, if not successfully completed, the register contains the number of sectors, which need to be transferred in order to complete, the request. This register's initial value is "01H".

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Sector count byte							

2.4.5 Sector Number Register

This register contains the starting sector number, which is started by following sector transfer command.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Sector number byte							

2.4.6 Cylinder Low Register

This register contains the low 8-bit of the starting cylinder address, which is started by following sector transfer command.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Cylinder low byte							

2.4.7 Cylinder High Register

This register contains the high 8-bit of the starting cylinder address, which is started by following sector transfer command.

August 2013 © Wintec Industries, Inc.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Cylinder high byte							

2.4.8 Drive Head Register

This register is used for selecting the Drive number and head number for the following command.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	LBA	1	DRV	Head #			

NOTE:
1. DRV: Drive number

Table 26: Drive Head Register Function

bit	Name	Function
7	1	This bit is set to "1".
6	LBA	LBA is a flag to select either Cylinder / Head / Sector (CHS) or Logical Block Address (LBA) mode. When LBA = 0, CHS mode is selected. When LBA = 1, LBA mode is selected. In LBA mode, the Logical Block Address is interrupted as follows: LBA07 - LBA00: Sector Number Register D7 - D0. LBA15 - LBA08: Cylinder Low Register D7 - D0. LBA23 - LBA16: Cylinder High Register D7 - D0. LBA27 - LBA24: Drive / Head Register bits HS3 - HS0.
5	1	This bit is set to "1".
4	DRV (DRiVe select)	This bit is used for selecting the Master (Card 0) and Slave (Card 1) in Master/Slave organization. The card is set to be Card 0 or 1 by using DRV# of the Socket and Copy register.
3 -0	Head number	This bit is used for selecting the Head number for the following command. Bit 3 is MSB.

2.4.9 Status Register

This register is read only register, and it indicates the card status of command execution. When this register is read in configured I/O card mode (INDEX = 1, 2, 3) and level interrupt mode, -IREQ is negated. This register should be accessed in byte mode. In word mode, it is recommended that Alternate status register may be used as this register.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

Table 27: Status Register Function

bit	Name	Function
7	BSY (BuSY)	This bit is set when the card internal operation is executing. When this bit is set to "1", other bits in this register are invalid.
6	DRDY (Drive ReaDY)	If this bit and DSC bit are set to "1", the card is capable of receiving the read or write or seek requests. If this bit is set to "0", the card prohibits these requests.
5	DWF (Drive Write Full)	This bit is set if this card indicates the write fault status.
4	DSC (Drive Seek Complete)	This bit is set when the drive seek complete.
3	DRQ (Data ReQuest)	This bit is set when the information can be transferred between the host and Data register. This bit is cleared when the card receives the other command.
2	CORR (CORRected data)	This bit is set when a correctable data error has been occurred and the data has been corrected.
1	IDX (InDeX)	This bit is always set to "0".
0	ERR (ERRor)	This bit is set when the previous command has ended in some type of error. The error information is set in the other Status register or Error register. This bit is cleared by the next command.

August 2013 © Wintec Industries, Inc.

2.4.10 Alternate Status Register

This register is the same as Status register in physically, so the it assignment refers to previous item of Status register. But this register is different from Status register that –IREQ is not negated when data read.

2.4.11 Command Register

This register is write only register, and it is used for writing the command at executing the drive operation. The command code written in the command register, after the parameter is written in the Task File during the card is Ready state.

Table 28: Command Register

Command	Command Code	Used Parameter						
		FR	SC	SN	CY	DR	HD	LBA
Check power mode	E5H or 98H	N	N	N	N	Y	N	N
Execute drive diagnostic	90H	N	N	N	N	Y	N	N
Erase sector	C0H	N	Y	Y	Y	Y	Y	Y
Format track	50H	N	Y	N	Y	Y	Y	Y
Identify Drive	ECH	N	N	N	N	Y	N	N
Idle	E3H or 97H	N	Y	N	N	Y	N	N
Idle immediate	E1H or 95H	N	N	N	N	Y	N	N
Initialize drive parameters	91H	N	Y	N	N	Y	Y	N
Read buffer	E4H	N	N	N	N	Y	N	N
Read multiple	C4H	N	Y	Y	Y	Y	Y	Y
Read long sector	22H or 23H	N	N	Y	Y	Y	Y	Y
Read sector	20H or 21H	N	Y	Y	Y	Y	Y	Y
Read verify sector	40H or 41H	N	Y	Y	Y	Y	Y	Y
Recalibrate	1XH	N	N	N	N	Y	N	N
Request sense	03H	N	N	N	N	Y	N	N
Seek	7XH	N	N	Y	Y	Y	Y	Y
Set features	EFH	Y	N	N	N	Y	N	N
Set multiple mode	C6H	N	Y	N	N	Y	N	N
Set sleep mode	E6H or 99H	N	N	N	N	Y	N	N
Stand by	E2H or 96H	N	N	N	N	Y	N	N
Stand by immediate	E0H or 94H	N	N	N	N	Y	N	N
Translate sector	87H	N	Y	Y	Y	Y	Y	Y
Wear level	F5H	N	N	N	N	Y	Y	N
Write buffer	E8H	N	N	N	N	Y	N	N
Write long sector	32H or 33H	N	N	Y	Y	Y	Y	Y
Write multiple	C5H	N	Y	Y	Y	Y	Y	Y
Write multiple w/o erase	CDH	N	Y	Y	Y	Y	Y	Y
Write sector	30H or 31H	N	Y	Y	Y	Y	Y	Y
Write sector w/o erase	38H	N	Y	Y	Y	Y	Y	Y
Write verify	3CH	N	Y	Y	Y	Y	Y	Y

NOTE:

FR: Feature register
SC: Sector Count register
SN: Sector Number register
CY: Cylinder register
DR: DRV bit of Drive Head register
HD: Head Number of Drive Head register
LBA: Logical Block Address Mode Supported
Y: The register contains a valid parameter for this command
N: The register does not contain a valid parameter for this command.

2.4.12 Device Control Register

This register is write only register, and it is used for controlling the card interrupt request and issuing an ATA soft reset to the card.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
				1	SRST	nIEN	0

Table 29: Device Control Register Function

bit	Name	Function
7 -4		Don't care
3	1	This bit is set to "1".
2	SRST (Software ReSeT)	This bit is set to "1" in order to force the card to perform Task File Reset operation. This does not change the Card Configuration registers as a Hardware Reset does. The card remains in Reset until this bit is reset to "0".
1	nIEN (Interrupt ENable)	This bit is used for enabling –IREQ. When this bit is set to "0", –IREQ is enabled. When this bit is set to "1", –IREQ is disabled.
0	0	This bit is set to "0".

2.4.13 Drive Address Register

This register is read only register, and it is used for confirming the drive status. This register is provided for compatibility with the AT disk drive interface. It is recommended that this register be not mapped into the host's I/O space because of potential conflicts on bit7.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	nWTG	nHS3	nHS2	nHS1	nHS0	nDS1	nDS0

Table 30: Drive Address Register Function

bit	Name	Function
7		This bit is unknown.
6	nWTG (WriTing Gate)	This bit is unknown.
5 -2	nHS3 -0(Head Select3 - 0)	These bits are the negative value of Head Select bits (bit 3 to 0) in Drive/Head register.
1	nDS1 (Idrive Select1)	This bit is unknown.
0	nDS0 (Idrive Select0)	This bit is unknown.

2.5 ATA Command Specification

This table summarizes the ATA command set with the paragraphs. Following shows the support commands and command codes, which are written in, command registers.

Table 31: ATA Command Set

No.	Command	Command Code	FR	SC	SN	CY	DR	HD	LBA
1	Check power mode	E5H or 98H	-	-	-	-	Y	-	-
2	Execute drive diagnostic	90H	-	-	-	-	Y	-	-
3	Erase sector	C0H	-	Y	Y	Y	Y	Y	Y
4	Format track	50H	-	Y	-	Y	Y	Y	Y
5	Identify Drive	ECH	-	-	-	-	Y	-	-
6	Idle	E3H or 97H	-	Y	-	-	Y	-	-
7	Idle immediate	E1H or 95H	-	-	-	-	Y	-	-
8	Initialize drive parameters	91H	-	Y	-	-	Y	Y	-

August 2013 © Wintec Industries, Inc.