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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Winbond Clock Generator
W83115RG-BW
W83115WG-BW
For INTEL Broadwater Chipset

Date: Dec./2006 Revision: 1.0

Winbond Electronics Corp.

STEPLESS FOR INTEL BROADWATER CLOCK GENERATOR

W83115RG-BW/W83115WG-BW Datasheet Revision History

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
1	n.a.	03/06/2006	0.5	n.a.	All of the versions before 0.50 are for internal use.
2	1,3-5,16	04/06/2006	0.51	n.a.	Modify some description in blue text.
3	2,3	05/18/2006	0.6	n.a.	Add DOTSEL$^{\&}$ hardware trapping pin.
4	6	06/06/2006	0.61	n.a.	Change default value about DOT96_SEL.
5		12/13/2006	1.0	n.a.	All of the versions before 1.0 are preliminary version
6					
7					
8					
9					
10					

Winbond Electronics Corp.

STEPLESS FOR INTEL BROADWATER CLOCK GENERATOR

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STEPLESS FOR INTEL BROADWATER CLOCK GENERATOR

1. GENERAL DESCRIPTION

The W83115RG-BW/W83115WG-BW is a Clock Synthesizer for Intel Broadwater series chipsets. W83115RG-BW/ W83115WG-BW provides all clocks required for the high-speed microprocessor and provides step-less frequency programming and 32 different frequencies of CPU, PCI, and SRC clocks setting, support SATA and DOT clock outputs, all clocks are externally selectable with smooth transitions.

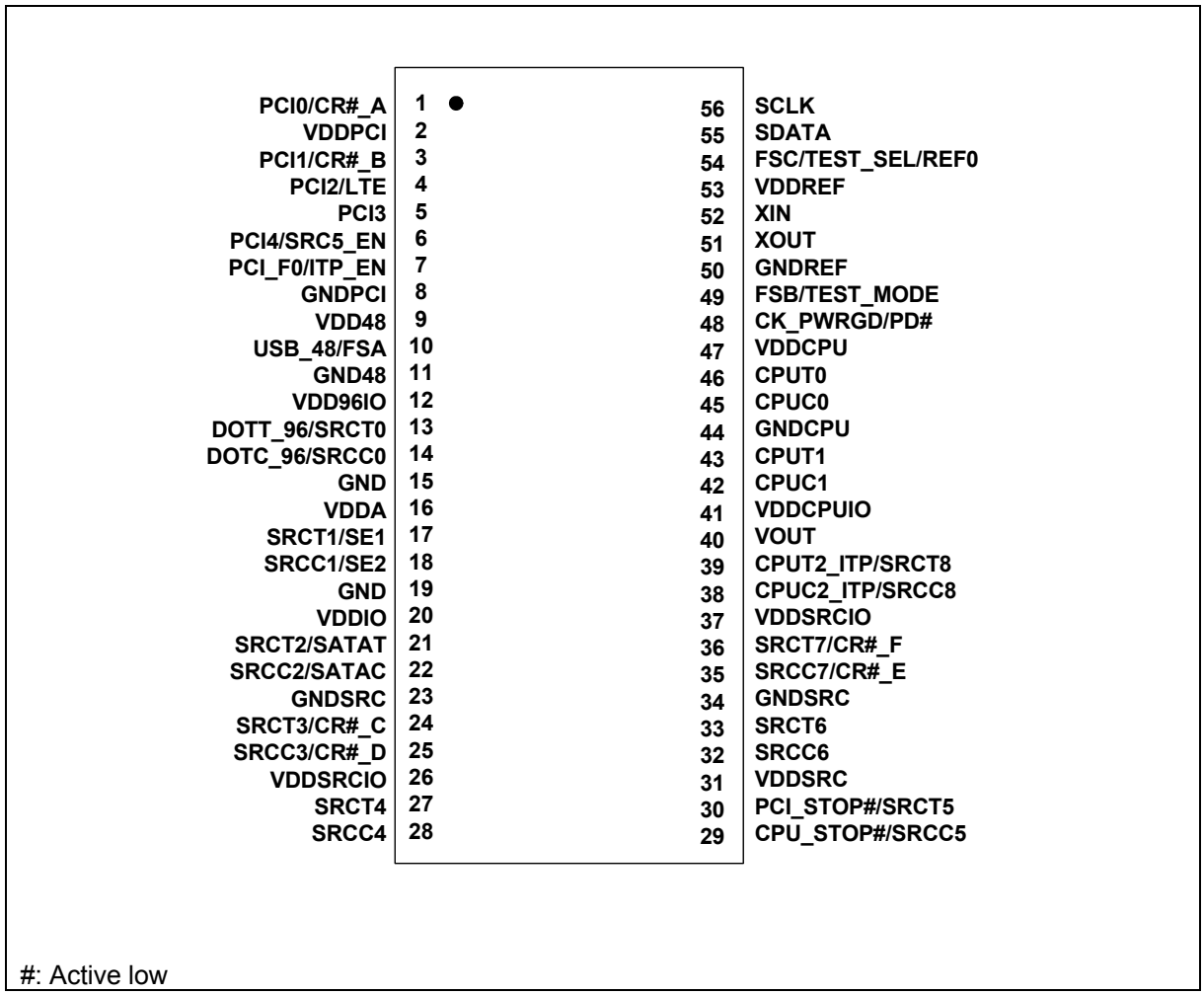
The W83115RG-BW/W83115WG-BW provides I^2C serial bus interface to program the registers to enable or disable each clock outputs and provides -0.5% down type spread spectrum or programmable S.S.T. scale to reduce EMI.

The W83115RG-BW/W83115WG-BW accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply.

2. PRODUCT FEATURES

- 2 pair push-pull Differential clock outputs for CPU.
- 7 pair push-pull Differential clock outputs for SRC.
- 1 pair push-pull Differential clock outputs for CPU/SRC selectable.
- 1 pair push-pull Differential clock outputs for DOT/SRC selectable.
- 5 PCI clock outputs, 1 free running.
- 1 48 MHz clock output for USB.
- 1 14.318MHz REF clock output.
- Smooth frequency switch with selections from 100 to 400MHz.
- Step-less frequency programming.
- I^2C 2-wire serial interface and support byte read/write and block read/write.
- -0.5% down type spread spectrum in H/W and software select mode.
- Programmable S.S.T. scale to reduce EMI in M/N mode.
- Programmable registers to enable/disable each output and select modes.
- Programmable clock outputs slew rate control and skew control.
- 56 pins TSSOP/SSOP package.

3. PIN CONFIGURATION



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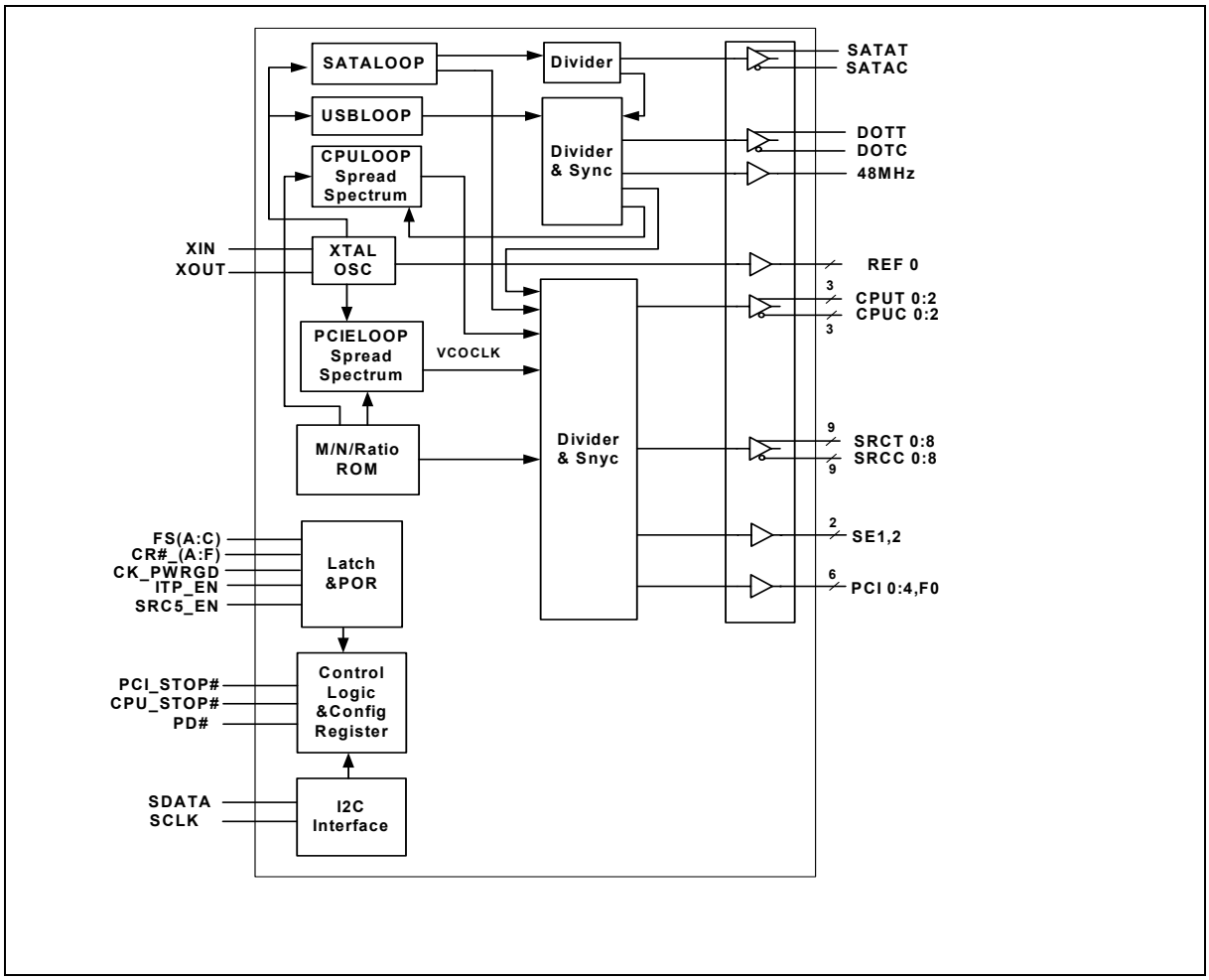
4. BLOCK DIAGRAM



5. PIN DESCRIPTION

PIN	PIN NAME	TYPE	DESCRIPTION
1	PCI0/CR#_A	I/O	PCI0 clock output or CLKREQ# control for either SRC0 or SRC2 pair
2	VDDPCI	PWR	Power supply for PCI
3	PCI1/CR#_B	I/O	PCI1 clock output or CLKREQ# control for either SRC1 or SRC4 pair
4	PCI2/LTE	I/O	PCI2 clock output and LTE strap
5	PCI3	OUT	PCI3 clock output
6	PCI4/SRC5_EN	I/O	PCI4 clock output and SRC5 enable strap (1=select SRC5 pair)
7	PCIF0/ITP_EN	I/O	PCIF0 free running clock output, ITP enable strap (1=select ITP pair)
8	GNDPCI	PWR	Ground pin
9	VDD48	PWR	Power supply for USB_48
10	USB_48/FSA	I/O	48MHz USB clock and FSA CPU frequency select
11	GND48	PWR	Ground pin
12	VDD96IO	PWR	Low voltage I/O power supply
13	DOTT_96/SRCT0	OUT	0.8V clock outputs for DOTT or SRCT0
14	DOTC_96/SRCC0	OUT	0.8V clock outputs for DOTC or SRCC0
15	GND	PWR	Ground pin
16	VDDA	PWR	Power supply for core
17	SRCT1/SE1	OUT	0.8V clock outputs for SRCT1 or 3.3V SE clock output
18	SRCC1/SE2	OUT	0.8V clock outputs for SRCC1 or 3.3V SE clock output
19	GND	PWR	Ground pin
20	VDDIO	PWR	Low voltage I/O power supply
21	SRCT2/SATAT	OUT	0.8V clock outputs for SRCT2 or SATAT
22	SRCC2/SATAC	OUT	0.8V clock outputs for SRCC2 or SATAC
23	GNDSRC	PWR	Ground pin
24	SRCT3/CR#_C	I/O	0.8V clock output for SRCT3 or CLKREQ# control for either SRC0 or SRC2 pair
25	SRCC3/CR#_D	I/O	0.8V clock output for SRCC3 or CLKREQ# control for either SRC1 or SRC4 pair
26	VDDSRCIO	PWR	Low voltage I/O power supply

PIN DESCRIPTION, continued.

PIN	PIN NAME	TYPE	DESCRIPTION
27	SRCT4	OUT	0.8V clock outputs for SRCT4
28	SRCC4	OUT	0.8V clock outputs for SRCC4
29	CPU_STOP#/SRCC5	I/O	CPU_STOP# or 0.8V clock output for SRCC5
30	PCI_STOP#/SRCT5	I/O	PCI_STOP# or 0.8V clock output for SRCT5
31	VDDSRC	PWR	Power supply for core
32	SRCC6	OUT	0.8V clock output for SRCC6
33	SRCT6	OUT	0.8V clock output for SRCT6
34	GNDSRC	PWR	Ground pin
35	SRCC7/CR#_E	I/O	0.8V clock output for SRCC7 or CLKREQ# control for SRC6 pair
36	SRCT7/CR#_F	I/O	0.8V clock output for SRCT7 or CLKREQ# control for SRC8 pair
37	VDDSRCIO	PWR	Low voltage I/O power supply for SRC
38	CPUC2_ITP/SRCC8	OUT	0.8V clock output for CPUC2_ITP or SRCC8
39	CPUT2_ITP/SRCT8	OUT	0.8V clock output for CPUT2_ITP or SRCT8
40	VOUT	PWR	Integrated linear regulator voltage control
41	VDDCPUIO	PWR	Low voltage I/O power supply for CPU
42	CPUC1	OUT	0.8V clock outputs for CPUC1
43	CPUT1	OUT	0.8V clock outputs for CPUT1
44	GNDCPU	PWR	Ground pin
45	CPUC0	OUT	0.8V clock outputs for CPUC0
46	CPUT0	OUT	0.8V clock outputs for CPUT0
47	VDDCPU	PWR	Power supply for core
48	CK_PWRGD/PD#	IN	Notifies CK505 to sample latched input or power down mode
49	FSB/TEST_MODE	IN	FSB CPU frequency select or entry to test mode input
50	GNDREF	PWR	Ground pin
51	XOUT	OUT	Crystal output at 14.318MHz nominally with internal loading capacitors (18pF).

PIN DESCRIPTION, continued.

PIN	PIN NAME	TYPE	DESCRIPTION
52	XIN	IN	Crystal input with internal loading capacitors (18pF) and feedback resistors.
53	VDDREF	PWR	Power supply for REF
54	FSC/TEST_SEL/REF0	I/O	14.318MHz REF clock and FSC CPU frequency select or test_sel
55	SDATA	I/O	Serial data of I^2C 2-wire control interface.
56	SCLK	IN	Serial clock of I^2C 2-wire control interface.

6. FREQUENCY SELECTION BY HARDWARE OR SOFTWARE

This frequency table is used at power on latched FS [2:0] value or software programming at SSEL [4:0] (Register 13 bit 7 ~ 3). If FS [2:0] no any external circuit to modify power on status the Gray shading is Hardware default frequency.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	CPU (MHZ)	SRC (MHZ)	SATA (MHZ)	PCI (MHZ)
FS4	FS3	FS2	FS1	FS0				
0	0	0	0	0	266.68	100.00	100.00	33.33
0	0	0	0	1	133.34	100.00	100.00	33.33
0	0	0	1	0	200.01	100.00	100.00	33.33
0	0	0	1	1	166.68	100.01	100.00	33.34
0	0	1	0	0	333.36	100.01	100.00	33.34
0	0	1	0	1	100.00	100.00	100.00	33.33
0	0	1	1	0	400.01	100.00	100.00	33.33
0	0	1	1	1	233.33	100.00	100.00	33.33
0	1	0	0	0	266.97	100.12	100.00	33.37
0	1	0	0	1	133.93	100.45	100.00	33.48
0	1	0	1	0	200.90	100.45	100.00	33.48
0	1	0	1	1	166.86	100.12	100.00	33.37
0	1	1	0	0	333.72	100.12	100.00	33.37
0	1	1	0	1	100.90	100.90	100.00	33.63
0	1	1	1	0	400.91	100.23	100.00	33.41
0	1	1	1	1	233.86	100.23	100.00	33.41
1	0	0	0	0	266.68	100.00	100.00	33.33
1	0	0	0	1	133.34	100.00	100.00	33.33
1	0	0	1	0	200.01	100.00	100.00	33.33
1	0	0	1	1	166.68	100.01	100.00	33.34
1	0	1	0	0	333.36	100.01	100.00	33.34
1	0	1	0	1	100.00	100.00	100.00	33.33
1	0	1	1	0	400.01	100.00	100.00	33.33
1	0	1	1	1	233.33	100.00	100.00	33.33
1	1	0	0	0	266.97	100.12	100.00	33.37
1	1	0	0	1	133.93	100.45	100.00	33.48
1	1	0	1	0	200.90	100.45	100.00	33.48
1	1	0	1	1	166.86	100.12	100.00	33.37
1	1	1	0	0	333.72	100.12	100.00	33.37
1	1	1	0	1	100.90	100.90	100.00	33.63
1	1	1	1	0	400.91	100.23	100.00	33.41
1	1	1	1	1	233.86	100.23	100.00	33.41

7. I²C CONTROL AND STATUS REGISTERS

PWD: Power on default value

7.1 Register 0: (Default : X1h)

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	AFFECTED PIN / FUNCTION DESCRIPTION	TYPE
7	FSC	X	Frequency table select bits.	Latch
6	FSB	X		
5	FSA	X		
4	IAMT_EN	0	0 : Legacy mode 1 : iMAT mode, Sticky 1 Set via SMBus or dynamically by combination of PWRDWN, CPUSTOP_N and PCISTOP_N. Sticky 1 : Mean that once written to a '1' cannot be cleared until power is removed.	R/W
3	PCIELOOP_EN	0	Activate PCIELOOP 1 : Enable 0 : Disable	R/W
2	SRC_SYNC_N	0	Sync SRC clock to CPU 1 : Async, SRC come from PCIELOOP 0 : Sync, SRC come from CPULOOP	R/W
1	FIX_SATA	0	Sync SATA clock to SRCs 1 : Async, SATA fix at 100M 0 : Sync, SATA follow SRC clocks	R/W
0	PD_RESTORE	1	Save last configuration status in power down mode 1 : Save final configuration 0 : Clear final configuration & return to power on default.	R/W

7.2 Register 1: (Default : 83h)

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	DOT96_SEL	1	Select SRC0 or DOT96 0 : SRC0 1 : DOT96 (Default)	R/W
6	PLL1_SST_CEN_SEL	0	Down spread or center spread to total 0.5% for CPULOOP 1: Center 0: Down	R/W
5	PLL3_SST_CEN_SEL	0	Down spread or center spread to total 0.5% for PCIELOOP 1: Center 0: Down	R/W
4	PLL3_QCFB<3>	0	PLL3 quick configuration bits <3:0> See Table2. & Set Reg0-bit3 = 1 prior to selecting these bits except 0000 & 0001.	R/W
3	PLL3_QCFB<2>	0		
2	PLL3_QCFB<1>	0		
1	PLL3_QCFB<0>	1		
0	FIX_PCI_N	1	Sync PCI clock to CPU 0 : Async, PCI fix at 33.33M 1 : PCI follow SRC clocks	R/W

7.3 Register 2: (Default : FFh)

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	REFEN	1	REF output control 1: Output enable 0: Output disable	R/W
6	USB48EN	1	USB48 output control 1: Output enable 0: Output disable	R/W
5	PCIF5EN	1	PCIF5 output control 1: Output enable 0: Output disable	R/W
4	PCIEN<4>	1	PCI4 output control 1: Output enable 0: Output disable	R/W

Register 2: (Default : FFh), continued.

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
3	PCIEN<3>	1	PCI3 output control 1: Output enable 0: Output disable	R/W
2	PCIEN<2>	1	PCI2 output control 1: Output enable 0: Output disable	R/W
1	PCIEN<1>	1	PCI1 output control 1: Output enable 0: Output disable	R/W
0	PCIEN<0>	1	PCI0 output control 1: Output enable 0: Output disable	R/W

7.4 Register 3: (Default : FFh)

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	SRCEN<11>	1	SRC11 output control 1: Output enable 0: Output disable	R/W
6	SRCEN<10>	1	SRC10 output control 1: Output enable 0: Output disable	R/W
5	SRCEN<9>	1	SRC9 output control 1: Output enable 0: Output disable	R/W
4	SRCEN<8>	1	SRC8 or CPU2_ITP output control 1: Output enable 0: Output disable	R/W
3	SRCEN<7>	1	SRC7 output control 1: Output enable 0: Output disable	R/W
2	SRCEN<6>	1	SRC6 output control 1: Output enable 0: Output disable	R/W
1	SRCEN<5>	1	SRC5 output control 1: Output enable 0: Output disable	R/W
0	SRCEN<4>	1	SRC4 output control 1: Output enable 0: Output disable	R/W

7.5 Register 4: (Default : FFh)

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	SRCEN<3>	1	SRC3 output control 1: Output enable 0: Output disable	R/W
6	SRCEN<2>	1	SRC2 or SATA output control 1: Output enable 0: Output disable	R/W
5	SRCEN<1>	1	SRC1 output control 1: Output enable 0: Output disable	R/W
4	SRCEN<0>	1	SRC0 or DOT96 output control 1: Output enable 0: Output disable	R/W
3	CPUEN<1>	1	CPU1 output control 1: Output enable 0: Output disable	R/W
2	CPUEN<0>	1	CPU0 output control 1: Output enable 0: Output disable	R/W
1	SS1_EN	1	Spread spectrum enable for CPULOOP 1: Enable 0: Disable	R/W
0	SS3_EN	1	Spread spectrum enable for PCIELOOP 1: Enable 0: Disable	R/W

7.6 Register 5: (Default : 00h)

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	CR#_A_EN	0	Enable CR#_A (clock request) feature 1: Enable =>configure PCI0/CR#_A as input pin, CR#_A. =>Set Reg2-Bit0 to 0, disable PCI0 clock output, prior to activate this feature 0 : Disable keep PCI0/CR#_A as output pin, PCI0.	R/W
6	CR#_A_SEL	0	Select SRC0 or SRC2 to be controlled by CR#_A. 1: SRC2 0: SRC0	R/W
5	CR#_B_EN	0	Enable CR#_B (clock request) feature 1: Enable =>configure PCI1/CR#_B as input pin, CR#_B. =>Set Reg2-Bit1 to 0, disable PCI1 clock output, prior to activate this feature 0 : Disable keep PCI1/CR#_B as output pin, PCI1.	R/W
4	CR#_B_SEL	0	Select SRC1 or SRC4 to be controlled by CR#_B. 1: SRC4 0: SRC1	R/W
3	CR#_C_EN	0	Enable CR#_C (clock request) feature 1: Enable =>configure SRC3T/CR#_C as input pin, CR#_C. =>Set Reg4-Bit7 to 0, disable SRC3 clock output, prior to activate this feature 0 : Disable keep SRC3T/CR#_C as output pin, SRC3T.	R/W
2	CR#_C_SEL	0	Select SRC2 or SRC0 to be controlled by CR#_C. 1: SRC2 0: SRC0	R/W
1	CR#_D_EN	0	Enable CR#_D (clock request) feature 1: Enable =>configure SRC3C/CR#_D as input pin, CR#_D. =>Set Reg4-Bit7 to 0, disable SRC3 clock output, prior to activate this feature 0 : Disable, Keep SRC3C/CR#_D as output pin,SRC3C.	R/W
0	CR#_D_SEL	0	Select SRC4 or SRC1 to be controlled by CR#_D. 1: SRC4 0: SRC1	R/W

7.7 Register 6: (Default : 0Ch)

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	CR#_E_EN	0	Enable CR#_E (clock request) feature for SRC6 1: Enable =>configure SRC7C/CR#_E as input pin, CR#_E. =>Set Reg3-Bit3 to 0, disable SRC7 clock output, prior to activate this feature 0 : Disable keep SRC7C/CR#_E as output pin, SRC7C.	R/W
6	CR#_F_EN	0	Enable CR#_F (clock request) feature for SRC8 1: Enable =>configure SRC7T/CR#_F as input pin, CR#_F. =>Set Reg3-Bit3 to 0, disable SRC7 clock output, prior to activate this feature 0 : Disable keep SRC7T/CR#_F as output pin, SRC7C.	R/W
5	CR#_G_EN	0	Enable CR#_G (clock request) feature for SRC9 1: Enable =>configure SRC11C/CR#_G as input pin, CR#_G. =>Set Reg3-Bit7 to 0, disable SRC11 clock output, prior to activate this feature 0 : Disable, keep SRC11C/CR#_G as output pin, SRC11C.	R/W
4	CR#_H_EN	0	Enable CR#_H (clock request) feature for SRC10 1: Enable =>configure SRC11T/CR#_H as input pin, CR#_H. =>Set Reg3-Bit7 to 0, disable SRC11 clock output, prior to activate this feature 0:Disable, keep SRC11T/CR#_H as output pin, SRC11T.	R/W
3	Reserved	1		R/W
2	Reserved	1		R/W
1	SRC1_FR_N	0	SRC1 free running control 1 : Stoppable with PCI_STOP# assertion 0 : Free running	R/W
0	SRCs_FR_N	0	SRCs free running control 1 : Stoppable with PCI_STOP# assertion 0 : Free running	R/W

7.8 Register 7: Winbond Chip ID – Project Code Register (Default : 04h)

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	CHIP_ID [7]	0	Winbond Chip ID. W83115RG/WG-BW	R
6	CHIP_ID [6]	0	Winbond Chip ID.	R
5	CHIP_ID [5]	0	Winbond Chip ID.	R
4	CHIP_ID [4]	0	Winbond Chip ID.	R
3	CHIP_ID [3]	0	Winbond Chip ID.	R
2	CHIP_ID [2]	1	Winbond Chip ID.	R
1	CHIP_ID [1]	0	Winbond Chip ID.	R
0	CHIP_ID [0]	0	Winbond Chip ID.	R

7.9 Register 8: (Default : 0Ch)

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	DEVICE_ID [3]	0	0001 : 64TSSOP 0000 : 56TSSOP	R
6	DEVICE_ID [2]	0		
5	DEVICE_ID [1]	0		
4	DEVICE_ID [0]	0		
3	Reserved	1		R/W
2	Reserved	1		R/W
1	SE1EN	0	Single-ended pin17 output enable 1 : Enable 0 : Disable	R/W
0	SE2EN	0	Single-ended pin18 output enable 1 : Enable 0 : Disable	R/W

7.10 Register 9: (Default : 25h)

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	PCIF5_FR_N	0	PCIF5 free running control 1 : Stoppable with PCI_STOP# assertion 0 : Free running	R/W
6	LTE_RB	0	LTE pin strap value 0 : allow over-clocking 1 : forbid over-clocking	Latch
5	Reserved	1		R/W
4	TEST_SEL	0	Allow to select output status 0 : All outputs are tri-state 1 : All outputs are REF/N besides REF clock	R/W
3	TEST_ENTRY	0	Allow to entry test mode 0 : Normal operation 1 : Entry test mode	R/W
2	IO_RAIL<2>	1	Programmable VDDXXX_IO 111 : 1.0V 110 : 0.9V 101 : 0.8V 100 : 0.7V others : 0.6V	R/W
1	IO_RAIL<1>	0		
0	IO_RAIL<0>	1		

7.11 Register 10: (Default : D0h)

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	NVAL<8>	1	Programmable N divisor value for CPU frequency. Bit 7 ~0 are defined in the Register 11.	R/W
6	NVAL<9>	1		
5	NVAL<10>	0		
4	MVAL<4>	1	Programmable M divisor for CPU frequency. Default value follow FS=2 (01_0000 = 16)	R/W
3	MVAL<3>	0		
2	MVAL<2>	0		
1	MVAL<1>	0		
0	MVAL<0>	0		

7.12 Register 11: (Default : 7Ah)

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	NVAL<7>	0	Programmable N divisor for CPU frequency. The bit 8,9,10 is defined in Register 10. Default value follow FS=2 (011_0111_1010 =894-4)	R/W
6	NVAL<6>	1		
5	NVAL<5>	1		
4	NVAL<4>	1		
3	NVAL<3>	1		
2	NVAL<2>	0		
1	NVAL<1>	1		
0	NVAL<0>	0		

7.13 Register 12: (Default : 7Ah)

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	N3VAL<7>	0	Programmable N divisor for SRC frequency. SRC programmable range is 115M ~ 86M.	R/W
6	N3VAL<6>	1		
5	N3VAL<5>	1		
4	N3VAL<4>	1		
3	N3VAL<3>	1		
2	N3VAL<2>	0		
1	N3VAL<1>	1		
0	N3VAL<0>	0		

7.14 Register 13: (Default : 10h)

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	SSEL<4>	0	Software frequency table selection through I^2C	R/W
6	SSEL<3>	0		
5	SSEL<2>	0		
4	SSEL<1>	1		
3	SSEL<0>	0		
2	EN_SSEL	0	Enable software table selection FS[4:0]. 0 = Hardware table setting (Jump mode). 1 = Software table setting through Bit7~3 . (Jumpless mode)	R/W
1	Reserved	0		R/W
0	ITP_EN	0	Select SRC8 or CPU2_ITP clock 0: to select the SRC8 clock 1: to select the CPU2_ITP clock	R/W

7.15 Register 14: (Default : 04h)

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	Reserved	0		R/W
6	Reserved	0		R/W
5	SATA_SSC_EN	0	Enable spread spectrum to SATA with –0.5%, only valid in SRCs over-clocking mode. 1 : Enable 0 : Disable	
4	PCIEMN_EN	0	Enable programming PCIE frequency	R/W
3	CPUMN_EN	0	Enable programming CPU frequency	R/W
2	SW_PCISTOP_N	1	Software PCISTOP function 0 : Stop all STOPPABLE PCI,PCIF and SRC clock with no glitches. 1 : Resume all STOPED PCI,PCIF and SRC clock with no glitches.	R/W
1	SRC5_EN	0	Configure the input/output function of SRC5T/PCISTOP_N and SRC5C/PCISTOP_N 1 : Output feature, SRC5. 0 : Input feature, PCISTOP_N & CPUSTOP_N.	Latch R
0	FSD	0	Frequency table select bit.	Latch R

7.16 Register 15: (Default : 0Bh)

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	SPH VAL1<3>	0	Spread Spectrum Up Counter bit 3 ~ bit 0 for CPULOOP .	R/W
6	SPH VAL1<2>	0		
5	SPH VAL1<1>	0		
4	SPH VAL1<0>	0		
3	SPL VAL1<3>	1	Spread Spectrum Down Counter bit 3 ~ bit 0 for CPULOOP. 2's complement representation. Ex: 1 -> 1111 ; 2 -> 1110 ; 7 -> 1001 ; 8 -> 1000	
2	SPL VAL1<2>	0		
1	SPL VAL1<1>	1		
0	SPL VAL1<0>	1		

7.17 Register 16: (Default : 30h)

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	INV_CPU	0	Invert the CPUCLKT1/0 phase 0: Default 1: Inverse	R/W
6	INV_SRC	0	Invert the SRCCLKT phase 0: Default 1: Inverse	R/W
5	SPCNT1<5>	1	Spread Spectrum Programmable time, the resolution is 280ns. Default period is 11.8us	R/W
4	SPCNT1<4>	1		
3	SPCNT1<3>	0		
2	SPCNT1<2>	0		
1	SPCNT1<1>	0		
0	SPCNT1<0>	0		

7.18 Register 17: (Default : 0Bh)

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	Reserved	0		R/W
6	Reserved	0		R/W
5	SPL VAH3<5>	0	Spread Spectrum DOWN Counter bit5 ~ bit 0 for PCIEXLOOP. 2's complement representation. Ex: 1 -> 111111 ; 2 -> 111110 ; 7 ->111001 ; 8 -> 111000	
4	SPL VAH3<4>	0		
3	SPL VAH3<3>	1		
2	SPL VAH3<2>	0		
1	SPL VAH3<1>	1		
0	SPL VAH3<0>	1		

7.19 Register 18: (Default : 00h)

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	Reserved	0		R/W
6	Reserved	0		R/W
5	SPH VAH3<5>	0	Spread Spectrum UP Counter bit5 ~ bit 0 for PCIEXLOOP. 2's complement representation. Ex: 1 -> 111111 ; 2 -> 111110 ; 7 -> 111001 ; 8 -> 111000	
4	SPH VAH3<4>	0		
3	SPH VAH3<3>	0		
2	SPH VAH3<2>	0		
1	SPH VAH3<1>	0		
0	SPH VAH3<0>	0		

7.20 Register 19: (Default : 30h)

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	INV_PCI	0	Invert the PCICLK phase 0: Default 1: Inverse	R/W
6	INV_USB48	0	Invert the USB48M phase 0: Default 1: Inverse	R/W
5	SPCNT3<5>	1	Spread Spectrum Programmable time, the resolution is 280ns. Default period is 11.8us	R/W
4	SPCNT3<4>	1		
3	SPCNT3<3>	0		
2	SPCNT3<2>	0		
1	SPCNT3<1>	0		
0	SPCNT3<0>	0		

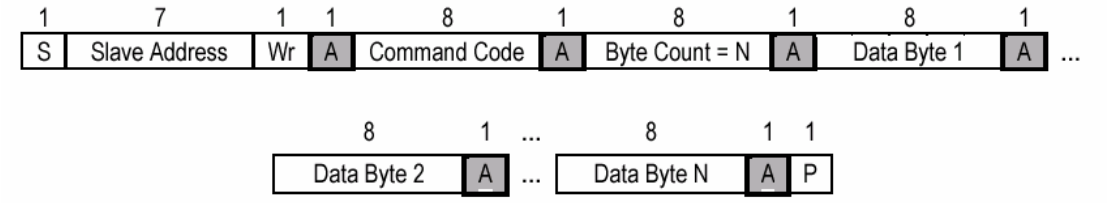
TABLE 2 : PIN17,18 (SRCT1/SE1, SRCC1/SE2) FREQ CONFIGURATION BASED ON PCIELOOP								
R1B4	R1B3	R1B2	R1B1	PIN17 (MHZ)	PIN18 (MHZ)	SPREAD (%)	CLOCK TYPE	COMMENT
0	0	0	0	100	100	-	Differential	PCIELOOP disable
0	0	0	1	100	100	0.5% down	Differential	SRC1 follow SRCs
0	0	1	0	100	100	0.5% down	Differential	SRC1 come from PCIELOOP
0	0	1	1	100	100	1% down	Differential	SRC1 come from PCIELOOP
0	1	0	0	100	100	1.5% down	Differential	SRC1 come from PCIELOOP
0	1	0	1	100	100	2% down	Differential	SRC1 come from PCIELOOP
0	1	1	0	100	100	2.5% down	Differential	SRC1 come from PCIELOOP
0	1	1	1	-	-	-	-	-
1	0	0	0	24.576	24.576	Non	Single End	-
1	0	0	1	24.576	98.304	Non	Single End	-
1	0	1	0	98.304	98.304	Non	Single End	-
1	0	1	1	27	27	Non	Single End	-
1	1	0	0	25	25	Non	Single End	-
1	1	0	1	-	-	-	-	-
1	1	1	0	-	-	-	-	-
1	1	1	1	-	-	-	-	-

8. ACCESS INTERFACE

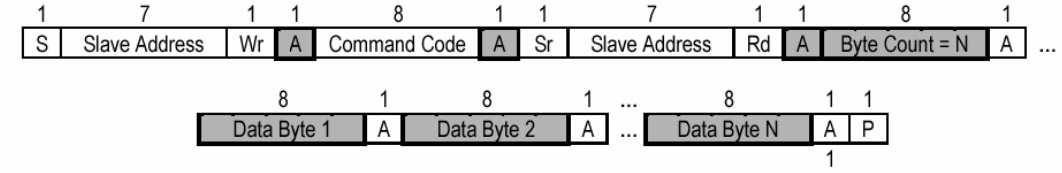
The W83115RG-BW/W83115WG-BW provides I^2C Serial Bus for microprocessor to read/write internal registers. In the W83115RG-BW/W83115WG-BW is provided Block Read/Block Write and Byte-Data Read/Write protocol. The I^2C address is defined at 0xD2.
The register number is increased by one if using byte data read/write protocol.

Example: In block mode, byte number of program register is 1
In byte mode, byte number of program register is 2 (Byte number of block mode +1)

8.1 Block Write protocol

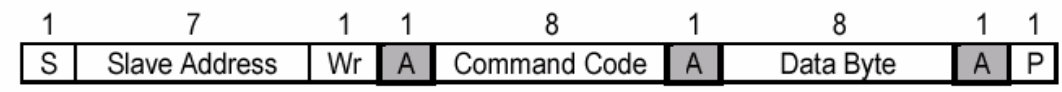


8.2 Block Read protocol

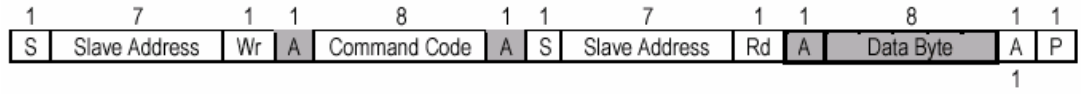


In block mode, the command code must filled 8'h00

8.3 Byte Write protocol



8.4 Byte Read protocol



9. SPECIFICATIONS

9.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or VDD).

PARAMETER	RATING
Absolute 3.3V Core Supply Voltage	-0.5V to +4.6V
Absolute 3.3V I/O Supple Voltage	- 0.5V to + 4.6V
Operating 3.3V Core Supply Voltage	3.135V to 3.465V
Operating 3.3V I/O Supple Voltage	3.135V to 3.465V
Absolute VDDIO Core Supply Voltage	-0.5V to +3.8V
Absolute VDDIO I/O Supple Voltage	- 0.5V to + 3.8V
Operating VDDIO Core Supply Voltage	0.7V to 0.9V
Operating VDDIO I/O Supple Voltage	0.7V to 0.9V
Storage Temperature	- 65°C to + 150°C
Ambient Temperature	- 55°C to + 125°C
Operating Temperature	0°C to + 70°C
Input ESD protection (Human body model)	2000V

9.2 General Operating Characteristics

VDD= 3.3V ± 5 %, TA = 0℃ to +70℃,					
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Input Low Voltage	V_{IL}		0.8	V_{dc}	
Input High Voltage	V_{IH}	2.0		V_{dc}	
Output Low Voltage	V_{OL}		0.4	V_{dc}	
Output High Voltage	V_{OH}	2.4		V_{dc}	
Operating Supply Current	I_{dd}		350	mA	CPU = 100 to 400 MHz PCI = 33.3 Mhz with load
Input pin capacitance	Cin		5	pF	
Output pin capacitance	Cout		6	pF	
Input pin inductance	Lin		7	nH	