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Winbond Clock Generator

W83195BR-118/W83195BG-118

For Intel 915/945 Chipsets

Date: May/02/2006 Revision: 0.81

W83195BR-118 Datasheet Revision History

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
1	n.a.	07/22/2004	0.5	n.a.	All of the versions before 0.50 are for internal use.
2	8,13	11/24/2004	0.6	n.a.	Correction IC version, add register default value and correction some description and default value
3	11,13	01/05/2005	0.7	n.a	Add spread spectrum function control bit, and correction some description and default value
4	19	01/17/2005	0.71	n.a	Add Pb-free part number
5	1-4,10-12,14-16	3/25/2005	0.8	n.a	Refine the description and register value
6	All	05/02/2006	0.81	n.a.	Change the part no from W83195BR-119 to W83195BR-118
7					
8					
9					

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STEPLESS FOR INTEL 915/945 CHIPSETS

1. GENERAL DESCRIPTION

The W83195BR-118 is a Clock Synthesizer for Intel P4 processors and Intel Grandsdale chipsets. W83195BR-118 provides all clocks required for high-speed microprocessor and provides step-less frequency programming, 32 different frequencies of CPU, PCI, PCI-Express clocks setting. Simultaneously W83195BR-118 supports SRC 100MHz for SATA and DOT 96MHz clock outputs for integrated graphic chipsets. All clocks are externally selectable with smooth transitions.

The W83195BR-118 programs the registers to enable or disable each clock outputs through I^2C serial bus interface and provides -0.5% down type spread spectrum or programmable spread spectrum scale to reduce EMI.

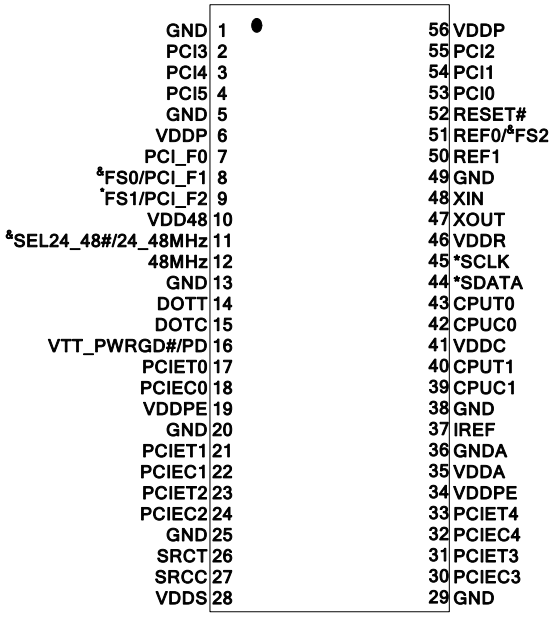
The W83195BR-118 also has watchdog timer and reset output pin to support auto-reset when systems hanging caused by improper frequency setting.

The W83195BR-118 is driven with a 14.318 MHz reference crystal and runs on a 3.3V supply.

2. PRODUCT FEATURES

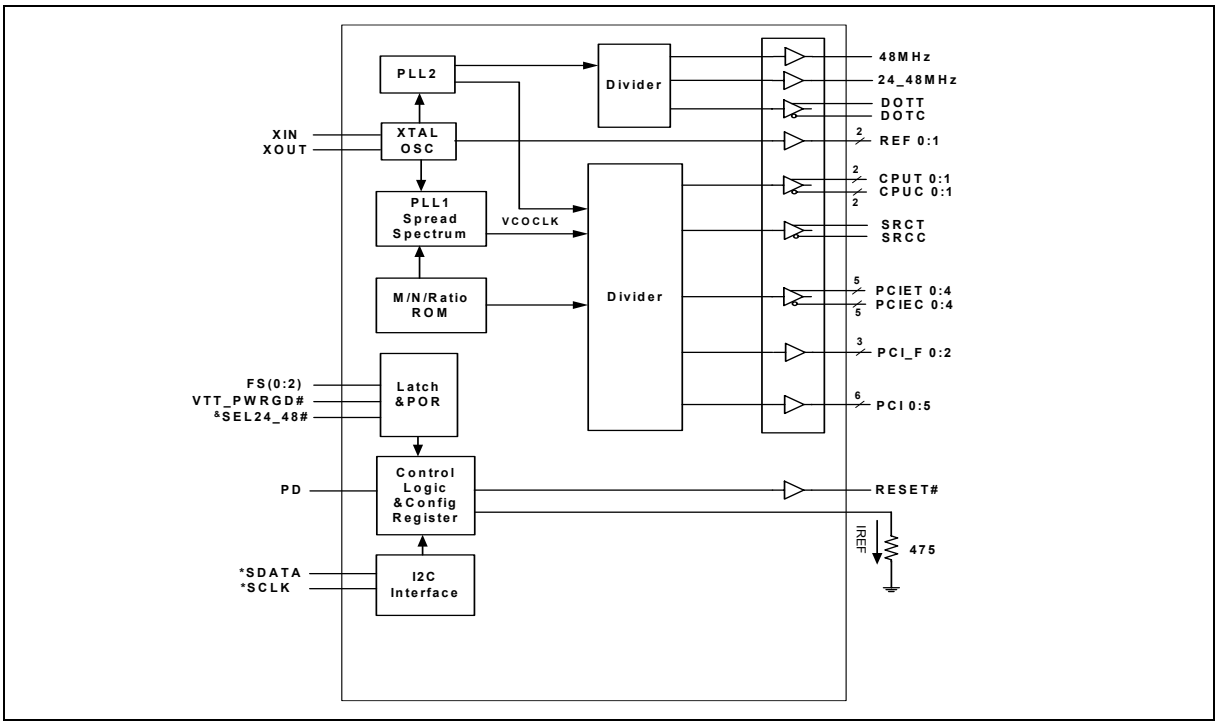
- 2 pair 0.7 V current mode Differential clock outputs for CPU
- 1 pair 0.7V current mode Differential 100 MHz clock outputs for SRC.
- 1 pair 0.7V current mode Differential 96MHz clock outputs for DOT.
- 5 pair 0.7V current mode Differential clock outputs for PCI-Express
- 6 PCI clock outputs for PCI
- 3 PCI clock free running outputs for PCI
- 1 24_48Mhz clock output for super I/O.
- 1 48 MHz clock output for USB.
- 2 14.318MHz REF clock outputs.
- Step-less frequency programming
- I^2C 2-Wire serial interface and support byte read/write and block read/write.
- -0.5% down type spread spectrum in H/W and software select mode
- Programmable spread spectrum scale to reduce EMI in M/N mode
- Programmable registers to enable/stop each output.
- Programmable clock outputs to control slew rate and skew.
- Watch Dog Timer and RESET# output pins
- 56 pin SSOP package

3. PIN CONFIGURATION



#: Active low
*: Internal pull up resistor 120K to VDD
&: Internal Pull-down resistor 120K to GND

4. BLOCK DIAGRAM



5. PIN DESCRIPTION

BUFFER TYPE SYMBOL	DESCRIPTION
IN	Input
IN_{tp120k}	Latched input at power up, internal 120kΩ pull up.
IN_{td120k}	Latched input at power up, internal 120kΩ pull down.
OUT	Output
OD	Open Drain
I/OD	Bi-directional Pin, Open Drain.
#	Active Low
*	Internal 120kΩ pull-up
&	Internal 120 kΩ pull-down

5.1 Crystal I/O

PIN	PIN NAME	TYPE	DESCRIPTION
48	XIN	IN	Crystal input with internal loading capacitors (18pF) and feedback resistors.
47	XOUT	OUT	Crystal output at 14.318MHz nominally with internal loading capacitors (18pF).

5.2 CPU and PCIE, PCI, Clock Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
43,42,40,39	CPUT [0:1] CPUC [0:1]	OUT	Low skew (< 125ps) 0.7V Current mode differential clock outputs for host frequencies of CPU
17,18,21,22,23,24,31,30,33,32	PCIET [0:4] PCIEC [0:4]	OUT	Low skew (<125ps) 0.7V Current mode differential clock outputs for PCI-Express
7	PCI_F0	OUT	3.3V free running PCI clock output.
8	PCI_F1	OUT	3.3V free running PCI clock output.
	&FS0	IN_{td120k}	Latched input for FS0 at initial power up for H/W selecting the output frequency. Latched voltage level refers to Vil_FS and Vih_FS voltage level. This is internal 120K pull down.
9	PCI_F2	OUT	3.3V free running PCI clock output.
	*FS1	IN_{tp120k}	Latched input for FS1 at initial power up for H/W selecting the output frequency. Latched voltage level refers to Vil_FS and Vih_FS voltage level. This is internal 120K pull up.
53,54,55,2,3,4	PCI [0:5]	OUT	Low skew (< 500ps) 3.3V PCI clock outputs

5.3 Fixed Frequency Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
51	REF0	OUT	3.3V REF 14.318Mhz clock output.
	&FS2	IN_{td120k}	Latched input for FS2 at initial power up for H/W selecting the output frequency, Latched voltage level refers to Vil_FS and Vih_FS voltage level. This is internal 120K pull down.
50	REF1	OUT	3.3V REF 14.318Mhz clock output.
11	24_48MHz	OUT	24MHz or 48MHz (default) clock output, In power on reset period, it is a hardware-latched pin, and it can be R/W by I2C control after power on reset period. Select by register 5 bit 7.
	&SEL24_48#	IN_{td120k}	Latched input for 24MHz or 48MHz select pin. This is internal 120K pull down default 48MHz. In power on reset period, it is a hardware-latched pin, and it can be R/W by I2C control after power on reset period. Select by register 5 bit 7.

Fixed Frequency Outputs, continued.

PIN	PIN NAME	TYPE	DESCRIPTION
12	48MHz	OUT	48MHz clock output for USB.
26,27	SRCT SRCC	OUT	0.7V current mode 100MHz differential clock outputs for S-ATA
14,15	DOTT/C	OUT	0.7V current mode 96MHz differential clock outputs for DOT

5.4 I²C Control Interface

PIN	PIN NAME	TYPE	DESCRIPTION
44	*SDATA	I/OD	Serial data of I²C 2-wire control interface with internal pull-up resistor.
45	*SCLK	IN	Serial clock of I²C 2-wire control interface with internal pull-up resistor.

5.5 Power Management Pins

PIN	PIN NAME	TYPE	DESCRIPTION
37	IREF	OUT	Deciding the reference current for the differential pairs. The pin was connected to the precision resistor tied to ground to decide the appropriate current; 475 ohm is the standard value.
52	RESET#	OD	System reset signal when the watchdog is time out. This pin will generate 250ms low phase when the watchdog timer is timeout.
16	VTT_PWRGD#	IN	Power good is a low active input signal used to determine when FS [2:0] are valid to be sample.
	PD	IN_{td120k}	Power Down Function. This is power down pin, high active (PD). Internal 120K pull down

5.6 Power Pins

PIN	PIN NAME	TYPE	DESCRIPTION
35	VDDA	PWR	3.3V power supply for PLL core.
6,56	VDDP	PWR	3.3V power supply for PCI.
19,34	VDDPE	PWR	3.3V power supply for PCI express pair.
28	VDDS	PWR	3.3V power supply for SRC pair.
10	VDD48	PWR	3.3V power supply for 48MHz.
41	VDDC	PWR	3.3V power supply for CPU.
46	VDDR	PWR	3.3V power supply for REF.
36	GNDA	PWR	Ground pin for PLL core.
1,5,13,20,25,29, 38,49	GND	PWR	Ground pin

6. FREQUENCY SELECTION BY HARDWARE OR SOFTWARE

This frequency table is used at power on latched FS [2:0] value or software programming at SSEL [4:0] (Register 0 bit 7 ~ 3).

FS4	FS3	FS2	FS1	FS0	CPU (MHZ)	PCIE (MHZ)	SRC (MHZ)	PCI (MHZ)
0	0	0	0	0	266.66	100.00	100.00	33.33
0	0	0	0	1	133.33	100.00	100.00	33.33
0	0	0	1	0	200.00	100.00	100.00	33.33
0	0	0	1	1	166.66	111.11	100.00	33.33
0	0	1	0	0	333.33	111.11	100.00	33.33
0	0	1	0	1	100.00	100.00	100.00	33.33
0	0	1	1	0	400.00	100.00	100.00	33.33
0	0	1	1	1	200.00	100.00	100.00	33.33
0	1	0	0	0	266.66	133.33	100.00	33.33
0	1	0	0	1	133.33	133.33	100.00	33.33
0	1	0	1	0	200.00	133.33	100.00	33.33
0	1	0	1	1	166.66	111.11	100.00	33.33
0	1	1	0	0	333.33	111.11	100.00	33.33
0	1	1	0	1	100.00	133.33	100.00	33.33
0	1	1	1	0	400.00	133.33	100.00	33.33
0	1	1	1	1	200.00	100.00	100.00	33.33
1	0	0	0	0	269.33	101.00	100.00	33.67
1	0	0	0	1	134.66	101.00	100.00	33.67
1	0	0	1	0	202.00	101.00	100.00	33.67
1	0	0	1	1	168.33	112.22	100.00	33.67
1	0	1	0	0	274.66	103.00	100.00	34.33
1	0	1	0	1	137.33	103.00	100.00	34.33
1	0	1	1	0	206.00	103.00	100.00	34.33
1	0	1	1	1	171.66	114.44	100.00	34.33
1	1	0	0	0	279.99	105.00	100.00	35.00
1	1	0	0	1	140.00	105.00	100.00	35.00
1	1	0	1	0	210.00	105.00	100.00	35.00
1	1	0	1	1	174.99	116.66	100.00	35.00
1	1	1	0	0	287.99	108.00	100.00	36.00
1	1	1	0	1	144.00	108.00	100.00	36.00
1	1	1	1	0	216.00	108.00	100.00	36.00
1	1	1	1	1	179.99	120.00	100.00	36.00

7. I²C CONTROL AND STATUS REGISTERS

7.1 Register 0: Frequency Select Register (Default = 10h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	SSEL [4]	0	Frequency selection by software via I²C	R/W
6	SSEL [3]	0		
5	SSEL [2]	0		
4	SSEL [1]	1		
3	SSEL [0]	0		
2	EN_SSEL	0	Enable software frequency table selection SSEL [4:0]. 0 = Select frequency by hardware. 1= Select frequency by software I²C - Bit 7~ 3.	R/W
1	SPSPEN	0	Enable Spread Spectrum 0 = Normal 1 = Spread Spectrum enabled	R/W
0	EN_SAFE_FREQ	0	Enable reload safe frequency when the watchdog is timeout. 0 = reload the FS [2:0] latched pins when watchdog time out. 1 = reload the safe frequency bit defined at Register 5 bit 4~0.	R/W

7.2 Register 1: CPU Clock Control (1 = Enable, 0 = Stopped) (Default: E2h)

BIT	PIN NO	PWD	DESCRIPTION	TYPE
7	Reserve	1	Reserved	R/W
6	40,39	1	CPUT1 / C1 output control	R/W
5	43,42	1	CPUT0 / C0 output control	R/W
4	Reserved	0	Reserved (Read only)	R
3	Reserved	0	Reserved (Read only)	R
2	-	X	Power on latched value of FS2 pin, Default: 0 (Read only).	R
1	-	X	Power on latched value of FS1 pin, Default: 1 (Read only).	R
0	-	X	Power on latched value of FS0 pin, Default: 0 (Read only).	R

7.3 Register 2: PCI Clock Control (1 = Enable, 0 = Stopped) (Default: FFh)

BIT	PIN NO	PWD	DESCRIPTION	TYPE
7	9	1	PCI_F2 output control	R/W
6	8	1	PCI_F1 output control	R/W
5	7	1	PCI_F0 output control	R/W
4	Reserved	1	Reserved	R/W
3	Reserved	1	Reserved	R/W
2	4	1	PCI5 output control	R/W
1	2,3	1	PCI3, PCI4 output control	R/W
0	Reserved	1	Reserved	R/W

7.4 Register 3: PCI Clock Control (1 = Enable, 0 = Stopped) (Default: FFh)

BIT	PIN NO	PWD	DESCRIPTION	TYPE
7	54,55	1	PCI1, PCI2 output control	R/W
6	Reserved	1	Reserved	R/W
5	53	1	PCI0 output control	R/W
4	Reserved	1	Reserved	R/W
3	Reserved	1	Reserved	R/W
2	Reserved	1	Reserved	R/W
1	Reserved	1	Reserved	R/W
0	Reserved	1	Reserved	R/W

7.5 Register 4: 24_48MHz, 48MHz, DOT, REF Control (1 = Enable, 0 = Stopped) (Default: FFh)

BIT	PIN NO	PWD	DESCRIPTION	TYPE
7	11	1	24_48MHz output control	R/W
6	14,15	1	DOT_T/C output control	R/W
5	12	1	48MHz output control	R/W
4	Reserved	1	Reserved	R/W
3	Reserved	1	Reserved	R/W
2	50,51	1	REF1, REF0 output control	R/W
1	Reserved	1	Reserved	R/W
0	Reserved	1	Reserved	R/W

7.6 Register 5: Watchdog Control (Default: 02h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	SEL24_48	X	24_ 48 MHz output selection, 1: 24 MHz, 0: 48 MHz (Default). Default value follow hardware trapping data on SEL24_48# pin.	R/W
6	EN_WD	0	Program this bit => 1: Enable Watchdog Timer feature. 0: Disable Watchdog Timer feature. Read-back this bit => During timer count down the bit read back to 1. If count to zero, this bit read back to 0.	R/W
5	WD_TIMEOUT	0	Read Back only. Timeout Flag. This bit is Read Only. 1: Watchdog has ever started and counts to zero. 0: Watchdog is restarted and counting.	R
4	SAF_FREQ [4]	0	These bits will be reloaded in Reg-0 to select frequency table. As the watchdog is timeout and EN_SAFE_FREQ=1.	R/W
3	SAF_FREQ [3]	0		
2	SAF_FREQ [2]	0		
1	SAF_FREQ [1]	1		
0	SAF_FREQ [0]	0		

7.7 Register 6: SRC, PCIE Control (1 = Enable, 0 = Stopped) (Default: FEh)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	26,27	1	SRCT/C output control	R/W
6	Reserved	1	Reserved	R/W
5	33,32	1	PCIET4/C4 output control	R/W
4	31,30	1	PCIET3/C3 output control	R/W
3	23,24	1	PCIET2/C2 output control	R/W
2	21,22	1	PCIET1/C1 output control	R/W
1	17,18	1	PCIET0/C0 output control	R/W
0	Reserved	0	Reserved	R/W

7.8 Register 7: Winbond Chip ID (Default: 22h) (Read Only)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	CHPI_ID [7]	0	Winbond Chip ID. W83195BR-118	R
6	CHPI_ID [6]	0	Winbond Chip ID.	R
5	CHPI_ID [5]	1	Winbond Chip ID.	R
4	CHPI_ID [4]	0	Winbond Chip ID.	R
3	CHPI_ID [3]	0	Winbond Chip ID.	R
2	CHPI_ID [2]	0	Winbond Chip ID.	R
1	CHPI_ID [1]	1	Winbond Chip ID.	R
0	CHPI_ID [0]	0	Winbond Chip ID.	R

7.9 Register 8: M/N Program (Default: 90h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	N_DIV [8]	1	Programmable N divisor value. Bit7~0 are defined in the Register 9	R/W
6	N_DIV [9]	0	Programmable N divisor value. Bit7~0 are defined in the Register 9	R/W
5	M_DIV [5]	0	Programmable M divisor value.	R/W
4	M_DIV [4]	1		R/W
3	M_DIV [3]	0		R/W
2	M_DIV [2]	0		R/W
1	M_DIV [1]	0		R/W
0	M_DIV [0]	0		R/W

7.10 Register 9: M/N Program Register (Default: BBh)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	N_DIV [7]	1	Programmable N divisor value bit 7 ~0. The bit 8 is defined in Register 8.	R/W
6	N_DIV [6]	0		R/W
5	N_DIV [5]	1		R/W
4	N_DIV [4]	1		R/W
3	N_DIV [3]	1		R/W
2	N_DIV [2]	0		R/W
1	N_DIV [1]	1		R/W
0	N_DIV [0]	1		R/W

7.11 Register 10: Reserved (Default: 3Bh)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	SRC_SPSPEN	0	Enable SRC spread spectrum feature 1: Enable 0: Disable	R/W
6	Reserved	0	Reserved	R/W
5	Reserved	1	Reserved	R/W
4	Reserved	1	Reserved	R/W
3	Reserved	1	Reserved	R/W
2	Reserved	0	Reserved	R/W
1	Reserved	1	Reserved	R/W
0	Reserved	1	Reserved	R/W

7.12 Register 11: Spread Spectrum Programming (Default: 0Eh)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	SP_UP [3]	0	Spread Spectrum Up Counter bit 3 ~ bit 0.	R/W
6	SP_UP [2]	0		R/W
5	SP_UP [1]	0		R/W
4	SP_UP [0]	0		R/W
3	SP_DOWN [3]	1	Spread Spectrum Down Counter bit 3 ~ bit 0	R/W
2	SP_DOWN [2]	1	2's complement representation.	R/W
1	SP_DOWN [1]	1	Ex: 1 -> 1111; 2 -> 1110; 7 -> 1001; 8 -> 1000	R/W
0	SP_DOWN [0]	0		R/W

7.13 Register 12: Divisor Control (Default: 08h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	Reserved	0	Reserved	R/W
6	KVAL6	X	Define the PCI divider ratio Table-2 integrate the all divider configuration	R/W
5	KVAL5	X		R/W
4	KVAL4	X	Define the PCIE divider ratio Refer to Table-2	R/W
3	KVAL3	X		R/W
2	KVAL2	X	Define the CPU divider ratio Refer to Table-2	R/W
1	KVAL1	X		R/W
0	KVAL0	X		R/W

Table-2 CPU, PCIE, PCI divider ratio selection Table

LSB / MSB		PCI		PCIE		CPU			
		Bit5		Bit3		Bit1, 0			
		0	1	0	1	00	01	10	11
Bit2/ Bit4/ Bit6	0	Div12	Div16	Div3	Div4	Div2	Div3	Div4	Div6
	1	Div20	Div24	Div8	Div6	Div8	Div8	Div8	Div8

7.14 Register 13: Step-less Enable Control (Default: 0Ah)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	EN_MN_PROG	0	0: Output frequency depend on frequency table 1: Program all clock frequency by changing M/N value The equation is **VCO =14.318MHz*(N+4)/ M**. Once the watchdog timer timeout, the bit will be clear. Then the frequency will be decided by hardware default FS<2:0> or desired frequency select SAF_FREQ [4:0] depend on EN_SAFE_FREQ (Reg0 - bit 0).	R/W
6	N<10>	0	Programmable N divisor bit 10.	R/W
5	Reserved	0	Reserved	R/W
4	Reserved	0	Reserved	R/W
3	IVAL<3>	1	Charge pump current selection	R/W
2	IVAL<2>	0		R/W
1	IVAL<1>	1		R/W
0	IVAL<0>	0		R/W

7.15 Register 14: Control (Default: 10h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	DRI_CONT	0	CPUT / SRCT / PCIE_T / DOT_T output state in during POWER DOWN assertion. 1: Driven (2*Iref), 0: Tristate (Floating) CPUT / SRCT / PCIE_T / DOT_T output state in during STOP Mode assertion. 1: Driven (6*Iref), 0: Tristate (Floating) Complementary parts always tri-state (floating) in power down or stop mode.	R/W
6	Reserved	0	Reserved	R/W
5	SPCNT [5]	0	Spread Spectrum Programmable time, the resolution is 280ns. Default period is 11.8us	R/W
4	SPCNT [4]	1		R/W
3	SPCNT [3]	0		R/W
2	SPCNT [2]	0		R/W
1	SPCNT [1]	0		R/W
0	SPCNT [0]	0		R/W

7.16 Register 15: SST Control (Default: ECh)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	INV_CPU	1	Invert the CPU phase, 1: Default, 0: Inverse	R/W
6	Reserved	1	Reserved	R/W
5	SPSP_TYPE	1	Spread spectrum implementation method 1 : Pendulum type 0 : Original	R/W
4	Reserved	0	Reserved	R/W
3	Reserved	1	Reserved	R/W
2	Reserved	1	Reserved	R/W
1	Reserved	0	Reserved	R/W
0	Reserved	0	Reserved	R/W

7.17 Register 16: Skew Control (Default: E4h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	INV_PCIE	1	Invert the PCIE phase, 1: Default, 0: Inverse	R/W
6	INV_PCI	1	Invert the PCI phase, 1: Default, 0: Inverse	R/W
5	CSKEW [2]	1	CPU1 to CPU0 skew control, Skew resolution is 300ps	R/W
4	CSKEW [1]	0	The decision of skew direction is same as CSKEW<2:0> setting	R/W
3	CSKEW [0]	0		R/W
2	PSKEW [2]	1	CPU1 to PCI skew control, Skew resolution is 300ps	R/W
1	PSKEW [1]	0	The decision of skew direction is same as PSKEW [2:0] setting	R/W
0	PSKEW [0]	0		R/W

7.18 Register 17: Slew rate Control (Default: 00h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	Reserved	X	Reserved	R/W
6	INV_48MHz	0	Invert the 48MHz phase, 0: In phase with 24_48MHz 1: 180 degrees out of phase	R/W
5	PCI_F0_S2	0	PCI_F0 slew rate control	R/W
4	PCI_F0_S1	0	11 : Strong , 00 : Weak , 10/01 : Normal	R/W
3	Reserved	0	Reserved	R/W
2	Reserved	0	Reserved	R/W
1	Reserved	0	Reserved	R/W
0	Reserved	0	Reserved	R/W

7.19 Register 18: Reserved (Default: 00h)

7.20 Register 19: Skew Control (Default: DAh)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	Reserved	1	Reserved	R/W
6	Reserved	1	Reserved	R/W
5	PCIESKEW<2>	0	CPU1 to PCIE skew control	R/W
4	PCIESKEW<1>	1	Skew resolution is 300ps	R/W
3	PCIESKEW<0>	1	The decision of skew direction is same as PCIESKEW<2:0> setting	R/W
2	Reserved	0	Reserved	R/W
1	Reserved	1	Reserved	R/W
0	Reserved	0	Reserved	R/W

7.21 Register 20: Watch dog timer (Default: 88h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	Reserved	1	Reserved	R/W
6	WD_TIME [6]	0	Setting the down count depth (Failure decision). One bit resolution represents 250ms. Default time depth is 8*250ms = 2.0 second. If the watchdog timer is counting, this register will return present down count value.	R/W
5	WD_TIME [5]	0		R/W
4	WD_TIME [4]	0		R/W
3	WD_TIME [3]	1		R/W
2	WD_TIME [2]	0		R/W
1	WD_TIME [1]	0		R/W
0	WD_TIME [0]	0		R/W

7.22 Register 21: Asynchronous Control (Default: 4Bh)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	Tri-state	0	Tri-state all output if set 1	R/W
6	Reserved	1	Reserved	R/W
5	Reserved	0	Reserved	R/W
4	Reserved	0	Reserved	R/W
3	Reserved	1	Reserved	R/W
2	SRC_BASE3	0	1: Asynchronous PCIE / PCI always at 100MHz / 33MHz 0: PCIE / PCI frequency are follow Bit1, 0 setting	R/W
1	FIX_ADDR<1>	1	Asynchronous PCIE / PCI frequency table selection FIX_ADDR<1:0> =>	R/W
0	FIX_ADDR<0>	1	00: 96 / 36MHz 01 : 96 / 32MHz 10: 128 / 38.4MHz 11 : Output from PLL1	R/W

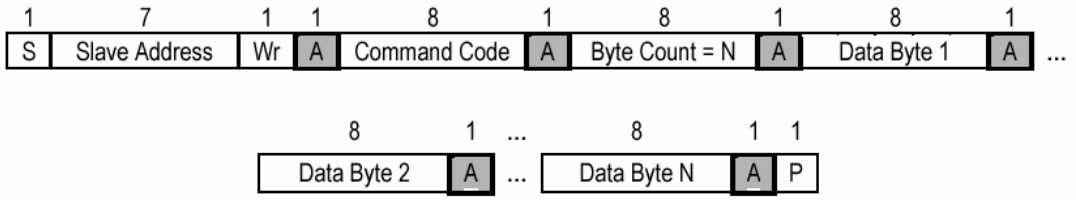
8. ACCESS INTERFACE

The W83195BR-118 provides I^{2}C Serial Bus for microprocessor to read/write internal registers. In the W83195BR-118 is provided Block Read/Block Write and Byte-Data Read/Write protocol. The I^{2}C address is defined at 0xD2.
The register number is increased by one if using byte data read/write protocol.

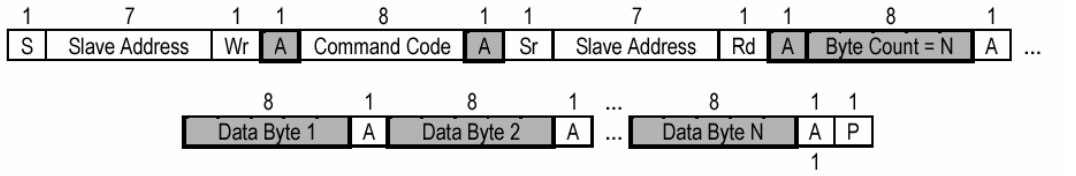
Example: In block mode, byte number of program register is 1
In byte mode, byte number of program register is 2 (Byte number of block mode +1)

Block Read and Block Write Protocol

8.1 Block Write protocol

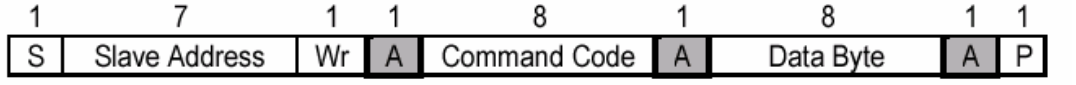


8.2 Block Read protocol

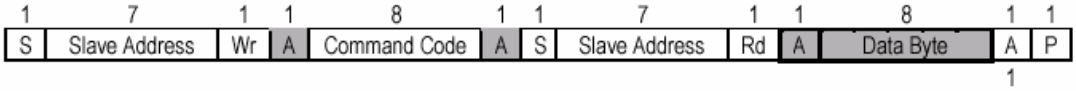


In block mode, the command code must filled 8'h00

8.3 Byte Write protocol



8.4 Byte Read protocol



9. SPECIFICATIONS

9.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or VDD).

PARAMETER	RATING
Absolute 3.3V Core Supply Voltage	-0.5V to +4.6V
Absolute 3.3V I/O Supple Voltage	- 0.5V to + 4.6V
Operating 3.3V Core Supply Voltage	3.135V to 3.465V
Operating 3.3V I/O Supple Voltage	3.135V to 3.465V
Storage Temperature	- 65°C to + 150°C
Ambient Temperature	- 55°C to + 125°C
Operating Temperature	0°C to + 70°C
Input ESD protection (Human body model)	2000V

9.2 General Operating Characteristics

VDD= 3.3V ± 5 %, TA = 0℃ to +70℃,					
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Input Low Voltage	V_{IL}		0.8	V_{dc}	
Input High Voltage	V_{IH}	2.0		V_{dc}	
Output Low Voltage	V_{OL}		0.4	V_{dc}	
Output High Voltage	V_{OH}	2.4		V_{dc}	
Operating Supply Current	I_{dd}		350	mA	CPU = 100 to 400 MHz PCI = 33.3 Mhz with load 10pF
Input pin capacitance	Cin		5	pF	
Output pin capacitance	Cout		6	pF	
Input pin inductance	Lin		7	nH	

9.3 Skew Group timing clock

VDD = 3.3V ± 5 %, TA = 0℃ to +70℃, Cl=10pF				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
CPU pair to CPU pair Skew		125	ps	Measure Crossing point
PCIE pair to PCIE pair Skew		125	ps	Measure Crossing point
PCI to PCI Skew		500	ps	Measured at 1.5V
48MHz to 48MHz Skew		1000	ps	Measured at 1.5V

9.4 CPU 0.7V Electrical Characteristics

*VDDC= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load Rs=33, Rp=49.9 Cl=2pF, Vol=0.175V, Voh=0.525V, Vr=475, IREF=2.32mA, Ioh=6*IREF*				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	175	700	ps	Measure Single Ended waveform
Fall Time	175	700	ps	Measure Single Ended waveform
Absolute crossing point Voltages	250	550	mV	Measure Single Ended waveform
Voltage High	660	850	mV	Measure Single Ended waveform
Voltage Low	-150		mV	Measure Single Ended waveform
Cycle to Cycle jitter		100	ps	Measure Differential waveform
Duty Cycle	45	55	%	Measure Differential waveform

9.5 SRC 0.7V Electrical Characteristics

*VDDS= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load Rs=33, Rp=49.9 Cl=2pF, Vol=0.175V, Voh=0.525V, Vr=475, IREF=2.32mA, Ioh=6*IREF*				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	175	700	ps	Measure Single Ended waveform
Fall Time	175	700	ps	Measure Single Ended waveform
Absolute crossing point Voltages	250	550	mV	Measure Single Ended waveform
Voltage High	660	850	mV	Measure Single Ended waveform
Voltage Low	-150		mV	Measure Single Ended waveform
Cycle to Cycle jitter		100	ps	Measure Differential waveform
Duty Cycle	45	55	%	Measure Differential waveform

9.6 PCIE 0.7V Electrical Characteristics

*VDDPE= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load Rs=33, Rp=49.9 Cl=2pF, Vol=0.175V, Voh=0.525V, Vr=475, IREF=2.32mA, Ioh=6*IREF*				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	175	700	ps	Measure Single Ended waveform
Fall Time	175	700	ps	Measure Single Ended waveform
Absolute crossing point Voltages	250	550	mV	Measure Single Ended waveform
Voltage High	660	850	mV	Measure Single Ended waveform
Voltage Low	-150		mV	Measure Single Ended waveform
Cycle to Cycle jitter		100	ps	Measure Differential waveform
Duty Cycle	45	55	%	Measure Differential waveform

9.7 PCI Electrical Characteristics

VDDP= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	500	2000	ps	Vol=0.4V, Voh=2.4V
Fall Time	500	2000	ps	Voh=2.4V, Vol=0.4V
Cycle to Cycle jitter		250	ps	Measured at 1.5V
Duty Cycle	45	55	%	Measured at 1.5V
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

9.8 24M, 48M Electrical Characteristics

VDD48= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	500	2000	ps	Vol=0.4V, Voh=2.4V
Fall Time	500	2000	ps	Voh=2.4V, Vol=0.4V
Long term jitter		500	ps	Measured at 1.5V
Duty Cycle	45	55	%	Measured at 1.5V
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

9.9 REF Electrical Characteristics

VDD= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	500	2000	ps	Vol=0.4V, Voh=2.4V
Fall Time	500	2000	ps	Voh=2.4V, Vol=0.4V
Cycle to Cycle jitter		1000	ps	Measured at 1.5V
Duty Cycle	45	55	%	Measured at 1.5V
Pull-Up Current Min	-29		mA	Vout=1.0V
Pull-Up Current Max		-23	mA	Vout=3.135V
Pull-Down Current Min	29		mA	Vout=1.95V
Pull-Down Current Max		27	mA	Vout=0.4V

9.10 DOT 0.7V Electrical Characteristics

*VDD= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load Rs=33, Rp=49.9 Cl=2pF, Vol=0.175V, Voh=0.525V, Vr=475, IREF=2.32mA, Ioh=6*IREF*				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	175	700	ps	Measure Single Ended waveform
Fall Time	175	700	ps	Measure Single Ended waveform
Absolute crossing point Voltages	250	550	mV	Measure Single Ended waveform
Voltage High	660	850	mV	Measure Single Ended waveform
Voltage Low	-150		mV	Measure Single Ended waveform
Cycle to Cycle jitter		250	ps	Measure Differential waveform
Duty Cycle	45	55	%	Measure Differential waveform