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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





Winbond
Bus Termination Regulator
W83310DS-A/W83310DG-A

W83310DS-A/W83310DG-A



W83310DS-A/W83310DG-A

Datasheet Revision History

| | PAGES | DATES | VERSION | VERSION ON WEB | MAIN CONTENTS |
|---|-------|-----------|---------|----------------|----------------|
| 1 | | 1/17/2006 | 0.5 | N.A. | First released |
| 2 | | | | | |
| 3 | | | | | |
| 4 | | | | | |
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LIFE SUPPORT APPLICATIONS

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W83310DS-A/W83310DG-A



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W83310DS-A/W83310DG-A



1. GENERAL DESCRIPTION

The W83310DS-A/W83310DG-A is a linear regulator provides a power achieves continuous 2.0Amp bi-directional sinking and driving capability for a high speed bus terminator application. The chip simply implements a stable power supply which tracks half of input power dynamically for bus terminator with a single chip. The W83310DS-A/W83310DG-A is promoted with small footprint 8-SOP 150mil power package. With W83310DS-A/W83310DG-A design, a high integration, high performance, and cost-effective solution are promoted.

2. FEATURES

- Regulates a bi-directional power with driving and sinking capability
- Provides achieve continuous 2.0Amp driving and sinking current
- Power MOSFET integrated
- Low external component count
- Low output voltage offset
- VCNTL Operates with +3.3V & 2.5 V power
- 8-SOP 90mil small power package
- Low cost and easy to use

3. APPLICATIONS

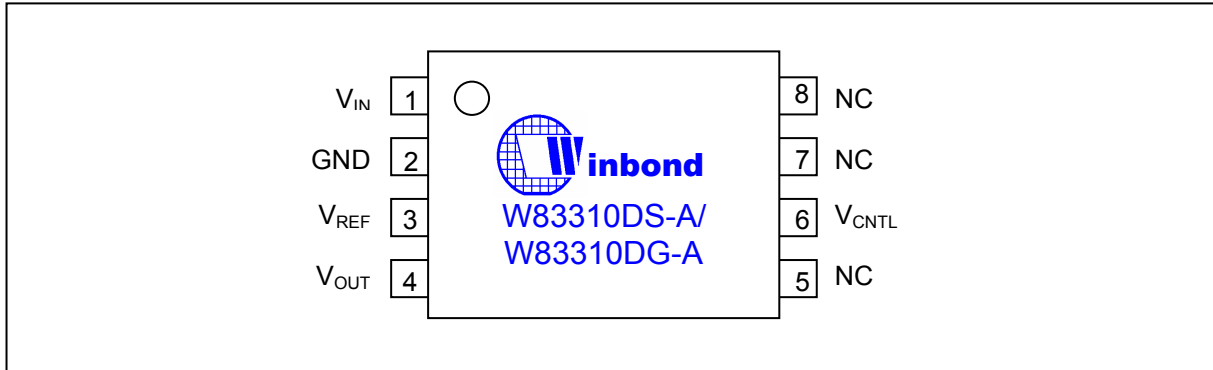
- DDR/DDRII Bus Termination Regulator
- Active Termination Bus
- Intel® Springdale GMCH- V_{TT} Support
- SSTL-2
- SSTL-3

W83310DS-A/W83310DG-A



4. PIN CONFIGURATION AND DESCRIPTION

- W83310DS-A/W83310DG-A



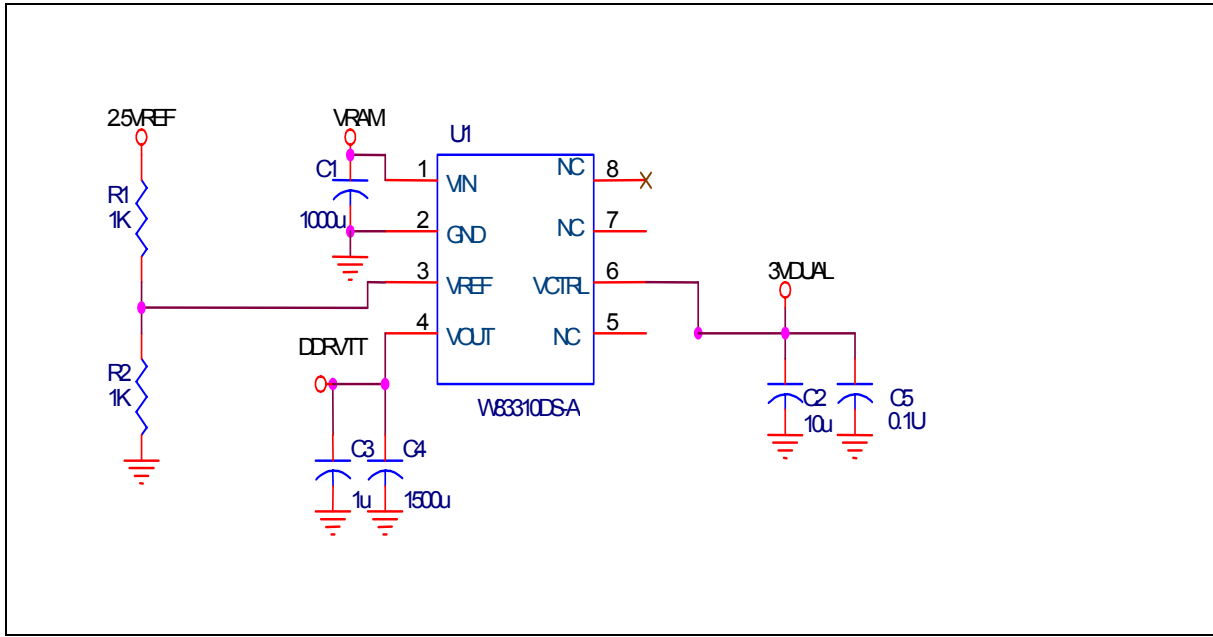
| SYMBOL | PIN | FUNCTION |
|------------|-----|---|
| V_{IN} | 1 | Main power input pin. |
| GND | 2 | Power ground. |
| V_{REF} | 3 | Internal reference voltage source. Reference voltage on the pin will be referred with the value of pin |
| V_{OUT} | 4 | Voltage output pin. |
| NC | 5 | |
| V_{CNTL} | 6 | Power for internal control logic use |
| NC | 7 | |
| NC | 8 | |

W83310DS-A/W83310DG-A



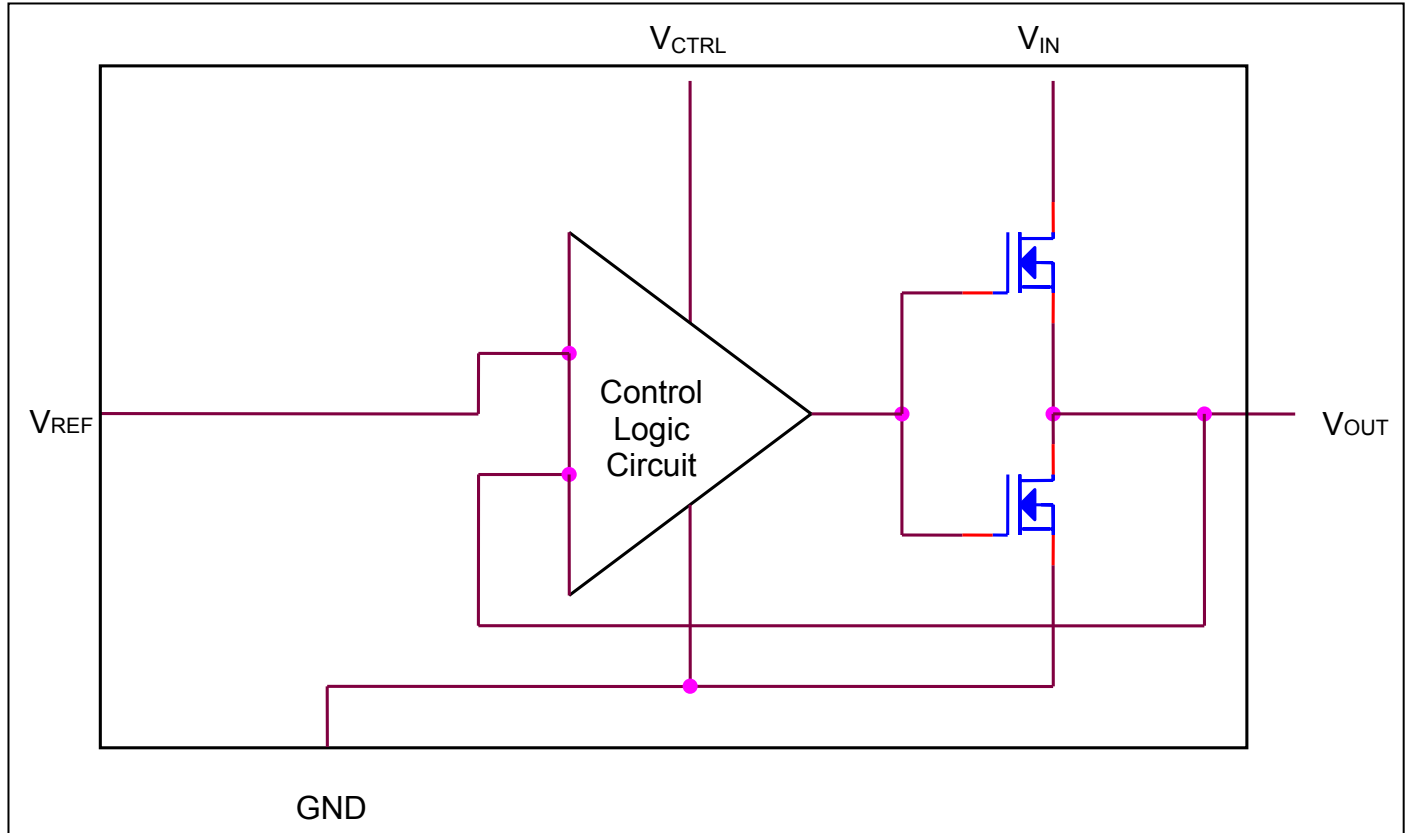
5. APPLICATION CIRCUIT

- W83310DS-A/W83310DG-A for DDR SDRAM Application





6. INTERNAL BLOCK DIAGRAM



W83310DS-A/W83310DG-A



7. ELECTRICAL CHARACTERISTICS

7.1 AC CHARACTERISTICS

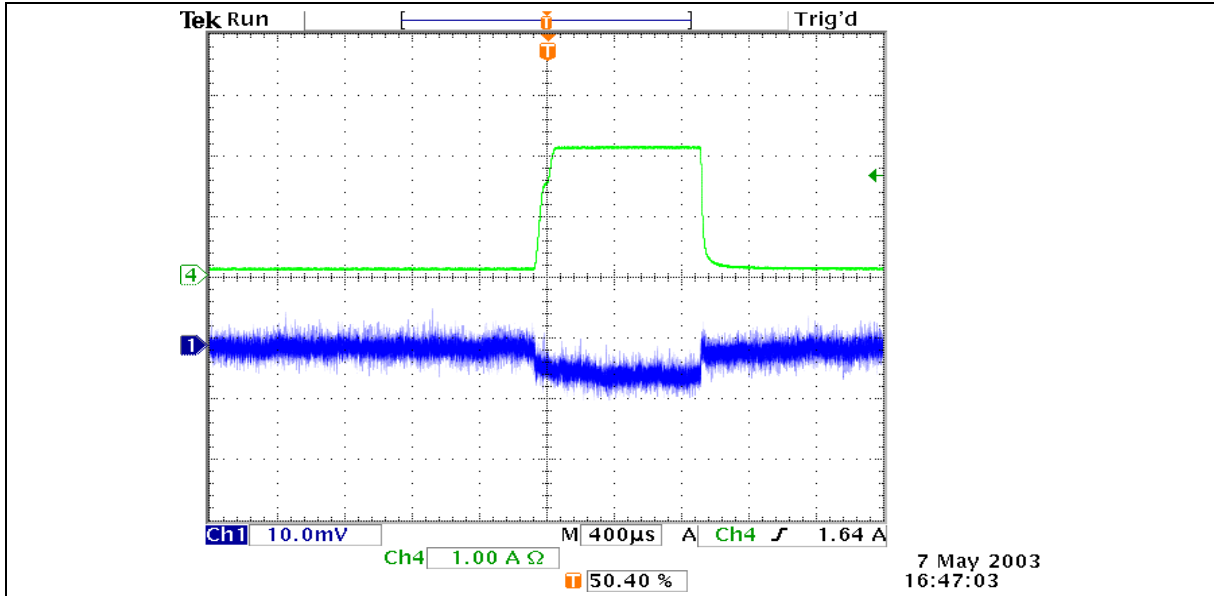
| <i>C_{out}</i> =1000uF, <i>T_A</i> = 0 °C to +70 °C | | | | | | |
|---|-------------------|------|-----|------|-------|-------------------------------|
| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | TEST CONDITIONS |
| Output Offset Voltage | V _{os} | -5 | 0 | +5 | mV | I _{out} =0A |
| Load Regulation | | | 0.8 | | % | Loading: 0A→2.0A |
| | | | 0.8 | | | Loading: 0A→-2.0A |
| Input Voltage Range | V _{IN} | 1.62 | | 3.63 | V | |
| | V _{CNTL} | | 3.3 | 3.63 | | |
| Operating Current of V _{CNTL} | I _{CNTL} | | 0.5 | 1 | mA | No Load(I _{out} =0A) |
| Short Current Limit | I _{LMT} | | 4.0 | | A | |

Note: Load regulation is tested by using a 1ms current pulse and V_{OUT} measuring.

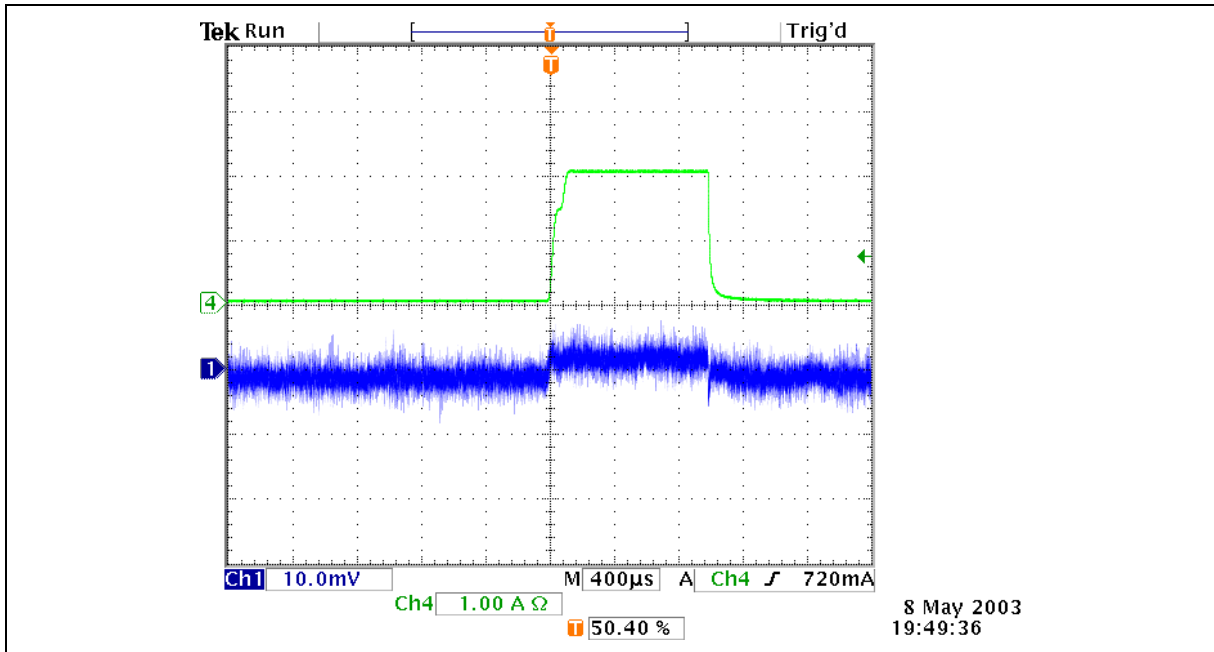


8. TYPICAL OPERATING WAVEFORM

Load regulation with test condition - $V_{CTRL}=3.3V$; $V_{IN}=2.5V$; $V_{OUT}=1.225V$; 2.0Amp pulse driving current.



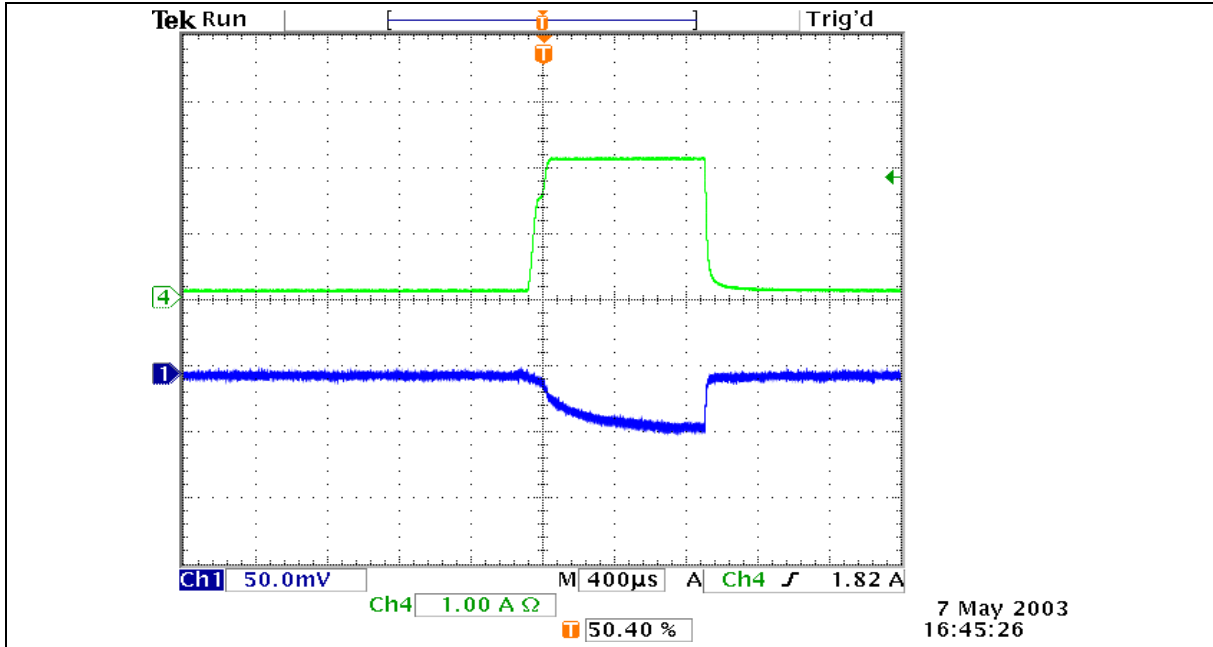
Load regulation with test condition - $V_{CTRL}=3.3V$; $V_{IN}=2.5V$; $V_{OUT}=1.225V$; 2.0Amp pulse sinking current.



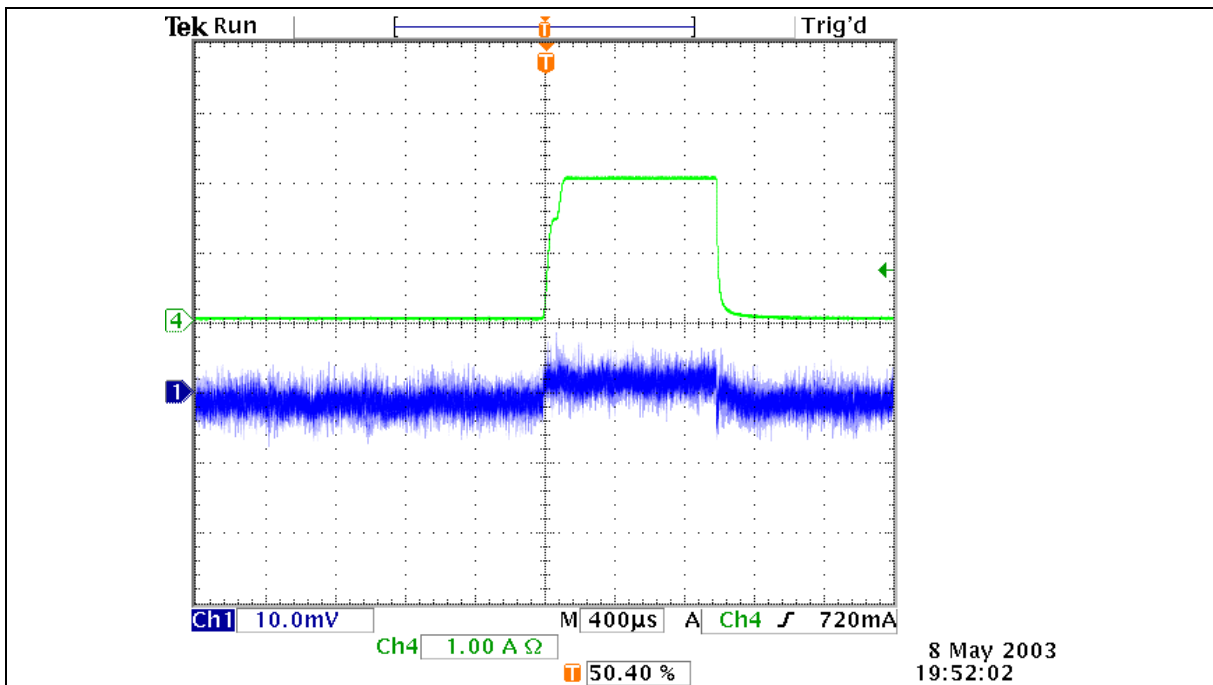
W83310DS-A/W83310DG-A



Load regulation with test condition - $V_{CTRL}=3.3V$; $V_{IN}=2.5V$; $V_{OUT}=1.45V$; 2.0Amp pulse driving current.



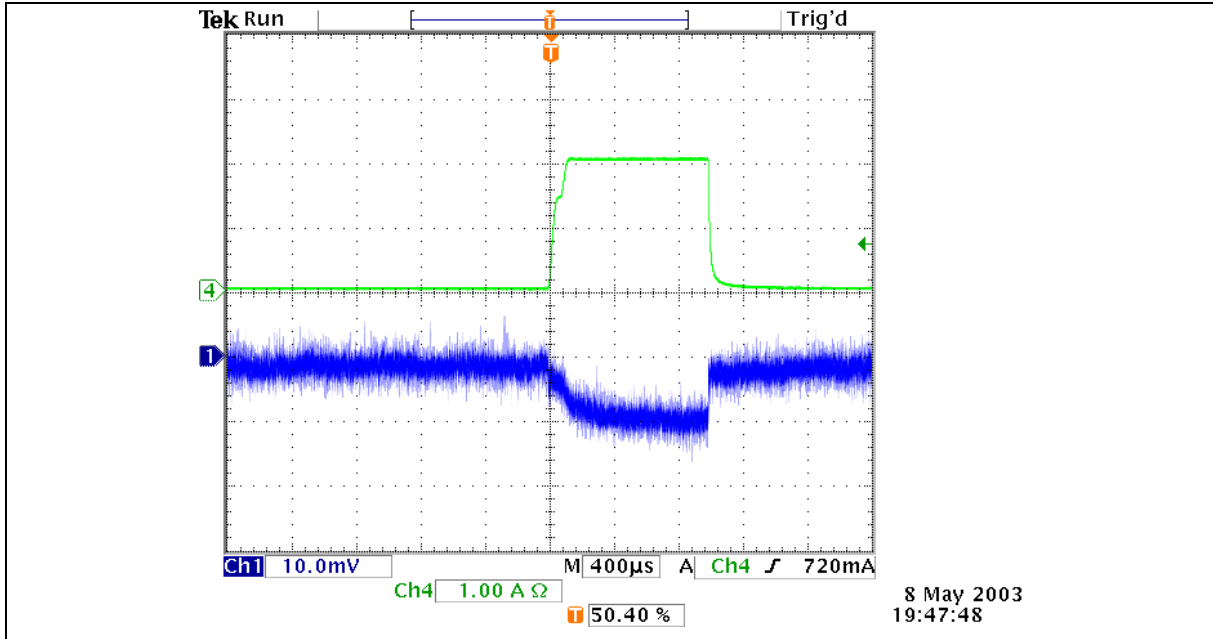
Load regulation with test condition - $V_{CTRL}=3.3V$; $V_{IN}=2.5V$; $V_{OUT}=1.45V$; 2.0Amp pulse sinking current.



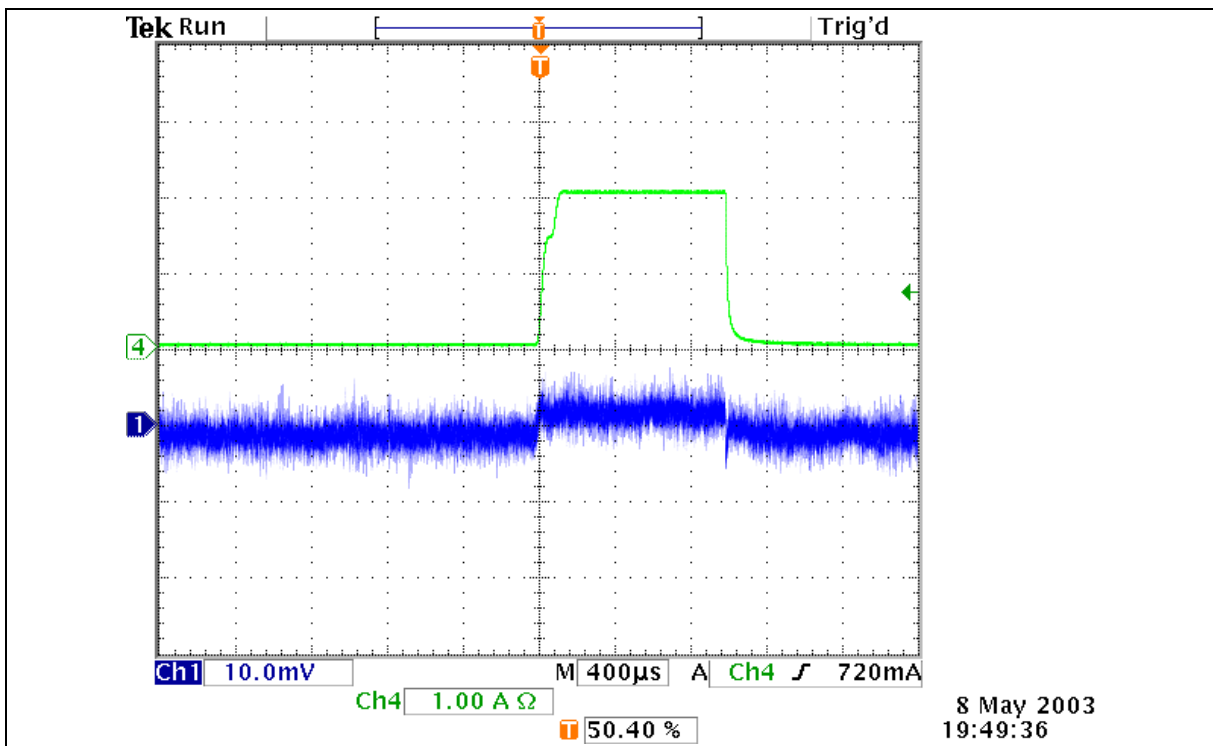
W83310DS-A/W83310DG-A



Load regulation with test condition - $V_{CTRL}=3.3V$; $V_{IN}=2.5V$; $V_{OUT}=1.25V$; 2.0Amp pulse driving current.



Load regulation with test condition - $V_{CTRL}=3.3V$; $V_{IN}=2.5V$; $V_{OUT}=1.25V$; 2.0Amp pulse sinking current.

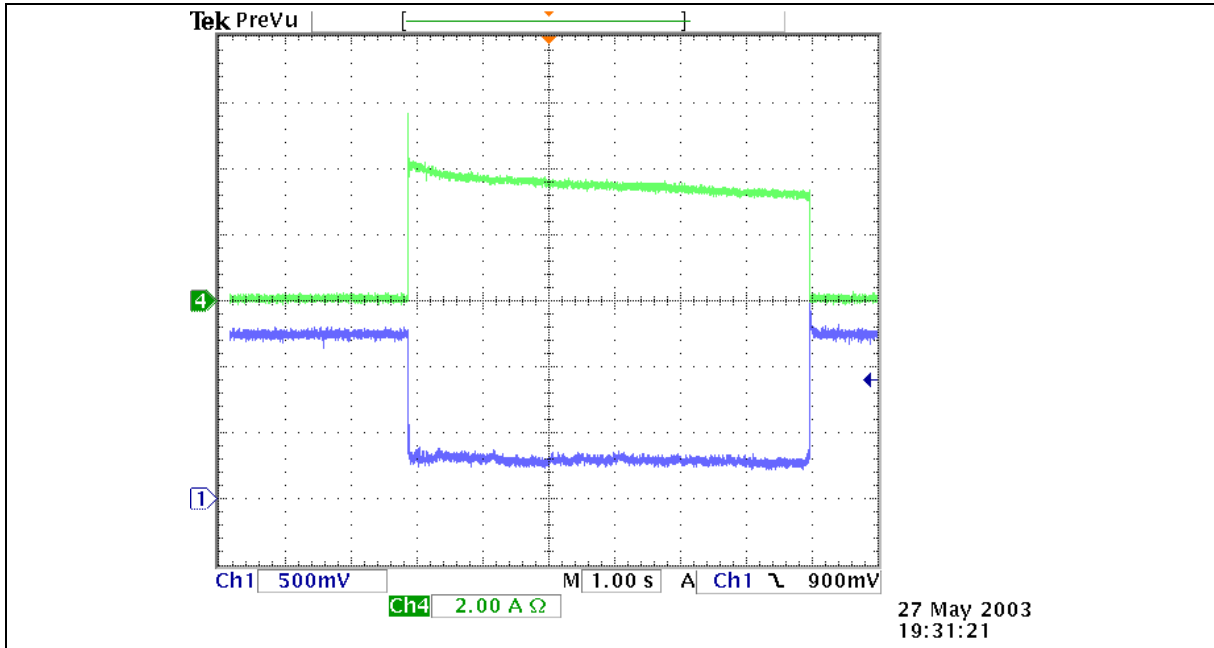


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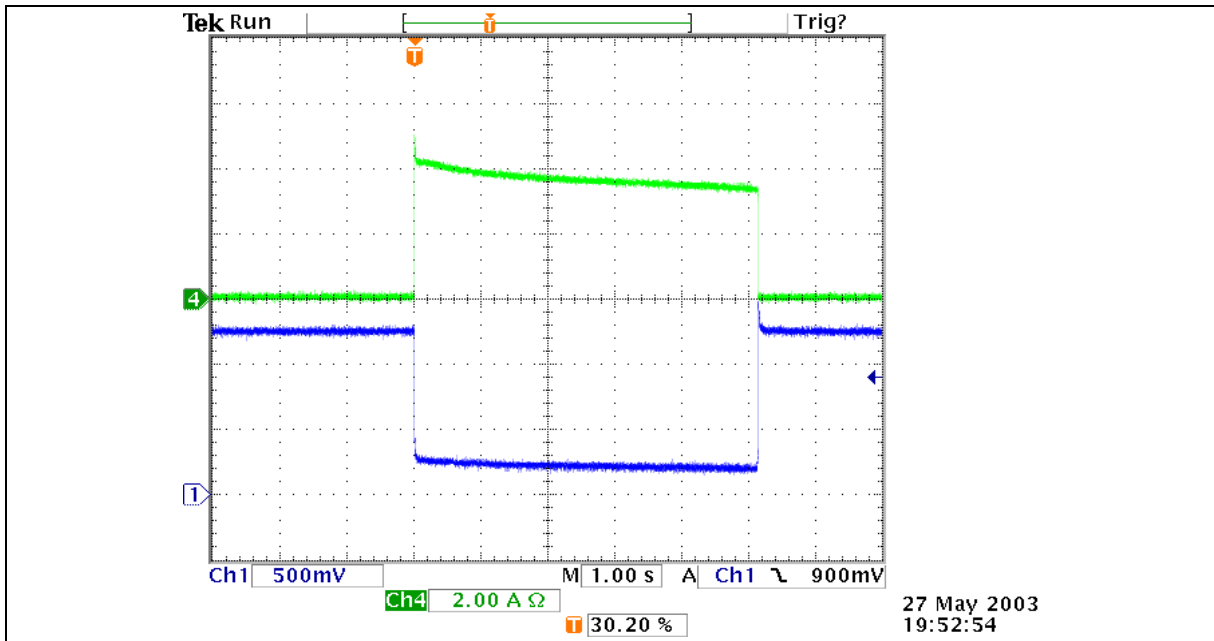


Short Current Limit

- $V_{CTRL} = 3.3V$



- $V_{CTRL} = 3.6V$

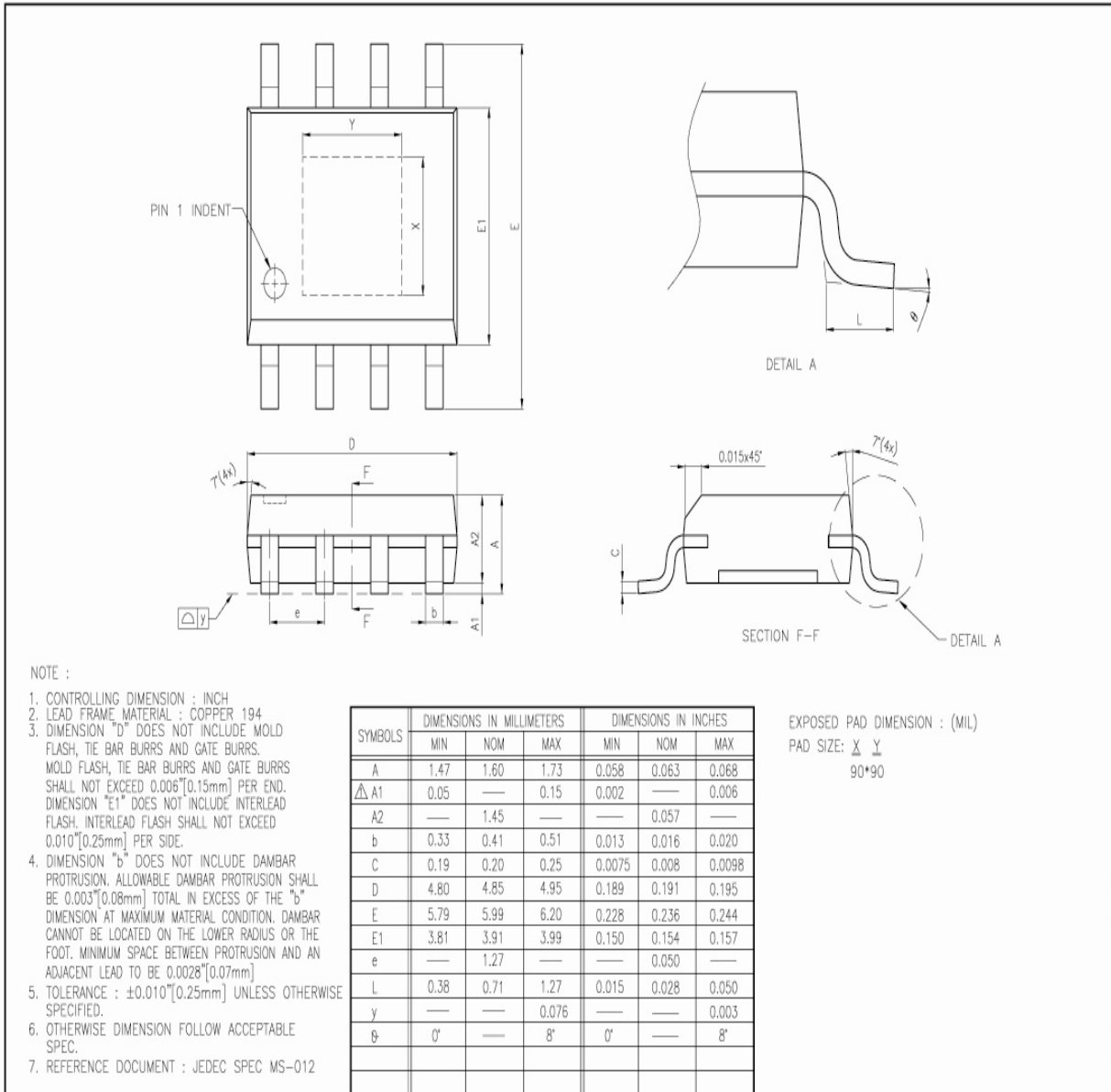


W83310DS-A/W83310DG-A



9. PACKAGE DIMENSION

8L Power SOP 150mil



W83310DS-A/W83310DG-A



10. THERMAL PERFORMANCE

| TEST ON FOUR-LAYER (2S2P) JEDEC TEST BOARD | | | | | | | |
|--|-----------|----------------------|-----|---------|------|---------|--------------|
| PACKAGE | POWER (W) | COMPONENT TEMP. (°C) | | | | | Θ JC (°C /W) |
| | | PACKAGE | DIE | DOWNSET | LEAD | AMBIENT | |
| PSOP-8 | 3.05 | 100 | 145 | 79 | 78 | 25 | 14.7 |

An area of 190mil*150mil on the top layer is use as a thermal pad for W83310DS and this is connected to the bottom layer by vias. The Θja of the W83310DS mounted on this demo board is about 39 °C /W. Assuming the TA=25 °C and TJ=160 °C, the maximum power dissipation is calculated as: PD(max)=(160-25)/39=3.46W

11. ORDERING INFORMATION

| PART NUMBER | PACKAGE TYPE | PRODUCTION FLOW |
|-------------|--------------|-----------------|
| W83310DS-A | Power SOP-8 | |
| W83310DG-A | Power SOP-8 | |

12. HOW TO READ THE TOP MARKING



Left line: Winbond logo

1st & 2nd line: W83310DS-A/W83310DG-A – the part number

3rd line: Tracking code 318 G A

318: packages assembled in Year 03', week 18

G: assembly house ID; O means OSE, G means GR, etc.

A: the IC version

W83310DS-A/W83310DG-A



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