Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

W83627DHG

WINBOND LPC I/O

Note: This document is for UBC, UBE and UBF version except specified descriptions

Date : April 10, 2007 Version : 1.4

Data Sheet Revision History

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
1	N.A.	12/15/2005	0.1	N.A.	1. First published version.
2	N.A.	02/22/2006	0.2	N.A.	1. Add descriptions of the registers, functions,, AC/DC timing, and top marking
3	N.A.	03/15/2006	0.3	N.A.	1. Revise Table 8.1 and the timing chart of section 10.3.1 2. Add registers for AMDSI at LDB, CRF5h,CRF6h and F7h(Bank1) 3. Swap LDB, CRF2h bit 0 and bit 1. 4. Modify the default values for LDA, CRFEh 5. Modify the descriptions of LD9, CR30h bit 0 and CRF7h bit 4. 6. Remove LDA, CRE9h bit4 ~ 3 7. Swap LDC, CRE0h bit3~0 and CRE5h bit7~4
4	N.A.	05/05/2006	0.4	N.A.	1. Add FDC, UART, Parallel Port and KBC interface descriptions 2. Remove all the descriptions about AMDSI 3. Modify the diagrams and descriptions for Current Mode 4. Add two control bits for the selections of SYSFANOUT and CPUFANOUT0 output type at CR[24h] 5. Remove the description of the internal pulled-up resistor of Parallel Port 6. Modify the definitions of edge/level and enable/disable debounce circuit of GP30, GP31 and GP35 7. Modify the descriptions of LD7, CRF7h and LD9, CRE6h ~ CRE9h 8. Correct typos and grammatical mistakes
5	N.A	05/15/2006	0.41	N.A	1. Remove the remaining descriptions about AMDSI in datasheet ver.0.4
6	N.A.	05/19/2006	0.42	N.A	1. Add a note for Index# of FDC Interface and pin 83(GP42) of Serial Port & Infrared Port Interface in Pin Description 2. Reserve the bit 7 of LD0, CRF0h 3. Modify the descriptions of TRAK0#, WP#, RDATA# and DSKCHG# of FDC Interface 4. Modify the descriptions for strapping pins: HEFRAS, PENROM, PENKBC and EN_GTL 5. Modify the DC spec.
7	N.A.	06/23/2006	0.5	N.A.	1. Remove the note and renew the descriptions for Index# of FDC Interface. 2. Correct the descriptions of HM Device Bank 0, CR[12h] bit0. 3. Add two control bits for AUXFANOUT and CPUFAOUT1 output type selection. 4. Add a new bit at LDC, CR[E8h] bit 1 for more PECI

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
					clock selection. 5. Modify the default values of HM Device Bank 0, CR[43h] bit 5,0 and CR[46h] bit 2~1.
8	N.A.	09/29/2006	0.6	N.A.	1. Add new chapters for Serial Peripheral Interface, Configuration Register Access Protocol, Power Management, Serialized IRQ, Watchdog Timer VID Inputs and Outputs, and PCI Reset Buffers. 2. Update the feature lists of the W83627DHG in Chapter 2 Features. 3. Add descriptions of PECI and SST and a table of SMBus in Chapter 5 Pin Description. 4. Add new sections of Caseopen and Beep Alarm Function in Chapter 7 Hardware Monitor. 5. Add Clock Input Timing, PECI & SST Timing, and SPI Timing in Chapter 21 Specifications. 6. Remove sections 9.4 and 9.5 (EXTFDD and EXT2FDD). 7. Modify the descriptions of Hardware Monitor Device, Bank 0, Index 59h, bits(6..4). 8. Add a beep control bit for VIN4 at Hardware Monitor Device, Bank 0, Index 57h, bit6. 9. Remove status bit of PME# status of MIDI IRQ event at Logical Device A, CRF4, bit 1. 10. Remove control bit of enable/disable PME# of MIDI at Logical Device A, CRF7, bit 1. 11. Modify the descriptions of Tape Drive Register in Chapter 10 Floppy Disk Controller. 12. Correct the description of Digital Input Register, bit (6-4) in Chapter 10 Floppy Disk Controller. 13. Remove the description of “MR pin” in Digital Output Register in Chapter 10 Floppy Disk Controller. 14. Adapt “Serial Flash Interface” to “Serial Peripheral Interface”. 15. Modify “Absolute Maximum Ratings” in Chapter 21 Specifications. 16. Remove “V_{DD} is 5V± 10% tolerance” from the description of DC Characteristics in Chapter 21 Specifications. 17. Update “$S5_{cold}$ state” to “S5 state. 18. Remove the section of “AT Interface” in Chapter 10 Floppy Disk Controller.
9	N.A.	10/05/2006	1.0	N.A.	1. Update AC Timing parameters and waveforms.
10	N.A.	12/12/2006	1.1	N.A.	1. Update Table 9.1 and Table 9.2 in Chapter 9 Serial Peripheral Interface 2. Update CR2Ah in Chapter 20 Configuration Register 3. Modify CR24h bit 0 to reserved

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
					4. Use “Tbase” instead of “TControl” 5. Add the pins, registers description and AC timing for new ACPI function – VSBGATE#, ATXPGD, FTPRST, PWROK2 and SUSC#
11	N.A.	01/25/2007	1.2	N.A.	1. Modify the description for VSBGATE#, ATXPGD, FTPRST. 2. Revise the definition for Logical Device A, CR[E5h] bit 0. 3. Add new section of PWROK Generation in Chapter 14 Power Management Event. 4. Add new timing of VSBGATE# in Chapter 21 Specifications. 5. Modify the description of CR[2Ah], bits [7:4]. 6. Modify the “t1” timing of RSMRST#. 7. Modify the descriptions of 7.7.2 OVT# Interrupt Mode. 8. Modify the “t3” and “t4” timing in Table 14.4 and section 21.3.3
12	N.A.	03/28/2007	1.3	N.A.	1. Add a new DC spec. of RSMRST# PWROK for UBF version (In section 14.3 and 14.4) 2. Add LPC Timing in section 21.4 3. Remove redundant Power on/off and LRESET# Timing
13	N.A.	04/10/2007	1.4	N.A.	1. Modify LPC Timing in section 21.4

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

Table of Contents-

1. GENERAL DESCRIPTION

The W83627DHG is a member of Winbond's Super I/O product line. This family features the LPC (Low Pin Count) interface. This interface is more economical than its ISA counterpart, in that it has approximately forty pins fewer, yet still provides as great performance. In addition, the improvement allows even more efficient operation of software, BIOS and device drivers.

In addition to providing an LPC interface for I/O, the W83627DHG monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures. In terms of temperature monitoring, the W83627DHG adopts the Current Mode (dual current source) approach. The W83627DHG also supports the Smart Fan control system, including "SMART FAN™ I and SMART FAN™ III, which makes the system more stable and user-friendly.

The W83627DHG supports four -- 360K, 720K, 1.2M, 1.44M, or 2.88M -- disk drive types and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s,1 Mb/s, and 2 Mb/s. The disk drive adapter supports the functions of floppy disk drive controller (compatible with the industry standard 82077/ 765), data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. Such a wide range of functions integrated into one W83627DHG greatly reduces the number of required components to interface with floppy disk drives.

The W83627DHG provides two high-speed serial communication ports (UARTs), one of which provides IR functions IrDA 1.0 (SIR for 1.152K bps). Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem-control capability, and a processor interrupt system. Both UARTs support legacy speeds up to 115.2K bps as well as even higher baud rates of 230K, 460K, or 921K bps to support higher speed modems.

The W83627DHG supports the PC-compatible printer port (SPP), the bi-directional printer port (BPP), the enhanced parallel port (EPP) and the extended capabilities port (ECP).

The W83627DHG provides a bridge of the Low Pin Count interface to Serial Peripheral Interface (SPI) that supports up to 8M bits serial flash ROM. The W83627DHG provides flexible I/O control functions through a set of 40 general purpose I/O (GPIO) ports. These GPIO ports may serve as simple I/O ports or may be individually configured to provide alternative functions.

The W83627DHG supports the SST (Simple Serial Transport) interface and Intel® PECI (Platform Environment Control Interface).

The W83627DHG fully complies with the Microsoft© PC98, PC99 and PC2001 System Design Guides and meets the requirements of ACPI.

The configuration registers inside the W83627DHG support mode selection, function enable and disable, and power-down selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature in Windows 95/98/2000/XP™, making the allocation of the system resources more efficient than ever.

One special characteristic of the Super I/O product line is the separation of the power supply in normal operation from that in standby operation. Please pay attention to the layout of these two power supplies to avoid short circuits. Otherwise, the feature will not function.

2. FEATURES

General

- Meet LPC Spec. 1.01
- Support LDRQ# (LPC DMA), SERIRQ (Serialized IRQ)
- Integrated hardware monitor functions
- Compliant with Microsoft PC98/PC99/PC2001 System Design Guide
- Support DPM (Device Power Management), ACPI (Advanced Configuration and Power Interface)
- Programmable configuration settings
- Single 24- or 48-MHz clock input
- Support selective pins of 5 V tolerance

FDC

- Variable write pre-compensation with track-selection capability
- Support vertical recording format
- DMA-enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detect all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD-write enable signal (write data signal forced to be inactive)
- Support 3.5-inch or 5.25-inch floppy disk drives
- Compatible with industry standard 82077
- 360K / 720K / 1.2M / 1.44M / 2.88M formats
- 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support 3-mode FDD and its Windows driver

UART

- Two high-speed, 16550-compatible UARTs with 16-byte send / receive FIFOs
- Fully programmable serial-interface characteristics:
  --- 5, 6, 7 or 8-bit characters
  --- Even, odd or no parity bit generation/detection
  --- 1, 1.5 or 2 stop-bit generation
- Internal diagnostic capabilities:
  --- Loop-back controls for communications link fault isolation
  --- Break, parity, overrun, framing error simulation
- Programmable baud rate generator allows division of clock source by any value from 1 to (2^{16}-1)
- Maximum baud rate for clock source 14.769 MHz is up to 921K bps. The baud rate at 24 MHz is 1.5 M bps.

Parallel Port

- Compatible with IBM parallel port
- Support PS/2-compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) - Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) - Compatible with IEEE 1284 specification
- Enhanced printer port back-drive current protection

Keyboard Controller

- 8042-based keyboard controller
- Asynchronous Access to two data registers and one status register
- Software-compatible with 8042
- Support PS/2 mouse
- Support Port 92
- Support both interrupt and polling modes
- Fast Gate A20 and Hardware Keyboard Reset
- 6, 8, 12, or 16 MHz operating frequency

Hardware Monitor Functions

- Smart Fan control system, supporting the functions of SMART FAN™ I -- "Thermal Cruise™" and "Speed Cruise™" modes, and SMART FAN™ III
- Programmable threshold temperature to speed fan fully while current temperature exceeds this threshold in the Thermal Cruise™ mode
- Three thermal inputs from the different combinations of remote thermistors, and the thermal diode output
- Support Current Mode (dual current source) temperature sensing method
- Nine voltage inputs (CPUVCORE, VIN[0..3] and 3VCC, AVCC , 3VSB, VBAT)
- Five fan-speed monitoring inputs
- Four fan-speed controls
- Dual mode for fan control (PWM and DC)
- Built-in case open detection circuit
- Programmable hysteresis and setting points for all monitored items
- Over-temperature indicator output
- Issue SMI#, OVT# to activate system protection
- Winbond Hardware Doctor™ support
- Eight VID inputs / outputs
- Provide I^2C interface to read / write registers

Serial Peripheral Interface

- Support up to 8M bits SPI Flash Memory with clock up to 33 MHz
- Support Mode 0 and Mode 3

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps

General Purpose I/O Ports

- 40 programmable general purpose I/O ports
- GPIO port 4 supports the optional functions of Watchdog Timer Out and Suspend LED Output
- GP30, GP31 and GP35 can distinguish whether the input pins undergo any transitions by reading the registers. All of the 3 GPIOs can assert PSOUT# or PME# to wake up the system if each of them undergoes any transition.

OnNow Functions

- Keyboard Wake-Up by programmable keys
- Mouse Wake-Up by programmable buttons
- OnNow Wake-Up from all of the ACPI sleeping states (S1-S5)

Simple Serial Transport™ Interface

- SST temperature and voltage Combination Sensor command support
- Support SST 0.9 Specification

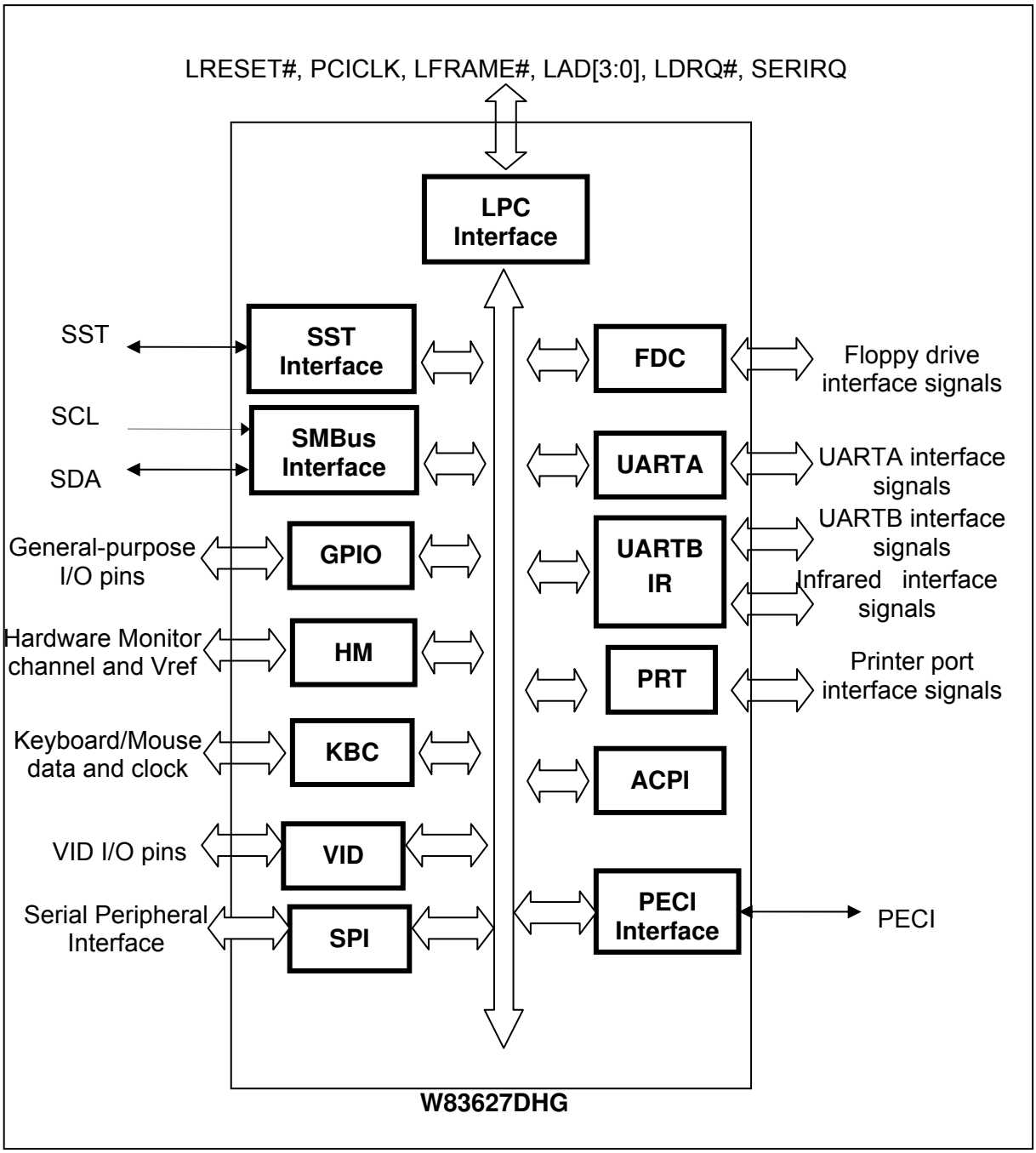
PECI Interface

- Support PECI 1.0 Specification
- Support 4 CPU addresses and 2 domains per CPU address

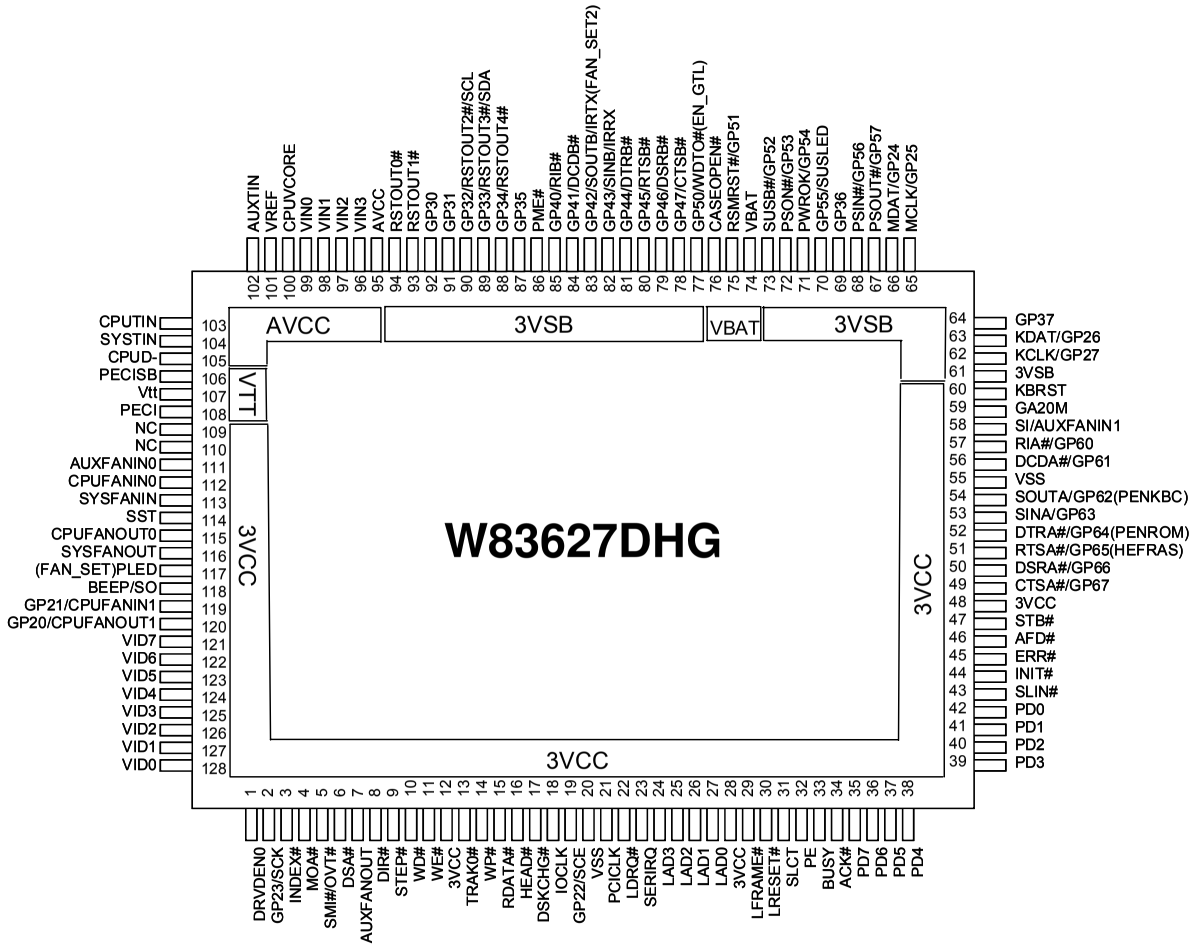
Package

- 128-pin QFP
- Pb-free/RoHS

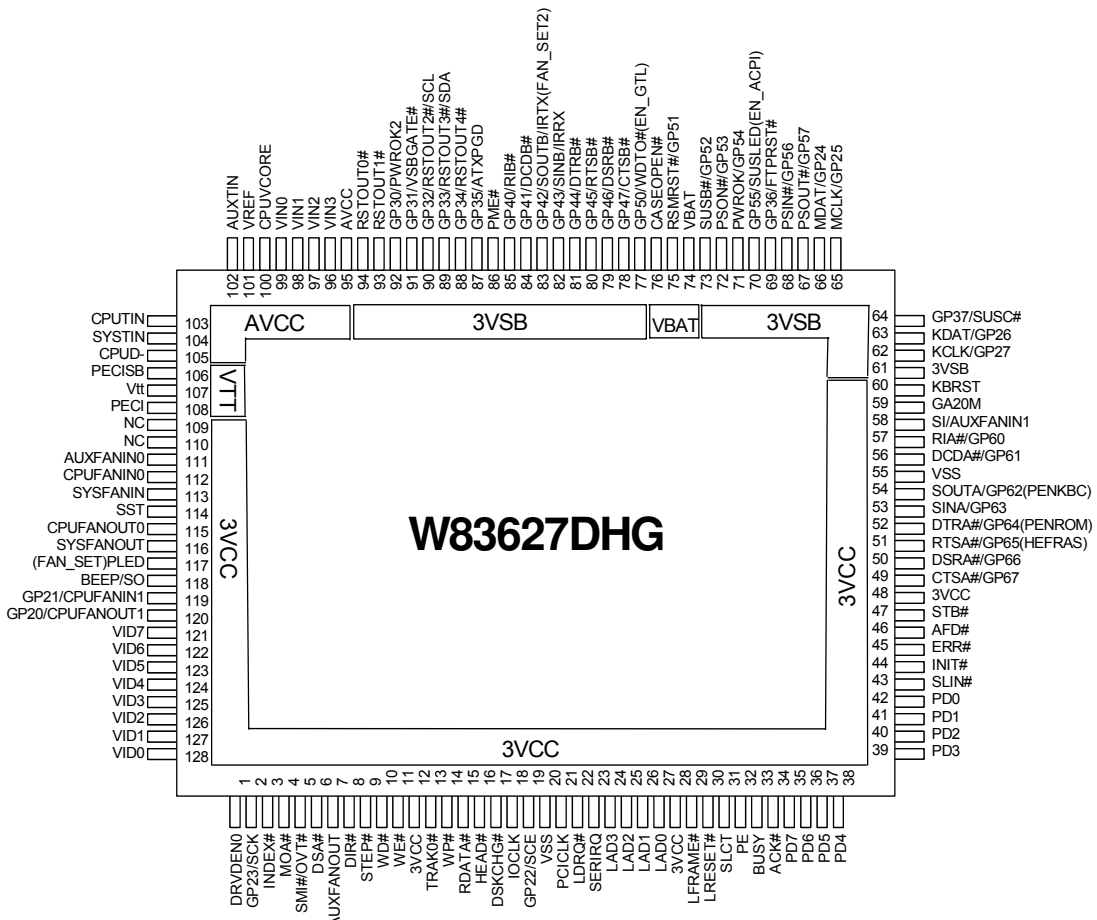
3. BLOCK DIAGRAM



4. PIN LAYOUT



Pin Layout for W83627DHG UBC version



Pin Layout for W83627DHG UBE and UBF version

5. PIN DESCRIPTION

Note: Please refer to Section 21.2 DC CHARACTERISTICS for details.

AOUT - Analog output pin
AIN - Analog input pin
IN_{cd} - CMOS-level input pin with internal pull-down resistor
IN_{cs} - CMOS-level, Schmitt-trigger input pin
IN_{csu} - CMOS-level, Schmitt-trigger input pin with internal pull-up resistor
IN_{t} - TTL-level input pin
IN_{td} - TTL-level input pin with internal pull-down resistor
IN_{ts} - TTL-level, Schmitt-trigger input pin
IN_{tp3} - 3.3V, TTL-level input pin
IN_{tsp3} - 3.3V TTL level Schmitt-trigger input pin
IN_{tu} - TTL-level input pin with internal pull-up resistor
I/O_{8} - bi-directional pin with 8-mA source-sink capability
I/O_{8t} - TTL-level, bi-directional pin with 8-mA source-sink capability
I/O_{12} - bi-directional pin with 12-mA source-sink capability
I/O_{12t} - TTL-level, bi-directional pin with 12-mA source-sink capability
I/O_{12ts} - Schmitt-trigger, bi-directional pin with 12-mA source-sink capability
I/O_{12tp3} - 3.3V, TTL-level, bi-directional pin with 12-mA source-sink capability
I/OD_{8t} - TTL-level, bi-directional pin. Open-drain output with 8-mA sink capability
I/OD_{12} - Bi-directional pin. Open-drain output with 12-mA sink capability
I/OD_{12t} - TTL-level bi-directional pin. Open-drain output with 12-mA sink capability
I/OD_{12cs} - CMOS-level, bi-directional, Schmitt-trigger pin. Open-drain output with 12-mA sink capability
I/OD_{12ts} - TTL-level, bi-directional, Schmitt-trigger pin. Open-drain output with 12-mA sink capability
I/OD_{12tp3} - 3.3V, TTL-level, bi-directional pin. Open-drain output with 12-mA sink capability
I/OD_{16t} - TTL-level, bi-directional pin. Open-drain output with 16-mA sink capability
I/OD_{16ts} - Schmitt-trigger, bi-directional pin. Open-drain output with 16-mA sink capability
I/OD_{16cs} - CMOS-level, Schmitt-trigger, bi-directional pin. Open-drain output with 16-mA sink capability
I/OD_{24t} - TTL-level, bi-directional pin. Open-drain output with 24-mA sink capability
O_{12p3} - 3.3V output pin with 12-mA source-sink capability
O_{12tp3} - 3.3V, TTL-level output pin with 12-mA source-sink capability
O_{8} - TTL-level output pin with 8-mA source-sink capability
O_{12} - TTL-level output pin with 12-mA source-sink capability
O_{24} - TTL-level output pin with 24-mA source-sink capability
OD_{8} - Open-drain output pin with 8-mA sink capability
OD_{12} - Open-drain output pin with 12-mA sink capability
OD_{24} - Open-drain output pin with 24-mA sink capability
I/O_{V3} - Bi-direction pin with source capability of 6 mA and sink capability of 1 mA

5.1 LPC Interface

SYMBOL	PIN	I/O	DESCRIPTION
IOCLK	18	IN_{tp3}	System clock input, either 24MHz or 48MHz. The actual frequency must be specified in the register. The default value is 48MHz.
PME#	86	OD_{12p3}	Generated PME event.
PCICLK	21	IN_{tsp3}	PCI-clock 33-MHz input.
LDRQ#	22	O_{12p3}	Encoded DMA Request signal.
SERIRQ	23	I/OD_{12tp3}	Serialized IRQ input / output.
LAD[3:0]	24-27	I/O_{12tp3}	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
LFRAME#	29	IN_{tsp3}	Indicates the start of a new cycle or the termination of a broken cycle.
LRESET#	30	IN_{tsp3}	Reset signal. It can be connected to the PCIRST# signal on the host.

5.2 FDC Interface

SYMBOL	PIN	I/O	DESCRIPTION
DRVDEN0	1	OD_{24}	Drive Density Select bit 0.
INDEX#	3	IN_{cs}	This Schmitt-trigger input from the disk drive is active-low when the head is positioned over the beginning of a track marked by an index hole. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
MOA#	4	OD_{24}	Motor A On. When set to 0, this pin activates disk drive A. This is an open-drain output.
DSA#	6	OD_{24}	Drive Select A. When set to 0, this pin activates disk drive A. This is an open-drain output.
DIR#	8	OD_{24}	Direction of the head step motor. An open-drain output. Logic 1 = outward motion Logic 0 = inward motion
STEP#	9	OD_{24}	Step output pulses. This active-low open-drain output produces a pulse to move the head to another track.
WD#	10	OD_{24}	Write data. This logic-low open-drain writes pre-compensation serial data to the selected FDD. An open-drain output.
WE#	11	OD_{24}	Write enable. An open-drain output.
TRAK0#	13	IN_{cs}	Track 0. This Schmitt-trigger input from the disk drive is active-low when the head is positioned over the outermost track. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.

FDC Interface, continued

SYMBOL	PIN	I/O	DESCRIPTION
WP#	14	IN_{cs}	Write protected. This active-low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
RDATA#	15	IN_{cs}	The read-data input signal from the FDD. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
HEAD#	16	OD_{24}	Head selection. This open-rain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
DSKCHG#	17	IN_{cs}	Diskette change. This signal is active-low at power-on and whenever the diskette is removed. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.

5.3 Multi-Mode Parallel Port

SYMBOL	PIN	I/O	DESCRIPTION
SLCT	31	IN_{ts}	PRINTER MODE: An active-high input on this pin indicates that the printer is selected. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
PE	32	IN_{ts}	PRINTER MODE: An active-high input on this pin indicates that the printer has detected the end of the paper. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
BUSY	33	IN_{ts}	PRINTER MODE: An active-high input indicates that the printer is not ready to receive data. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
ACK#	34	IN_{ts}	PRINTER MODE: ACK# An active-low input on this pin indicates that the printer has received data and is ready to accept more data. See the descriptions of the parallel port for the definition of this pin in ECP and EPP modes.
ERR#	45	IN_{ts}	PRINTER MODE: ERR# An active-low input on this pin indicates that the printer has encountered an error condition. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
SLIN#	43	OD_{12}	PRINTER MODE: SLIN# Output line for detection of printer selection. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.

Multi-Mode Parallel Port, continued.

SYMBOL	PIN	I/O	DESCRIPTION
INIT#	44	OD_{12}	PRINTER MODE: INIT# Output line for the printer initialization. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
AFD#	46	OD_{12}	PRINTER MODE: AFD# An active-low output from this pin causes the printer to auto feed a line after a line is printed. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
STB#	47	OD_{12}	PRINTER MODE: STB# An active-low output is used to latch the parallel data into the printer. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
PD0	42	I/O_{12ts}	PRINTER MODE: PD0 Parallel port data bus bit 0. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
PD1	41	I/O_{12ts}	PRINTER MODE: PD1 Parallel port data bus bit 1. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
PD2	40	I/O_{12ts}	PRINTER MODE: PD2 Parallel port data bus bit 2. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
PD3	39	I/O_{12ts}	PRINTER MODE: PD3 Parallel port data bus bit 3. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
PD4	38	I/O_{12ts}	PRINTER MODE: PD4 Parallel port data bus bit 4. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
PD5	37	I/O_{12ts}	PRINTER MODE: PD5 Parallel port data bus bit 5. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
PD6	36	I/O_{12ts}	PRINTER MODE: PD6 Parallel port data bus bit 6. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
PD7	35	I/O_{12ts}	PRINTER MODE: PD7 Parallel port data bus bit 7. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.

5.4 Serial Port & Infrared Port Interface

SYMBOL	PIN	I/O	DESCRIPTION
RIA#	57	IN_t	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
GP60		I/OD_{12t}	General-purpose I/O port 6 bit 0.
DCDA#	56	INt	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
GP61		I/OD_{12t}	General-purpose I/O port 6 bit 1.
SOUTA	54	O_8	UART A Serial Output. This pin is used to transmit serial data out to the communication link.
PENKBC		IN_t	During power on reset, this pin is pulled down internally and is defined as PENKBC, and the power-on values are shown at CR24 bit 2. The PCB layout should reserve space for a 1-kΩ resistor to pull down this pin to ensure the disabling of KBC, and a 1-kΩ resistor is recommended to pull the pin up If wish to enable KBC.
GP62		I/O_8	General-purpose I/O port 6 bit 2.
SINA	53	IN_t	Serial Input. This pin is used to receive serial data through the communication link.
GP63		I/OD_{12t}	General-purpose I/O port 6 bit 3.
DTRA#	52	O_8	UART A Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
PENROM		IN_t	During power-on reset, this pin is pulled down internally and is defined as PENROM disabled, and the power-on values are shown at CR24 bit 1 (ENROM). The PCB layout should reserve space for a 1-kΩ resistor to pull down this pin to ensure the disabling of SPI interface, and a 1-kΩ resistor is recommended to pull the pin up if wish to enable ROM.
GP64		I/O_8	General-purpose I/O port 6 bit 4.
RTSA#	51	O_8	UART A Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
HEFRAS		IN_t	During power-on reset, this pin is pulled down internally and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). The PCB layout should reserve space for a 1-kΩ resistor to pull down this pin so as to ensure the selection of I/O port's configuration address to 2EH, and a 1-kΩ resistor is recommended to pull it up if 4EH is selected as I/O port's configuration address.
GP65		I/O_8	General-purpose I/O port 6 bit 5.
DSRA#	50	IN_t	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
GP66		I/OD_{12t}	General-purpose I/O port 6 bit 6.

Serial Port & Infrared Port Interface , continued.

SYMBOL	PIN	I/O	DESCRIPTION
CTSA#	49	IN_t	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
GP67		I/OD_{12t}	General-purpose I/O port 6 bit 7.
RIB#	85	IN_t	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
GP40*		I/OD_{12t}	General-purpose I/O port 4 bit 0.
DCDB#	84	IN_t	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
GP41***		I/OD_{12t}	General-purpose I/O port 4 bit 1.
FAN_SET2	83	IN_t	Determines the initial FAN speed. Power-on configuration for 2 fan speeds, 50% or 100%. When VCC is on, this pin needs a pulled-up or a pulled-down resistor to decide whether the fan speed is 50% or 100%. Only CPUFANOUT1 is supported.
SOUTB		O_{12}	UART B Serial Output. This pin is used to transmit serial data out to the communication link.
IRTX			IR Transmitter output.
GP42*		I/O_{12t}	General-purpose I/O port 4 bit 2. Note: This pin changes to input state during internal PWROK from low to high, then goes back to the previous setting state. (Please see the AP Note 1 of W83627DHG)
SINB	82	IN_t	Serial Input. This pin is used to receive serial data through the communication link.
IRRX			IR Receiver input.
GP43***		I/OD_{12t}	General-purpose I/O port 4 bit 3.
DTRB#	81	O_{12}	UART B Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
GP44*		I/OD_{12t}	General-purpose I/O port 4 bit 4.
RTSB#	80	O_{12}	UART B Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
GP45***		I/OD_{12t}	General-purpose I/O port 4 bit 5.
DSRB#	79	IN_t	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
GP46*		I/OD_{12t}	General-purpose I/O port 4 bit 6.
CTSB#	78	IN_t	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
GP47***		I/OD_{12t}	General-purpose I/O port 4 bit 7.

Note: Regarding the * sign, please see 5.11.8 GPIO-4 for detailed WDTO# / SUSLED multi-function information.