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W83627EHF/EF

W83627EHG/EG

WINBOND LPC I/O

Date : November/16/2006 Revision :1.3

Data Sheet Revision History

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
1		10/01/2004	0.5	N/A	First published preliminary version.
2		11/09/2004	0.51	N/A	Correct typo at 5.11.
3		12/07/2004	0.52	N/A	1. Correct DC CHARACTERISTICS description 2. Update Demo Circuit 3. Add Pb-free part no:W83627EHG
4		03/18/2005	0.6	N/A	Add SMART FAN™ III description
5		06/10/2005	0.61	N/A	Update application circuit
6		07/06/2005	0.62	N/A	Add new part W83627EF and W83627EG.
7		07/19/2005	0.63	N/A	Update pin configuration and application circuit
8		9/13/2005	1.0	N/A	Correct information and add AC Power Loss Timing chart
9	P.18	02/14/2006	1.1	N/A	Correct LPT function pins description.
10	P.79; P.80	08/04/2006	1.2	N/A	Remove “2N3904 activation” selection
11	P.103, P.104	11/16/2006	1.3	N/A	Correct description of CRF0 of Logical Device 2/3 (UARTA/B)

winbond

Table of Contents-

1. GENERAL DESCRIPTION

W83627EHF/EHG/EF/EG is an evolving product from Winbond's most popular I/O family. They feature a whole new interface, namely LPC (Low Pin Count) interface, which will be supported in the new generation chip-set. This interface as its name suggests is to provide an economical implementation of I/O's interface with lower pin count and still maintains equivalent performance as its ISA interface counterpart. Approximately 40 pin counts are saved in LPC I/O comparing to ISA implementation. It is fully transparent in terms of software which means no BIOS or device driver update is needed except chip-specific configuration.

The disk drive adapter functions of W83627EHF/EHG/EF/EG include a floppy disk drive controller compatible with the industry standard 82077/ 765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. The wide range of functions integrated onto the W83627EHF/EHG/EF/EG greatly reduces the number of components required for interfacing with floppy disk drives. W83627EHF/EHG/EF/EG supports four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s,1 Mb/s, and 2 Mb/s.

W83627EHF/EHG/EF/EG provides two high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. Both UARTs provide legacy speed with baud rate up to 115.2k bps and also advanced speed with baud rates of 230k, 460k, or 921k bps which support higher speed modems. In addition, W83627EHF/EHG/EF/EG provides IR functions: IrDA 1.0 (SIR for 1.152K bps) .

W83627EHF/EHG/EF/EG supports one PC-compatible printer port (SPP), Bi-directional Printer port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). And W83627EHF/EHG/EF/EG contains a Game port and a MIDI port. The game port is designed to support 2 joysticks and can be applied to all standard PC game control devices, they are very important for a entertainment or consumer computer.

W83627EHF/EHG/EF/EG provides Serial Flash ROM interface. That can support up to 8M bits serial flash ROM.

W83627EHF/EHG/EF/EG provides flexible I/O control functions to the system designer through a set of General Purpose I/O ports. These GPIO ports may serve as simple I/O or may be individually configured to provide a predefined alternate function.

W83627EHF/EHG supports hardware status monitoring for personal computers. It can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system to work stably and properly. Moreover, W83627EHF/EHG supports the Smart Fan control system, including the "Thermal Cruise™" and "Speed Cruise™" functions. Smart Fan can make system more stable and user friendly.

W83627EHF/EHG/EF/EG is made to fully comply with Microsoft© PC98 and PC99 Hardware Design Guide, and meet the requirements of ACPI.

The configuration registers support mode selection, function enable/disable, and power down function selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature demand of Windows 95/98™, which makes system resource allocation more efficient than ever.

The special characteristic of Super I/O product line is to avoid power rails short. This is especially true to a multi-power system where power partition is much more complex than a single-power one. Special care might be applied during layout stage or the IC will fail even though its intended function is workable.

2. FEATURES

General

- Meet LPC Spec. 1.01
- Support LDRQ#(LPC DMA), SERIRQ (Serial IRQ)
- Integrated Hardware Monitor functions
- Compliant with Microsoft PC2000/PC2001 Hardware Design Guide
- Support DPM (Device Power Management), ACPI
- Programmable configuration settings
- Single 24 or 48 MHz clock input
- It is 3.3V level but 5V tolerance support

  --- Besides LPC function pins(Pin21 ~ Pin30) and H/W monitor analog pins(Pin95 ~ Pin110)

  --- Input level can up to 5V and maximum input level can be up to 5V+10%

FDC

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- Support vertical recording format
- DMA enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detects all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD write enable signal (write data signal was forced to be inactive)
- Support up to four 3.5-inch or 5.25-inch floppy disk drives
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support 3-mode FDD, and its Win95/98 driver

UART

- Two high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs
- MIDI compatible
- Fully programmable serial-interface characteristics:

  --- 5, 6, 7 or 8-bit characters

  --- Even, odd or no parity bit generation/detection

  --- 1, 1.5 or 2 stop bits generation

- Internal diagnostic capabilities:

  --- Loop-back controls for communications link fault isolation

  --- Break, parity, overrun, framing error simulation

- Programmable baud rate generator allows division of 1.8461 MHz and 24 MHz by 1 to (216-1)
- Maximum baud rate up to 921k bps for 14.769 MHz and 1.5M bps for 24 MHz

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps

Parallel Port

- Compatible with IBM parallel port
- Support PS/2 compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) - Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) - Compatible with IEEE 1284 specification
- Enhanced printer port back-drive current protection

Game Port

- Support two separate Joysticks
- Support every Joystick two axis (X, Y) and two button (A, B) controllers

MIDI Port

- The baud rate is 31.25 K baud
- 16-byte input FIFO
- 16-byte output FIFO

Keyboard Controller

- 8042 based with optional F/W from AMIKKEYTM-2, Phoenix MultiKey/42TM or customer code with 2K bytes of programmable ROM, and 256 bytes of RAM
- Asynchronous Access to Two Data Registers and One status Register
- Software compatibility with the 8042
- Support PS/2 mouse
- Support port 92
- Support both interrupt and polling modes
- Fast Gate A20 and Hardware Keyboard Reset
- 8 Bit Timer/ Counter
- Support binary and BCD arithmetic
- 6 MHz, 8 MHz, 12 MHz, or 16 MHz operating frequency

Serial Flash ROM Interface

- Support up to 8M bits flash ROM

General Purpose I/O Ports

- 48 programmable general purpose I/O ports
- GPIO port 1 and 4 can not only serve as simple I/O ports but also watch dog timer output, Power LED output, Suspend LED output
- Functional in power down mode (GP24 ~ GP27, GPIO-3, GPIO-4, GPIO-5)

OnNow Functions

- Keyboard Wake-Up by programmable keys
- Mouse Wake-Up by programmable buttons
- On Now Wake-Up from all of the ACPI sleeping states (S1-S5)

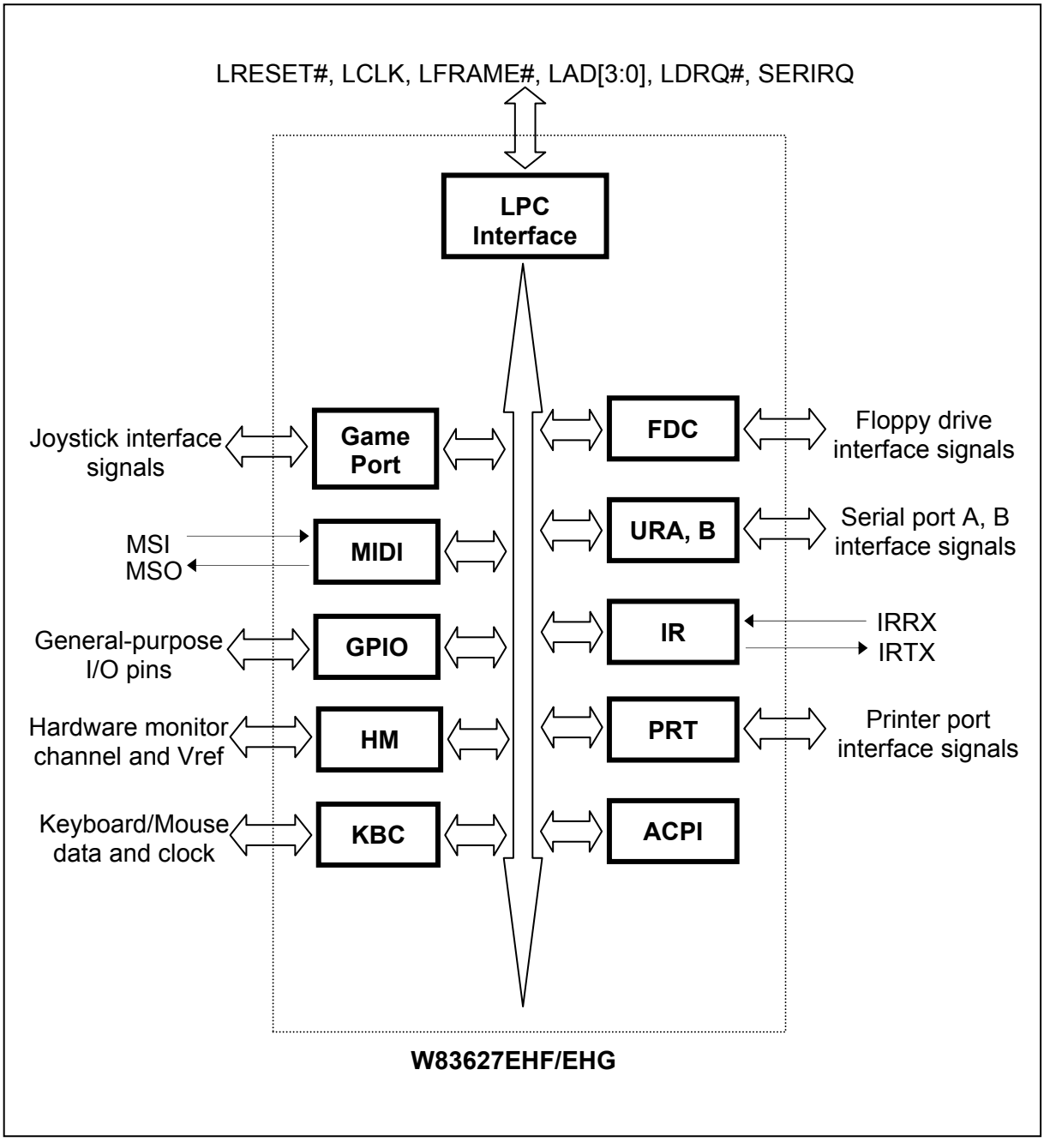
Hardware Monitor Functions (For W83627EHF/EHG only)

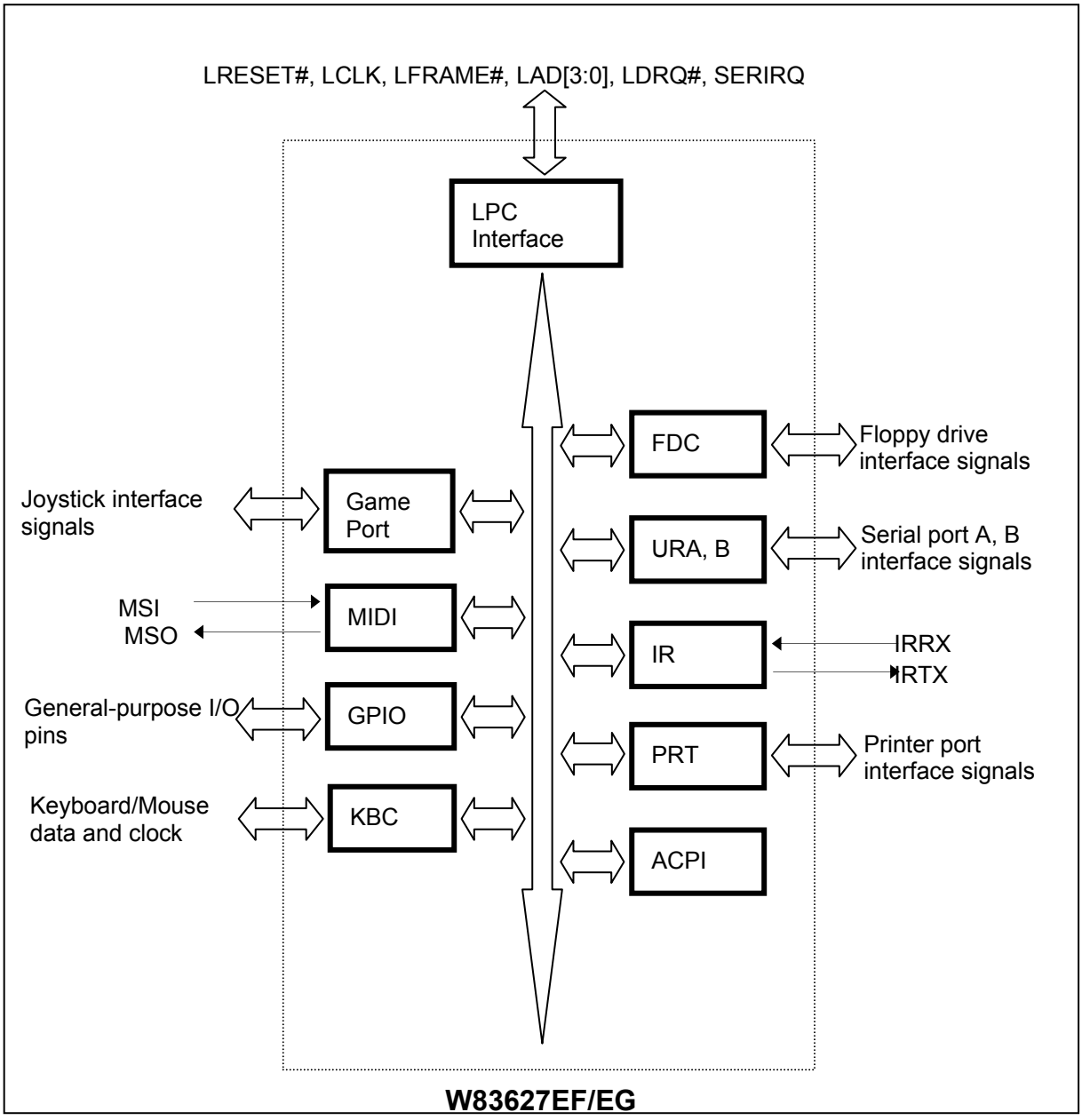
- Smart Fan control system, support SMART FANTM I - "Thermal CruiseTM" and "Speed CruiseTM" Mode , SMART FANTM III function
- 3 thermal inputs from optionally remote thermistors or entiumTM II/III/4 thermal diode output
- 10 voltage inputs (CPUVCORE, VIN[0..4] and intrinsic 3VCC, AVCC , 3VSB, VBAT)
- 5 fan speed monitoring inputs
- 4 fan speed control
- Dual mode for fan control (PWM & DC)
- Build in case open detection circuit
- Programmable hysteresis and setting points for all monitored items
- Over temperature indicate output
- Issue SMI#, OVT# to activate system protection
- Winbond Hardware DoctorTM Support
- 6 VID inputs / outputs
- Provide I2C interface to read/write registers

Package

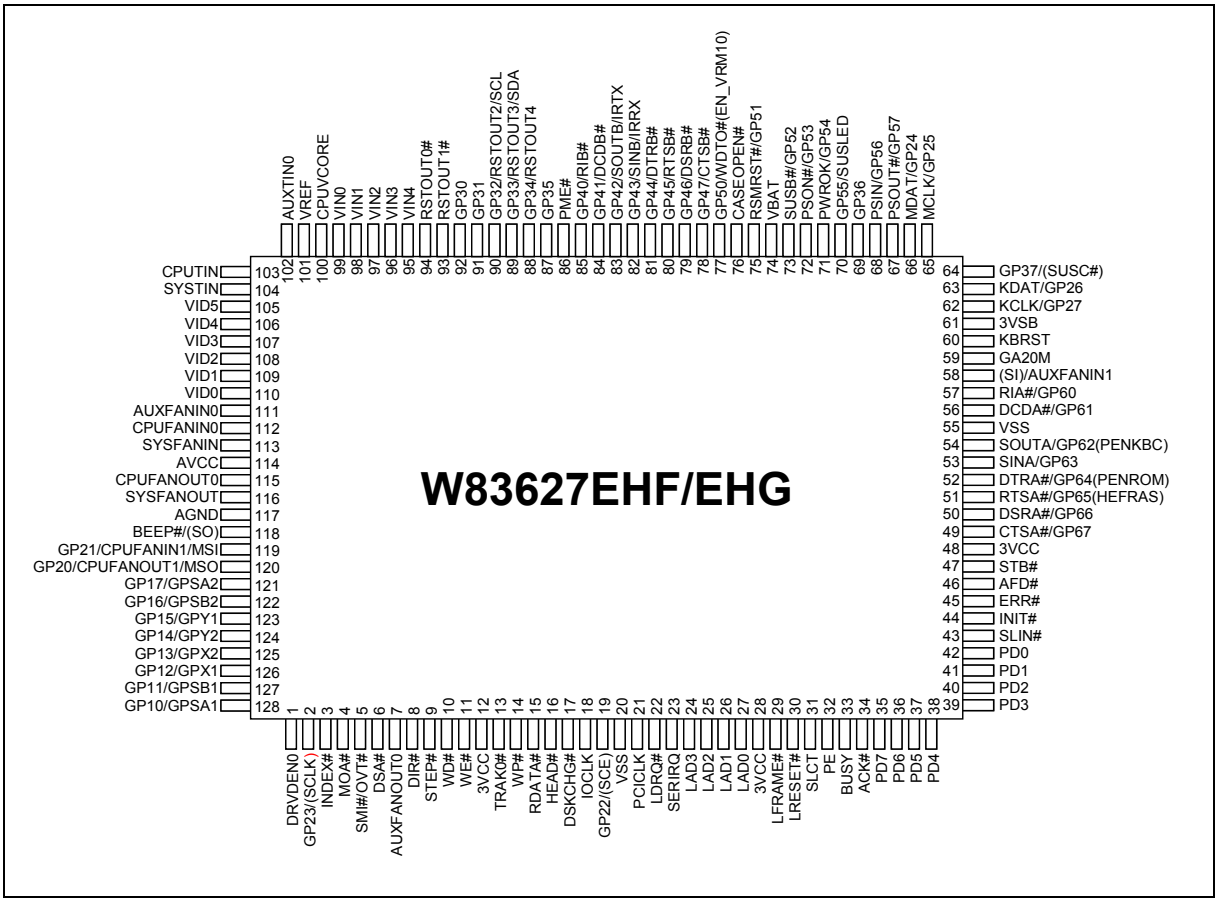
- 128-pin PQFP

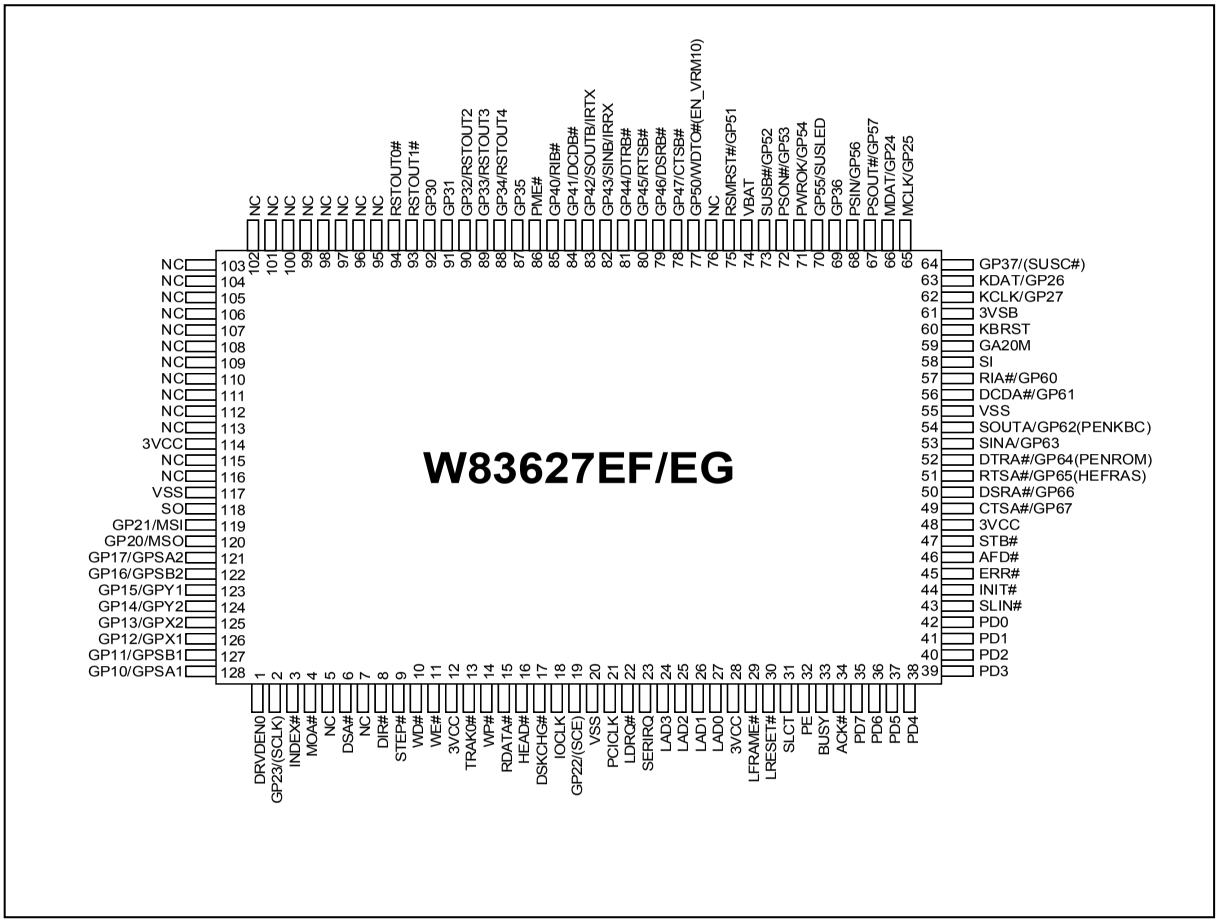
3. BLOCK DIAGRAM




LRESET#, LCLK, LFRAME#, LAD[3:0], LDRQ#, SERIRQ
LPC Interface
FDC
Floppy drive interface signals
Joystick interface signals
Game Port
URA, B
Serial port A, B interface signals
MSI
MSO
MIDI
IR
IRRX
IRTX
General-purpose I/O pins
GPIO
PRT
Printer port interface signals
Keyboard/Mouse data and clock
KBC
ACPI
W83627EF/EG

4. PIN CONFIGURATION




W83627EF/EG
1 DRVDEN0
2 GP23/(SCLK)
3 INDEX#
4 MOA#
5 NC
6 DSA#
7 NC
8 DIR#
9 STEP#
10 WD#
11 WE#
12 3VCC
13 TRAK0#
14 WP#
15 RDATA#
16 HEAD#
17 DSKCHG#
18 IOCLK
19 GP22/(SCE)
20 VSS
21 PCICLK
22 LDRQ#
23 SERIRQ
24 LAD3
25 LAD2
26 LAD1
27 LAD0
28 3VCC
29 LFRAME#
30 LRESET#
31 SLCT
32 PE
33 BUSY
34 ACK#
35 PD7
36 PD6
37 PD5
38 PD4
39 PD3
40 PD2
41 PD1
42 PD0
43 SLIN#
44 INIT#
45 ERR#
46 AFD#
47 STB#
48 3VCC
49 CTSA#/GP67
50 DSRA#/GP66
51 RTSA#/GP65(HEFRAS)
52 DTRA#/GP64(PENROM)
53 SINA/GP63
54 SOUTA/GP62(PENKBC)
55 VSS
56 DCDA#/GP61
57 RIA#/GP60
58 SI
59 GA20M
60 KBRST
61 3VSB
62 KCLK/GP27
63 KDAT/GP26
64 GP37/(SUSC#)
65 MCLK/GP25
66 MDAT/GP24
67 PSOUT#/GP57
68 PSIN/GP56
69 GP36
70 GP55/SUSLED
71 PWROK/GP54
72 PSON#/GP53
73 SUSB#/GP52
74 VBAT
75 RSMRST#/GP51
76 NC
77 GP50/WDTO#(EN_VRM10)
78 GP47/CTSB#
79 GP46/DSRB#
80 GP45/RTSB#
81 GP44/DTRB#
82 GP43/SINB/IRRX
83 GP42/SOUTB/IRTX
84 GP41/DCDB#
85 GP40/RIB#
86 PME#
87 GP35
88 GP34/RSTOUT4
89 GP33/RSTOUT3
90 GP32/RSTOUT2
91 GP31
92 GP30
93 RSTOUT1#
94 RSTOUT0#
95 NC
96 NC
97 NC
98 NC
99 NC
100 NC
101 NC
102 NC
103 NC
104 NC
105 NC
106 NC
107 NC
108 NC
109 NC
110 NC
111 NC
112 NC
113 NC
114 3VCC
115 NC
116 NC
117 VSS
118 SO
119 GP21/MSI
120 GP20/MSO
121 GP17/GPSA2
122 GP16/GPSB2
123 GP15/GPY1
124 GP14/GPY2
125 GP13/GPX2
126 GP12/GPX1
127 GP11/GPSB1
128 GP10/GPSA1

5. PIN DESCRIPTION

Note: Please refer to Section 8.2 DC CHARACTERISTICS for details.

AOUT - Analog output pin
AIN - Analog input pin
IN_{cs} - CMOS level Schmitt-triggered input pin
IN_{t} - TTL level input pin
IN_{td} - TTL level input pin with internal pull down resistor
IN_{ts} - TTL level Schmitt-triggered input pin
IN_{tsp3} - 3.3V TTL level Schmitt-triggered input pin
IN_{tu} - TTL level input pin with internal pull up resistor
I/O_{8t} - TTL level bi-directional pin with 8 mA source-sink capability
I/O_{12t} -3.3V TTL level bi-directional pin with 12 mA source-sink capability
I/OD_{12ts} - 3.3V TTL level bi-directional Schmitt-triggered pin. Open-drain output with 12 mA sink capability
I/OD_{16cs} - CMOS level Schmitt-triggered bi-directional pin. Open-drain output with 16 mA sink capability
I/OD_{24t} - TTL level bi-directional pin. Open-drain output with 24 mA sink capability
OUT_{8} - TTL level output pin with 8 mA source-sink capability
OUT_{12} -3.3V TTL level output pin with 12 mA source-sink capability
OUT_{24} - TTL level output pin with 24 mA source-sink capability
OD_{8} - Open-drain output pin with 8 mA sink capability
OD_{12} - Open-drain output pin with 12 mA sink capability
OD_{24} - Open-drain output pin with 24 mA sink capability

5.1 LPC Interface

SYMBOL	PIN	I/O	FUNCTION
IOCLK	18	IN_{t}	System clock input, which is selective by the register according to the input frequency either 24MHz or 48MHz. Default is 48MHz.
PME#	86	OD_{12}	Generated PME event.
PCICLK	21	IN_{ts}	PCI clock 33 MHz input.
LDRQ#	22	O_{12}	Encoded DMA Request signal.
SERIRQ	23	I/OD_{12t}	Serial IRQ Input/Output.
LAD[3:0]	24-27	I/O_{12t}	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
LFRAME#	29	IN_{ts}	Indicates start of a new cycle or termination of a broken cycle.
LRESET#	30	IN_{ts}	Reset signal. It can connect to PCIRST# signal on the host.

5.2 FDC Interface

SYMBOL	PIN	I/O	FUNCTION
DRVDEN0	1	OD_{24}	Drive Density Select bit 0.
INDEX#	3	IN_{csu}	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin can be pulled up internally by a 1 KΩ(±50%). The resistor also can be disabled/enabled by bit 7 of LD0-CRF0(FIPURDWN). Default is disabled.
MOA#	4	OD_{24}	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
DSA#	6	OD_{24}	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
DIR#	8	OD_{24}	Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
STEP#	9	OD_{24}	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
WD#	10	OD_{24}	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
WE#	11	OD_{24}	Write enable. An open drain output.
TRAK0#	13	IN_{csu}	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track. This input pin can be pulled up internally by a 1 KΩ(±50%). The resistor also can be disabled/enabled by bit 7 of LD0-CRF0(FIPURDWN). Default is disabled.
WP#	14	IN_{csu}	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin can be pulled up internally by a 1 KΩ(±50%). The resistor also can be disabled/enabled by bit 7 of LD0-CRF0(FIPURDWN). Default is disabled.
RDATA#	15	IN_{csu}	The read data input signal from the FDD. This input pin can be pulled up internally by a 1 KΩ(±50%). The resistor also can be disabled/enabled by bit 7 of LD0-CRF0(FIPURDWN). Default is disabled.
HEAD#	16	OD_{24}	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
DSKCHG#	17	IN_{csu}	Diskette change. This signal is active low at power on and whenever the diskette is removed. This input pin can be pulled up internally by a 1 KΩ(±50%) . The resistor also can be disabled/enabled by bit 7 of LD0-CRF0 (FIPURDWN). Default is disabled.

5.3 Multi-Mode Parallel Port

SYMBOL	PIN	I/O	FUNCTION
SLCT	31	IN_{ts}	PRINTER MODE: An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
PE	32	IN_{ts}	PRINTER MODE: An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
BUSY	33	IN_{ts}	PRINTER MODE: An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
ACK#	34	IN_{ts}	PRINTER MODE: ACK# An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
ERR#	45	IN_{ts}	PRINTER MODE: ERR# An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
SLIN#	43	OD_{12} $/OUT_{12}$	PRINTER MODE: SLIN# Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
INIT#	44	OD_{12} $/OUT_{12}$	PRINTER MODE: INIT# Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
AFD#	46	OD_{12} $/OUT_{12}$	PRINTER MODE: AFD# An activtput from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
STB#	47	OD_{12} $/OUT_{12}$	PRINTER MODE: STB# An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
PD0	42	I/O_{12ts}	PRINTER MODE: PD0 Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.

Multi-Mode Parallel Port, continued.

SYMBOL	PIN	I/O	FUNCTION
PD1	41	I/O_{12ts}	PRINTER MODE: PD1 Parallel port data bus bit 1. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
PD2	40	I/O_{12ts}	PRINTER MODE: PD2 Parallel port data bus bit 2. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
PD3	39	I/O_{12ts}	PRINTER MODE: PD3 Parallel port data bus bit 3. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
PD4	38	I/O_{12ts}	PRINTER MODE: PD4 Parallel port data bus bit 4. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
PD5	37	I/O_{12ts}	PRINTER MODE: PD5 Parallel port data bus bit 5. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
PD6	36	I/O_{12ts}	PRINTER MODE: PD6 Parallel port data bus bit 6. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
PD7	35	I/O_{12ts}	PRINTER MODE: PD7 Parallel port data bus bit 7. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.

5.4 Serial Port & Infrared Port Interface

SYMBOL	PIN	I/O	FUNCTION
CTSA#	49	IN_t	Clear To Send. It is the modem control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
GP67		I/OD_{12t}	General purpose I/O port 6 bit 7.
CTSB#	78	IN_t	Clear To Send. It is the modem control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
GP47***		I/OD_{12t}	General purpose I/O port 4 bit 7.
DSRA#	50	IN_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
GP66		I/OD_{12t}	General purpose I/O port 6 bit 6.

Serial Port & Infrared Port Interface, Continued.

SYMBOL	PIN	I/O	FUNCTION
DSRB#	79	IN_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
GP46*		I/OD_{12t}	General purpose I/O port 4 bit 6.
RTSA#	51	OUT_8	UART A Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
HEFRAS		IN_t	During power-on reset, this pin is pulled down internally(20K± 30%) and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). A 1 kΩ is reserved to pull down and a 1 kΩ is recommended if intends to pull up. (select 4EH as configuration I/O port's address)
GP65		I/O_8	General purpose I/O port 6 bit 5.
RTSB#	80	OUT_8	UART B Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
GP45***		I/OD_{8t}	General purpose I/O port 4 bit 5.
DTRA#	52	OUT_8	UART A Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate.
PENROM		IN_t	During power-on reset, this pin is pulled down internally(20K ± 30%)and is defined as PENROM disable, which provides the power-on value for CR24 bit 1 (ENROM). A 1 kΩ is reserved to pull down and a 1 kΩ resistor is recommended if intends to pull-up to enable ROM.
GP64		I/O_8	General purpose I/O port 6 bit 4.
DTRB#	81	OUT_8	UART B Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
GP44*		I/OD_{8t}	General purpose I/O port 4 bit 4.
SINA	53	IN_t	Serial Input. It is used to receive serial data through the communication link.
GP63		I/OD_8	General purpose I/O port 6 bit 3.
SINB	82	IN_t	Serial Input. It is used to receive serial data through the communication link.
IRRX			IR Receiver input.
GP43***		I/OD_{12}	General purpose I/O port 4 bit 3.

Serial Port & Infrared Port Interface, Continued.

SYMBOL	PIN	I/O	FUNCTION
SOUTA	54	OUT_8	UART A Serial Output. It is used to transmit serial data out to the communication link.
PENKBC		IN_t	During power on reset, this pin is pulled down internally(20K ± 30%)and is defined as PENKBC, which provides the power on value for CR24 bit 2. A 1 kΩ is reserved to pull down and a 1 kΩ is recommended if intends to pull up.
GP62		I/O_8	General purpose I/O port 6 bit 2.
SOUTB	83	OUT_8	UART B Serial Output. It is used to transmit serial data out to the communication link.
IRTX			IR Transmitter output.
GP42*		I/OD_8	General purpose I/O port 4 bit 2.
DCDA#	56	IN_t	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
GP61		I/OD_{12}	General purpose I/O port 6 bit 1.
DCDB#	84	IN_t	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
GP41***		I/OD_{12}	General purpose I/O port 4 bit 1.
RIA#	57	IN_t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
GP60	57	I/OD_{12}	General purpose I/O port 6 bit 0.
RIB#	85	IN_t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
GP40*		I/OD_12	General purpose I/O port 4 bit 0.

Note. The * sign see 5.10.8 GPIO-1 and GPIO-4 with WDTO# / SUSLED / PLED multi-function

5.5 KBC Interface

SYMBOL	PIN	I/O	FUNCTION
GA20M	59	OUT_{12}	Gate A20 output. This pin is high after system reset. (KBC P21)
KBRST	60	OUT_{12}	Keyboard reset. This pin is high after system reset. (KBC P20)
KCLK	62	I/OD_{16ts}	Keyboard Clock.
GP27		I/OD_{16t}	General purpose I/O port 2 bit 7.
KDAT	63	I/OD_{16ts}	Keyboard Data.
GP26		I/OD_{16t}	General purpose I/O port 2 bit 6.
MCLK	65	I/OD_{16ts}	PS2 Mouse Clock.
GP25		I/OD_{16t}	General purpose I/O port 2 bit 5.
MDAT	66	I/OD_{16ts}	PS2 Mouse Data.
GP24		I/OD_{16t}	General purpose I/O port 2 bit 4.

5.6 Serial Flash Interface

SYMBOL	PIN	I/O	FUNCTION
SCE#	19	OUT_{12}	Serial Flash ROM interface chip select.
GP22		I/OD_{12t}	General purpose I/O port 2 bit 2.
SCK	2	OUT_{12}	Clock output for Serial Flash. (33MHz)
GP23		I/OD_{12t}	General purpose I/O port 2 bit 3.
SO	118	OUT_{8}	Transfer commands, address or data to Serial Flash. It is connected to SI of Serial Flash.
BEEP		OD_{8}	Beep function for hardware monitor. This pin is low after system reset.**(for H version only, C version is tri- state)**
SI	58	IN_{ts}	Receive data from Serial Flash. It is connected to SO of Serial Flash.
AUXFANIN1		I/O_{12ts}	0 to +3V amplitude fan tachometer input.

5.7 Hardware Monitor Interface

SYMBOL	PIN	I/O	FUNCTION
BEEP	118	OD_8	Beep function for hardware monitor. This pin is low after system reset. **(for H version only, C version is tri-state)**
SO		OUT_8	Transfer commands, address or data to Serial Flash. It is connected to SI of Serial Flash.
CASEOPEN#	76	IN_t	CASE OPEN detected. An active low level input from an external device when case is opened. This signal can be latched if pin VBAT is connect to battery, even W83627EHF/EHG is power off. This pin is VSS for W83627EF/EG.**Pull down is recommended if useless**. **(For H version only, C version is falling edge trigger only)**
VIN4	95	AIN	0V to 2.048V FSR Analog Inputs. (FSR: Full Scale Register)
VIN3	96	AIN	0V to 2.048V FSR Analog Inputs.
VIN2	97	AIN	0V to 2.048V FSR Analog Inputs.
VIN1	98	AIN	0V to 2.048V FSR Analog Inputs.
VIN0	99	AIN	0V to 2.048V FSR Analog Inputs.
CPUVCORE	100	AIN	0V to 2.048V FSR Analog Inputs.
VREF	101	AOUT	Reference Voltage (2.048V) for temperature maturation.
AUXTIN	102	AIN	Temperature sensor 3 inputs. It is used for temperature maturation.
CPUTIN	103	AIN	Temperature sensor 2 inputs. It is used for CPU temperature maturation.
SYSTIN	104	AIN	Temperature sensor 1 input. It is used for system temperature maturation.
OVT#	5	OD_{12}	Over temperature Shutdown Output. It indicated the temperature is over temperature limit.
HM_SMI#		OD_{12}	System Management Interrupt channel output. (Default after PCIRST)
VID5 VID4 VID3 VID2 VID1 VID0	105 106 107 108 109 110	I/O_{12}	VID input detect, also with output control.
AUXFANIN1	58	I/O_{12ts}	0V to +3.3V amplitude fan tachometer input.
SI		IN_{ts}	Receive data from Serial Flash. It is connected to SO of Serial Flash.

Hardware Monitor Interface, continued.

SYMBOL	PIN	I/O	FUNCTION
AUXFANIN0 CPUFANIN0 SYSFANIN	111 112 113	I/O_{12ts}	0V to +3.3V amplitude fan tachometer input.
CPUFANIN1	119	I/O_{12ts}	0V to +3.3V amplitude fan tachometer input. (Default)
MSI		IN_{cs}	MIDI serial data input.
GP21		I/OD_{12t}	General purpose I/O port 2 bit 1.
AUXFANOUT CPUFANOUT0 SYSFANOUT	7 115 116	AOUT/ OD_{12}	DC/PWM fan output control. CPUFANOUT0 & AUXFANOUT are default PWM Mode, CPUFANOUT1 & SYSFANOUT are default DC Mode. (For H version, while SYSFANOUT or CPUFANOUT0 be selected to PWM Mode, either of them can be open-drain or push-pull output. The controlled bits are CR24h bit[4:3]. Open-drain output is default.)
CPUFANOUT1	120	AOUT/ OUT_{12}	DC/PWM fan output control. CPUFANOUT0 & AUXFANOUT are default PWM Mode, CPUFANOUT1 & SYSFANOUT are default DC Mode.
MSO		OUT_{12}	MIDI serial data output.
GP20		I/OD_{12t}	General purpose I/O port 2 bit 0.

5.8 Game Port & MIDI Port

SYMBOL	PIN	I/O	FUNCTION
GPSA1	128	IN_{cs}	Active-low, Joystick I switch input 1. (Default)
GP10*		I/OD_{12cs}	General purpose I/O port 1 bit 0.
GPSB1	127	IN_{cs}	Active-low, Joystick II switch input 1. (Default)
GP11**		I/OD_{12cs}	General purpose I/O port 1 bit 1.
GPX1	126	I/OD_{12cs}	Joystick II timer pin. This pin connects to X positioning variable resistors for the Joystick. (Default)
GP12*			General purpose I/O port 1 bit 2.
GPX2	125	I/OD_{12cs}	Joystick II timer pin. This pin connects to X positioning variable resistors for the Joystick. (Default)
GP13**			General purpose I/O port 1 bit 3.

Game Port & MIDI Port, continued.

SYMBOL	PIN	I/O	FUNCTION
GPY2	124	I/OD_{12cs}	Joystick II timer pin. This pin connects to Y positioning variable resistors for the Joystick. (Default)
GP14*			General purpose I/O port 1 bit 4.
GPY1	123	I/OD_{12cs}	Joystick I timer pin. This pin connects to Y positioning variable resistors for the Joystick. (Default)
GP15**			General purpose I/O port 1 bit 5.
GPSB2	122	IN_{cs}	Active-low, Joystick II switch input 2. (Default)
GP16*		I/OD_{12cs}	General purpose I/O port 1 bit 6.
GPSA2	121	IN_{cs}	Active-low, Joystick I switch input 2. (Default)
GP17**		I/OD_{12cs}	General purpose I/O port 1 bit 7.
MSI	119	IN_{cs}	MIDI serial data input. (Default)
CPUFANIN1		I/O_{12ts}	0V to +3.3V amplitude fan tachometer input.
GP21		I/OD_{12t}	General purpose I/O port 2 bit 1.
MSO	120	OUT_{12}	MIDI serial data output. (Default)
CPUFANOUT1		AOUT/ OUT_{12}	DC/PWM fan output control. CPUFANOUT0 & AUXFANOUT are default PWM Mode, CPUFANOUT1 & SYSFANOUT are default DC Mode.
GP20		I/OD_{12t}	General purpose I/O port 2 bit 0.

Note. The * sign see 5.10.8 GPIO-1 and GPIO-4 with WDTO# / SUSLED / PLED multi-function

5.9 ACPI Interface

SYMBOL	PIN	I/O	FUNCTION
PSIN	68	IN_{td}	Panel Switch Input. This pin is high active with an internal pull down resistor.
GP56		I/OD_{12t}	General purpose I/O port 5 bit 6.
PSOUT#	67	OD_{12}	Panel Switch Output. This signal is used for Wake-Up system from $S5_{cold}$ state. This pin is pulse output, active low.
GP57		I/OD_{12t}	General purpose I/O port 5 bit 7.
VBAT	74	PWR	+3.3V on-board battery for the digital circuitry.
RSTOUT0#	94	OD_{12}	Secondary LRESET# output 0.
RSTOUT1#	93	OUT_{12}	Secondary LRESET# output 1.
RSTOUT2#	90	OUT_{12}	Secondary LRESET# output 2.
GP32		I/OD_{12t}	General purpose I/O port 3 bit 2.
SCL		IN_{ts}	Serial Bus clock.
RSTOUT3#	89	OUT_{12}	Secondary LRESET# output 3.
GP33		I/OD_{12t}	General purpose I/O port 3 bit 3.
SDA		I/OD_{12ts}	Serial bus bi-directional Data.
RSTOUT4#	88	OUT_{12}	Secondary LRESET# output 4.
GP34		I/OD_{12t}	General purpose I/O port 3 bit 4.

5.10 General Purpose I/O Port

5.10.1 GPIO Power Source

SYMBOL	POWER SOURCE
GPIO port 1	VCC
GPIO port 2 (Bit0-3)	VCC
GPIO port 2 (Bit4-7)	VSB
GPIO port 3	VSB
GPIO port 4	VSB
GPIO port 5	VSB
GPIO port 6	VCC

5.10.2 GPIO-1 Interface

see 5.8 Game Port