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W83627HF/F
W83627HG/G

Winbond LPC I/O

Date： 2006/06/09　Revision： 2.27

W83627HF/F, W83627HG/G Data Sheet Revision History

VERSION	DATE	PAGE	DESCRIPTION
0.50	09/25/98	n.a.	Not released For internal use only
0.51	11/10/98	88-93,102,105, 139,151,153	First published. Explanation of H/W Monitor function andregister correction.
0.52	01/11/99	90-93;113-115	Pinout and register correction.
0.53	07/26/99	90,91,113-115, 119-123,133,136, 137,140,141	Typo and data correction. H/W Monitor register explanation.
1.0	11/14/00	All	New composition.
2.0	11/01/02	All	New composition.
2.1	03/07/03	90	Correct SUSLED mode register
2.2	04/09/03	1. P74 ~ P76 2. P3,P90,P111 3. P6~P7	1. Add Section 4.1 Plug and Pla Configuration. 2. Remove Phoenix MultiKey related. 3. Add Block Digram
2.21	02/03/04	121	Add the top marking of W83627HG and W83627G.
2.22	05/28/04	12,13,21,23,39,4 5,46,82,93,94,98 ~ 100	Typo and data correction.
2.23	07/07/04	20,24,84,100	Data correction.
2.24	10/28/04	48,79	Data correction.
2.25	11/02/04	98	Data correction.
2.26	01/11/05	24, 76,77,120	Add part No.to Section 13 Ordering Instruction and data correction.
2.27	06/09/06	8 ~ 11	Add pin configuration of W83627G & W83627HG

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1. GENERAL DESCRIPTION

The W83627HF and W83627F are evolving product from Winbond's most popular I/O family. They feature a whole new interface, namely LPC（Low Pin Count）interface, which will be supported in the next generation Intel chip-set. This interface as its name suggests is to provide an economical implementation of I/O's interface with lower pin count and still maintains equivalent performance as its ISA interface counterpart. Approximately 40 pin counts are saved in LPC I/O comparing to ISA implementation. With this additional freedom, we can implement more devices on a single chip as demonstrated in W83627F/HF's integration of Game Port and MIDI Port.It is fully transparent in terms of software which means no BIOS or device driver update is needed except chip-specific configuration.

The disk drive adapter functions of W83627F/HF include a floppy disk drive controller compatible with the industry standard 82077/ 765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. The wide range of functions integrated onto the W83627F/HF greatly reduces the number of components required for interfacing with floppy disk drives. The W83627F/HF supports four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s,1 Mb/s, and 2 Mb/s.

The W83627F/HF provides two high-speed serial communication ports（UARTs）, one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. Both UARTs provide legacy speed with baud rate up to 115.2k bps and also advanced speed with baud rates of 230k, 460k, or 921k bps which support higher speed modems. In addition, the W83627F/HF provides IR functions： IrDA 1.0 （SIR for 1.152K bps）and TV remote IR （Consumer IR, supporting NEC, RC-5, extended RC-5, and RECS-80 protocols）.

The W83627F/HF supports one PC-compatible printer port（SPP）, Bi-directional Printer port（BPP） and also Enhanced Parallel Port （EPP） and Extended Capabilities Port（ECP）. Through the printer port interface pins, also available are： Extension FDD Mode and Extension 2FDD Mode allowing one or two external floppy disk drives to be connected.

The configuration registers support mode selection, function enable/disable, and power down function selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature demand of Windows 95/98™, which makes system resource allocation more efficient than ever.

The W83627F/HF provides functions that complies with ACPI （*Advanced Configuration and Power Interface*）, which includes support of legacy and ACPI power management through PME# or PSOUT# function pins. For OnNow keyboard Wake-Up, OnNow mouse Wake-Up, and OnNow CIR Wake-Up. The W83627F/HF also has auto power management to reduce the power consumption.

The keyboard controller is based on 8042 compatible instruction set with a 2K Byte programmable ROM and a 256-Byte RAM bank. Keyboard BIOS firmware are available with optional AMIKEY™-2, Phoenix MultiKey/42™, or customer code.

The W83627F/HF provides a set of flexible I/O control functions to the system designer through a set of General Purpose I/O ports. These GPIO ports may serve as simple I/O or may be individually configured to provide a predefined alternate function. General Purpose Port 1 is designed to be functional even in power down mode（VCC is off）.

The W83627F/HF is made to fully comply with Microsoft PC98 and PC99 Hardware Design Guide. Moreover W83627F/HF is made to meet the specification of PC98/PC99's requirement in the power management： ACPI and DPM （Device Power Management）.

The W83627F/HF contains a game port and a MIDI port. The game port is designed to support 2 joysticks and can be applied to all standard PC game control devices, They are very important for a entertainment or consumer computer.

Only the W83627HF support hardware status monitoring for personal computers. It can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system to work stably and properly.

2. FEATURES

General

- Meet LPC Spec. 1.0
- Support LDRQ#（LPC DMA）, SERIRQ （serial IRQ）
- Include all the features of Winbond I/O W83977TF and W83977EF
- Integrate Hardware Monitor functions
- Compliant with Microsoft PC98/PC99 Hardware Design Guide
- Support DPM （Device Power Management）, ACPI
- Programmable configuration settings
- Single 24 or 48 MHz clock input

FDC

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- Support vertical recording format
- DMA enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detects all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD write enable signal （write data signal was forced to be inactive）
- Support up to four 3.5-inch or 5.25-inch floppy disk drives
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support 3-mode FDD, and its Win95/98 driver

UART

- Two high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs
- MIDI compatible
- Fully programmable serial-interface characteristics：
  - — 5, 6, 7 or 8-bit characters
  - — Even, odd or no parity bit generation/detection
  - — 1, 1.5 or 2 stop bits generation

- Internal diagnostic capabilities：
  - — Loop-back controls for communications link fault isolation
  - — Break, parity, overrun, framing error simulation
- Programmable baud generator allows division of 1.8461 MHz and 24 MHz by 1 to （2^{16}-1）
- Maximum baud rate up to 921k bps for 14.769 MHz and 1.5M bps for 24 MHz

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps

Parallel Port

- Compatible with IBM parallel port
- Support PS/2 compatible bi-directional parallel port
- Support Enhanced Parallel Port（EPP）– Compatible with IEEE 1284 specification
- Support Extended Capabilities Port（ECP）– Compatible with IEEE 1284 specification
- Extension FDD mode supports disk drive B; and Extension 2FDD mode supports disk drives A and B through parallel port
- Enhanced printer port back-drive current protection

Keyboard Controller

- 8042 based with optional F/W from AMIKKEY^{TM}-2,or customer code with 2K bytes of programmable ROM, and 256 bytes of RAM
- Asynchronous Access to Two Data Registers and One status Register
- Software compatibility with the 8042
- Support PS/2 mouse
- Support port 92
- Support both interrupt and polling modes
- Fast Gate A20 and Hardware Keyboard Reset
- 8 Bit Timer/ Counter
- Support binary and BCD arithmetic
- 6 MHz, 8 MHz, 12 MHz, or 16 MHz operating frequency

Game Port

- Support two separate Joysticks
- Support every Joystick two axis （X,Y） and two button （A,B） controllers

MIDI Port

- The baud rate is 31.25 Kbaud
- 16-byte input FIFO
- 16-byte output FIFO

General Purpose I/O Ports

- 22 programmable general purpose I/O ports
- General purpose I/O ports can serve as simple I/O ports, interrupt steering inputs, watch dog timer output, power LED output, infrared I/O pins, KBC control I/O pins, suspend LED output, RSMRST# signal, PWROK signal, Beep output
- Functional in power down mode （GP1 only）

OnNow Functions

- Keyboard Wake-Up by programmable keys
- Mouse Wake-Up by programmable buttons
- CIR Wake-Up by programmable keys
- On Now Wake-Up from all of the ACPI sleeping states （S1-S5）

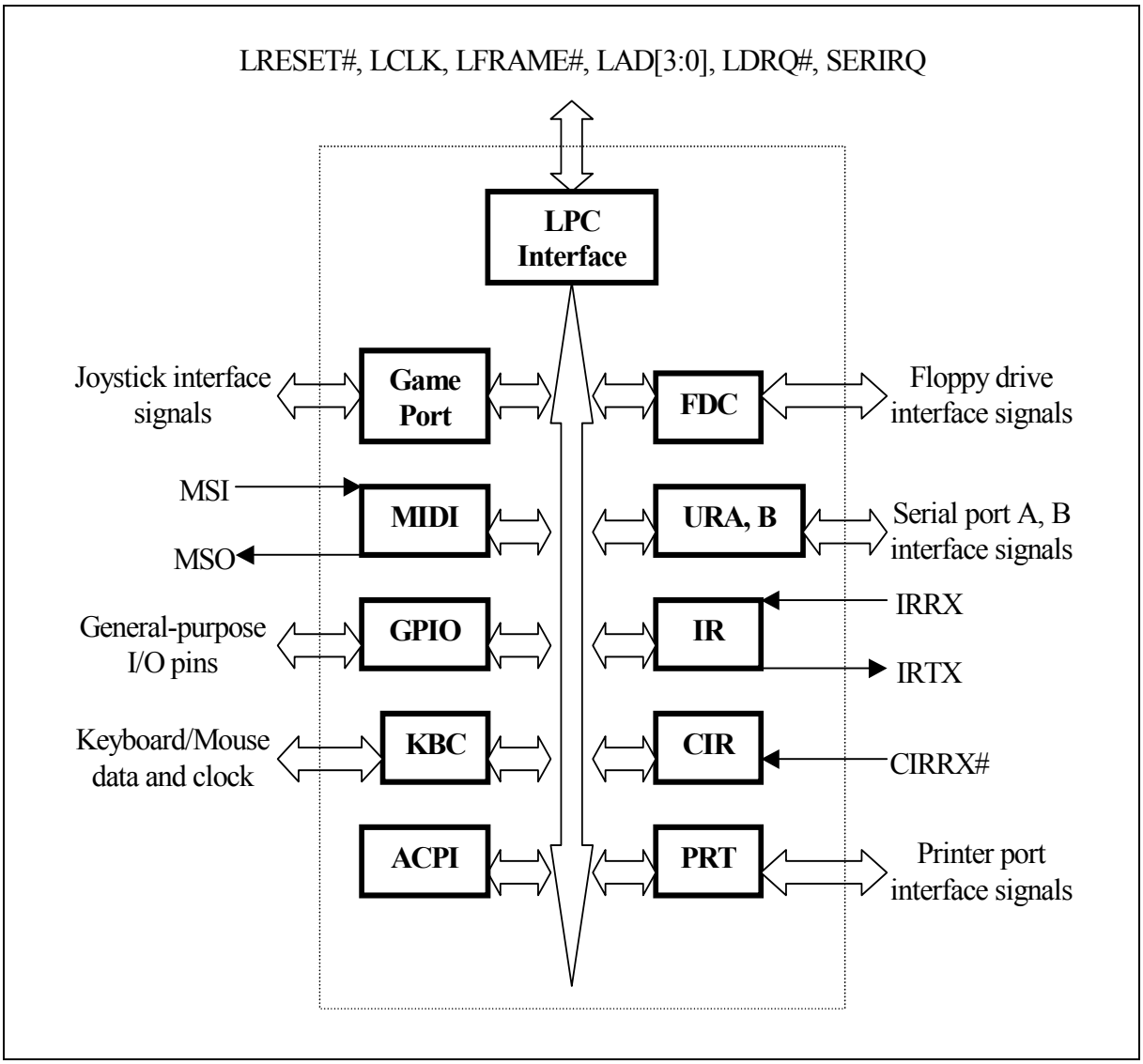
Hardware Monitor Functions （ Only for W83627HF）

- 5 VID input pins for CPU Vcore identification
- 3 thermal inputs from optionally remote thermistors or 2N3904 transistors or Pentium™ II （Deschutes） thermal diode output
- 7 positive voltage inputs （typical for +12V, -12V, +5V, -5V, +3.3V, VcoreA, VcoreB）
- 2 intrinsic voltage monitoring （typical for Vbat, +5VSB）
- 3 fan speed monitoring inputs
- 2 fan speed control
- Build in Case open detection circuit
- WATCHDOG comparison of all monitored values
- Programmable hysteresis and setting points for all monitored items
- Over temperature indicate output
- Automatic Power On voltage detection Beep
- Issue SMI#, IRQ, OVT# to activate system protection
- Intel LDCM™ / Acer ADM™ compatible

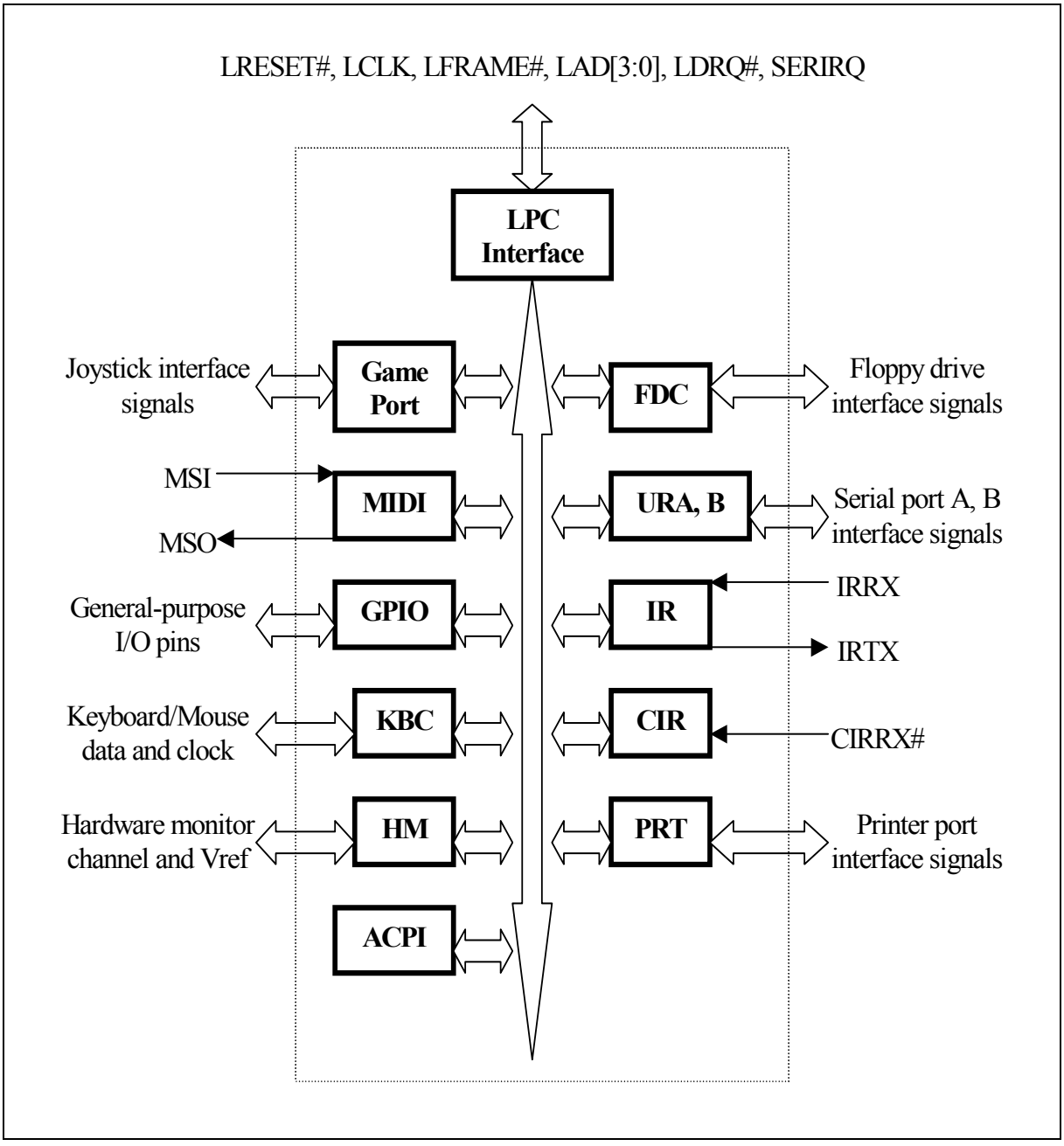
Package

- 128-pin PQFP

3. BLOCK DIAGRAM FOR W83627F

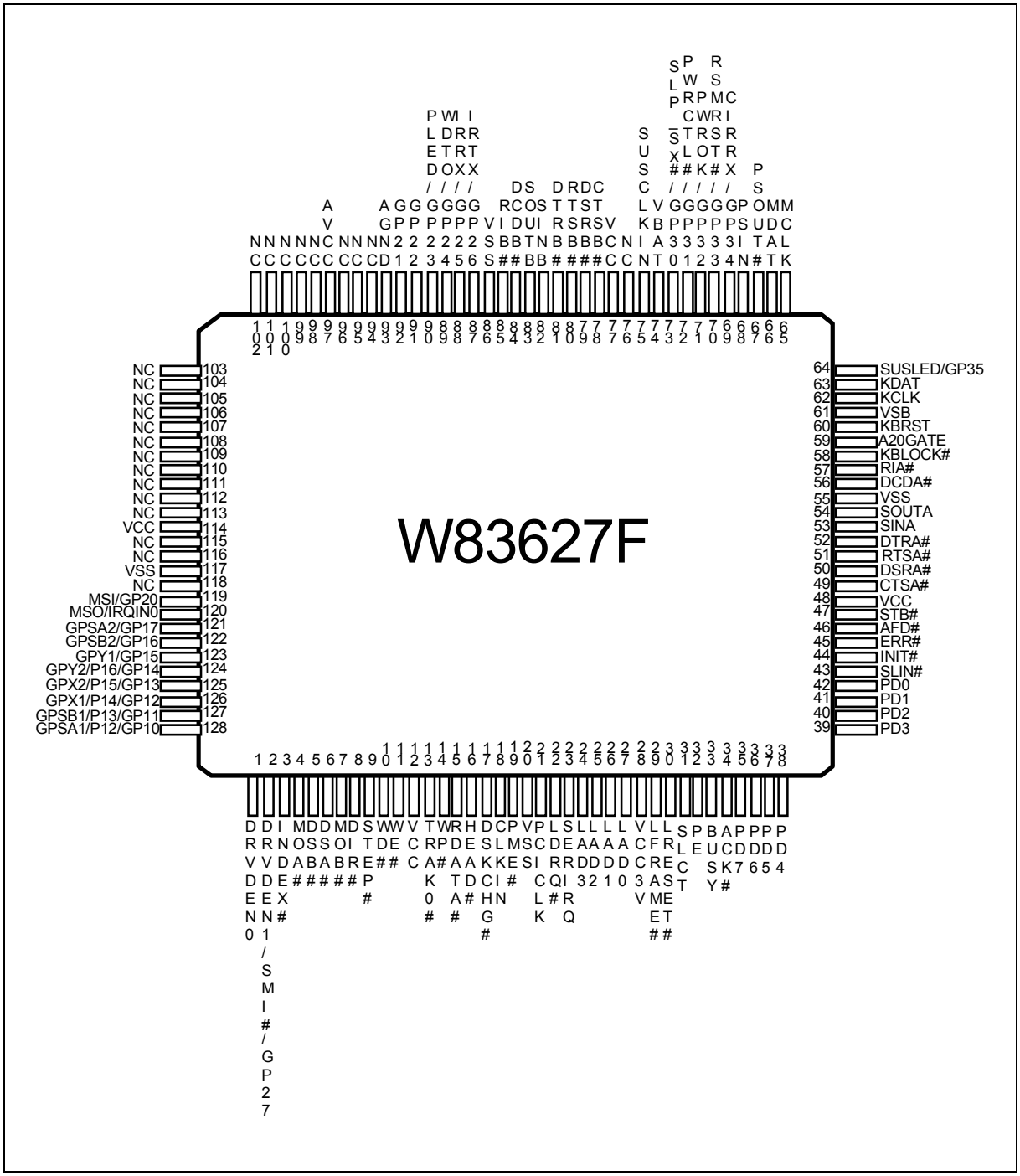


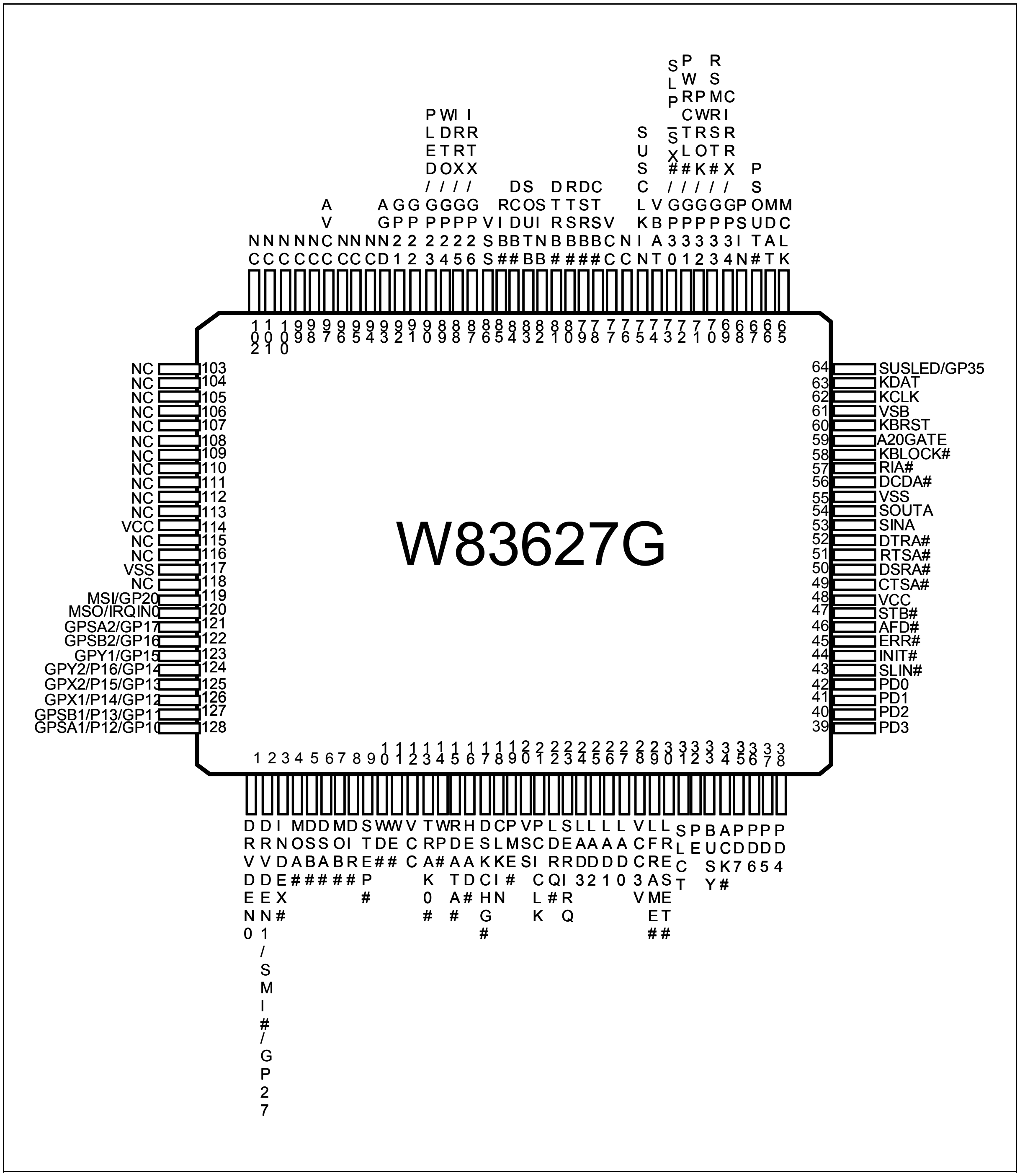
4. BLOCK DIAGRAM FOR W83627HF



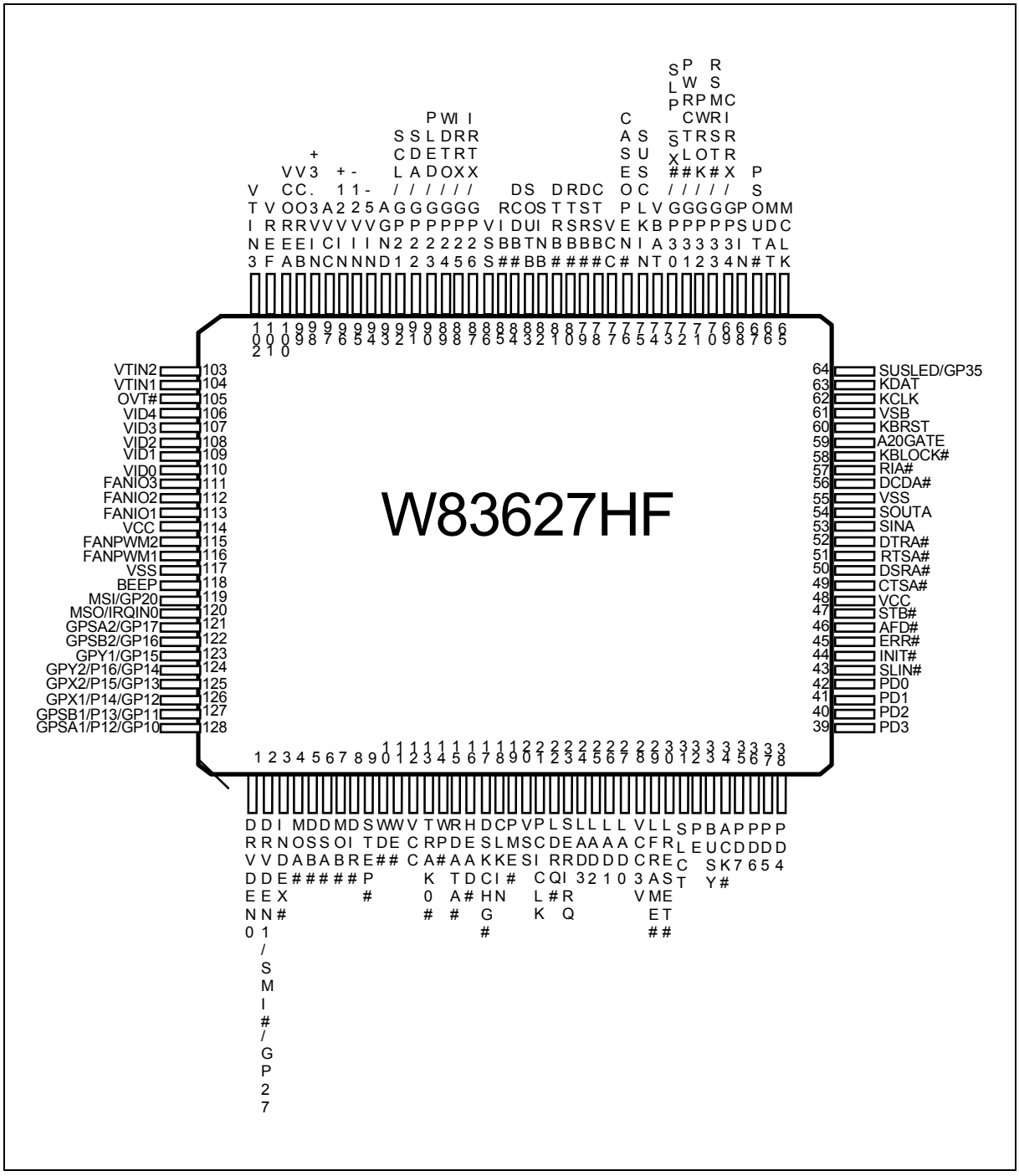
5. PIN CONFIGURATION

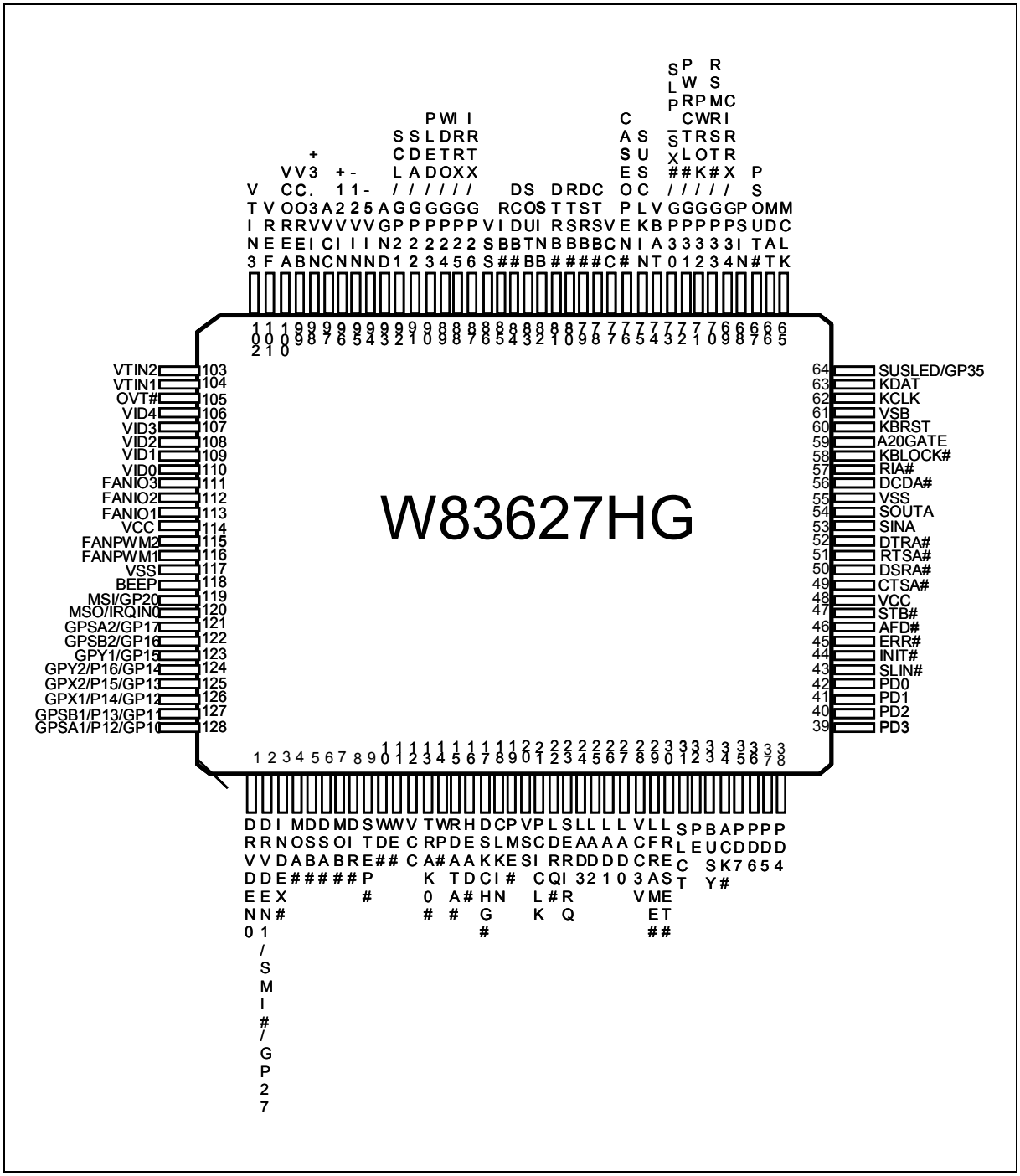
Pin configuration of W83627F and W83627G




W83627G
NC 103
NC 104
NC 105
NC 106
NC 107
NC 108
NC 109
NC 110
NC 111
NC 112
NC 113
VCC 114
NC 115
NC 116
VSS 117
NC 118
MSI/GP20 119
MSO/IRQIN0 120
GPSA2/GP17 121
GPSB2/GP16 122
GPY1/GP15 123
GPY2/P16/GP14 124
GPX2/P15/GP13 125
GPX1/P14/GP12 126
GPSB1/P13/GP11 127
GPSA1/P12/GP10 128
64 SUSLED/GP35
63 KDAT
62 KCLK
61 VSB
60 KBRST
59 A20GATE
58 KBLOCK#
57 RIA#
56 DCDA#
55 VSS
54 SOUTA
53 SINA
52 DTRA#
51 RTSA#
50 DSRA#
49 CTSA#
48 VCC
47 STB#
46 AFD#
45 ERR#
44 INIT#
43 SLIN#
42 PD0
41 PD1
40 PD2
39 PD3

PIN CONFIGURATION of W83627HF and W83627HG




W83627HG
VTIN2 103
VTIN1 104
OVT# 105
VID4 106
VID3 107
VID2 108
VID1 109
VID0 110
FANIO3 111
FANIO2 112
FANIO1 113
VCC 114
FANPWM2 115
FANPWM1 116
VSS 117
BEEP 118
MSI/GP20 119
MSO/IRQIN0 120
GPSA2/GP17 121
GPSB2/GP16 122
GPY1/GP15 123
GPY2/P16/GP14 124
GPX2/P15/GP13 125
GPX1/P14/GP12 126
GPSB1/P13/GP11 127
GPSA1/P12/GP10 128
64 SUSLED/GP35
63 KDAT
62 KCLK
61 VSB
60 KBRST
59 A20GATE
58 KBLOCK#
57 RIA#
56 DCDA#
55 VSS
54 SOUTA
53 SINA
52 DTRA#
51 RTSA#
50 DSRA#
49 CTSA#
48 VCC
47 STB#
46 AFD#
45 ERR#
44 INIT#
43 SLIN#
42 PD0
41 PD1
40 PD2
39 PD3

6. PIN DESCRIPTION

TYPE	DESCRIPTION
I/O_{8t}	TTL level bi-directional pin with 8mA source-sink capability
I/O_{12t}	TTL level bi-directional pin with 12mA source-sink capability
I/O_{24t}	TTL level bi-directional pin with 24 mA source-sink capability
I/O_{12tp3}	3.3V TTL level bi-directional pin with 12mA source-sink capability
I/O_{12ts}	TTL level Schmitt-trigger bi-directional pin with 12mA source-sink capability
I/O_{24ts}	TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability
I/O_{24tsp3}	3.3V TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability
I/OD_{12t}	TTL level bi-directional pin and open-drain output with 12mA sink capability
I/OD_{24t}	TTL level bi-directional pin and open-drain output with 24mA sink capability
I/OD_{12ts}	TTL level Schmitt-trigger bi-directional pin and open-drain output with 12mA sink capability
I/OD_{16ts}	TTL level Schmitt-trigger bi-directional pin and open-drain output with 16mA sink capability
I/OD_{24ts}	TTL level Schmitt-trigger bi-directional pin and open-drain output with 24mA sink capability
I/OD_{12cs}	CMOS level Schmitt-trigger bi-directional pin and open-drain output with 12mA sink capability
I/OD_{16cs}	CMOS level Schmitt-trigger bi-directional pin and open-drain output with 16mA sink capability
I/OD_{12csd}	CMOS level Schmitt-trigger bi-directional pin with internal pull down resistor and open-drain output with 12mA sink capability
I/OD_{12csu}	CMOS level Schmitt-trigger bi-directional pin with internal pull up resistor and open-drain output with 12mA sink capability
O_4	Output pin with 4 mA source-sink capability
O_8	Output pin with 8 mA source-sink capability
O_{12}	Output pin with 12 mA source-sink capability
O_{16}	Output pin with 16 mA source-sink capability
O_{24}	Output pin with 24 mA source-sink capability
O_{12p3}	3.3V output pin with 12 mA source-sink capability
O_{24p3}	3.3V output pin with 24 mA source-sink capability
OD_{12}	Open-drain output pin with 12 mA sink capability
OD24	Open-drain output pin with 24 mA sink capability
OD12p3	3.3V open-drain output pin with 12 mA sink capability

PIN DESCRIPTION, continued.

TYPE	DESCRIPTION
IN_t	TTL level input pin
IN_{tp3}	3.3V TTL level input pin
IN_{td}	TTL level input pin with internal pull down resistor
IN_{tu}	TTL level input pin with internal pull up resistor
IN_{ts}	TTL level Schmitt-trigger input pin
IN_{tsp3}	3.3V TTL level Schmitt-trigger input pin
IN_c	CMOS level input pin
IN_{cd}	CMOS level input pin with internal pull down resistor
IN_{cs}	CMOS level Schmitt-trigger input pin
IN_{csu}	CMOS level Schmitt-trigger input pin with internal pull up resistor

Note： Please refer to Section 11.2 DC CHARACTERISTICS for details.

6.1 LPC Interface

SYMBOL	PIN	I/O	FUNCTION
CLKIN	18	IN_{t3}	System clock input. According to the input frequency 24MHz or 48MHz, it is selectable through register. Default is 24MHz input.
PME#	19	OD_{12p3}	Generated PME event.
PCICLK	21	IN_{tsp3}	PCI clock input.
LDRQ#	22	O_{12p3}	Encoded DMA Request signal.
SERIRQ	23	I/O_{12tp3}	Serial IRQ input/Output.
LAD[3：0]	24-27	I/O_{12tp3}	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
LFRAME#	29	IN_{tsp3}	Indicates start of a new cycle or termination of a broken cycle.
LRESET#	30	IN_{tsp3}	Reset signal. It can connect to PCIRST# signal on the host.
SUSCLKIN	75	IN_{tsp3}	32khz clock input, for CIR only.

6.2 FDC Interface

SYMBOL	PIN	I/O	FUNCTION
DRVDEN0	1	OD_{24}	Drive Density Select bit 0.
DRVDEN1 SMI# IRQIN1 GP27	2	OD12 OD12 INt I/OD12t	Drive Density Select bit 1.（Default） System Management Interrupt Interrupt channel input. General purpose I/O port 2 bit 7.
INDEX#	3	IN_{csu}	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin is pulled up internally by a 500 ohm resistor. The resistor can be disabled by bit 7 of LD0-CRF0（FIPURDWN）.
MOA#	4	OD_{24}	Motor A On. When set to 0, this pin enables disk drive 0.
DSB# FANIN3	5	OD_{24} I/O_{24ts}	Drive Select B. When set to 0, this pin enables disk drive B. 0V to +5V amplitude fan tachometer input
DSA#	6	OD_{24}	Drive Select A. When set to 0, this pin enables disk drive A.
MOB# FANPWM3	7	OD_{24} OD_{24}	Motor B On. When set to 0, this pin enables disk drive 1. Fan speed control. Use the Pulse Width Modulation（PWM）technical knowledge to control the Fan's RPM.
DIR#	8	OD_{24}	Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
STEP#	9	OD_{24}	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
WD#	10	OD_{24}	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
WE#	11	OD_{24}	Write enable. An open drain output.
TRACK0#	13	IN_{csu}	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track. This input pin is pulled up internally by a 1 K ohm resistor.The resistor can be disabled by bit 7 of L0-CRF0（FIPURDWN）.
WP#	14	IN_{csu}	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin is pulled up internally by a 1 K ohm resistor. The resistor can be disabled by bit 7 of L0-CRF0 （FIPURDWN）.

FDC Interface, continued.

SYMBOL	PIN	I/O	FUNCTION
RDATA#	15	IN_{csu}	The read data input signal from the FDD. This input pin is pulled up internally by a 1 K ohm resistor. The resistor can be disabled by bit 7 of L0-CRF0 （FIPURDWN）.
HEAD#	16	OD_{24}	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
DSKCHG#	17	IN_{csu}	Diskette change. This signal is active low at power on and whenever the diskette is removed. This input pin is pulled up internally by a 1 K ohm resistor. The resistor can be disabled by bit 7 of L0-CRF0 （FIPURDWN）.

6.3 Multi-Mode Parallel Port

The following pins have alternate functions (Printer Mode and Extension FDD Mode), which are selected by CR28 and LD1-CRF0 setting.

SYMBOL	PIN	I/O	FUNCTION
SLCT	31	IN_{ts}	PRINTER MODE： An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
WE2#		OD_{12}	EXTENSION FDD MODE： This pin is for Extension FDD B; its function is the same as the WE# pin of FDC. EXTENSION 2FDD MODE： This pin is for Extension FDD A and B; its function is the same as the WE# pin of FDC.
PE	32	IN_{ts}	PRINTER MODE： An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
WD2#		OD_{12}	EXTENSION FDD MODE： This pin is for Extension FDD B; its function is the same as the WD# pin of FDC. EXTENSION 2FDD MODE： This pin is for Extension FDD A and B; its function is the same as the WD# pin of FDC.

Multi-Mode Parallel Port, continued.

SYMBOL	PIN	I/O	FUNCTION
BUSY	33	IN_{ts}	PRINTER MODE： An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
MOB2#		OD_{12}	EXTENSION FDD MODE： This pin is for Extension FDD B; its function is the same as the MOB# pin of FDC. EXTENSION 2FDD MODE： This pin is for Extension FDD A and B; its function is the same as the MOB# pin of FDC.
ACK#	34	IN_{ts}	PRINTER MODE： An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DSB2#		OD_{12}	EXTENSION FDD MODE： This pin is for the Extension FDD B; its functions are the same as the DSB# pin of FDC. EXTENSION 2FDD MODE： This pin is for Extension FDD A and B; its function is the same as the DSB# pin of FDC.
PD7	35	I/O_{12ts}	PRINTER MODE： PD7 Parallel port data bus bit 7. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DSA2#		OD_{12}	EXTENSION FDD MODE： This pin is a tri-state output. EXTENSION 2FDD MODE： This pin is for Extension FDD A; its function is the same as the DSA# pin of FDC.

Multi-Mode Parallel Port, continued.

SYMBOL	PIN	I/O	FUNCTION
PD6	36	I/O_{12ts}	PRINTER MODE： PD6 Parallel port data bus bit 6. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
MOA2#		OD_{12}	EXTENSION FDD MODE： This pin is a tri-state output. EXTENSION. 2FDD MODE： MOA2# This pin is for Extension FDD A; its function is the same as the MOA# pin of FDC.
PD5	37	I/O_{12ts}	PRINTER MODE： PD5 Parallel port data bus bit 5. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE： This pin is a tri-state output. EXTENSION 2FDD MODE： This pin is a tri-state output.
PD4	38	I/O_{12ts}	PRINTER MODE： PD4 Parallel port data bus bit 4. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DSKCHG2#		IN_{ts}	EXTENSION FDD MODE： This pin is for Extension FDD B; the function of this pin is the same as the DSKCHG# pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE： This pin is for Extension FDD A and B; this function of this pin is the same as the DSKCHG# pin of FDC. It is pulled high internally.
PD3	39	I/O_{12ts}	PRINTER MODE： PD3 Parallel port data bus bit 3. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
RDATA2#		IN_{ts}	EXTENSION FDD MODE： RDATA2# This pin is for Extension FDD B; its function is the same as the RDATA# pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE： RDATA2# This pin is for Extension FDD A and B; its function is the same as the RDATA# pin of FDC. It is pulled high internally.

Multi-Mode Parallel Port, continued.

SYMBOL	PIN	I/O	FUNCTION
PD2	40	I/O_{12ts}	PRINTER MODE： PD2 Parallel port data bus bit 2. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
WP2#		IN_{ts}	EXTENSION FDD MODE： WP2# This pin is for Extension FDD B; its function is the same as the WP# pin of FDC. It is pulled high internally. EXTENSION. 2FDD MODE： WP2# This pin is for Extension FDD A and B; its function is the same as the WP# pin of FDC. It is pulled high internally.
PD1	41	I/O_{12ts}	PRINTER MODE： PD1 Parallel port data bus bit 1. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
TRAK02#		IN_{ts}	EXTENSION FDD MODE： TRAK02# This pin is for Extension FDD B; its function is the same as the TRAK0# pin of FDC. It is pulled high internally. EXTENSION. 2FDD MODE： TRAK02# This pin is for Extension FDD A and B; its function is the same as the TRAK0# pin of FDC. It is pulled high internally.
PD0	42	I/O_{12ts}	PRINTER MODE： PD0 Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
INDEX2#		IN_{ts}	EXTENSION FDD MODE： This pin is for Extension FDD B; its function is the same as the INDEX# pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE： This pin is for Extension FDD A and B; its function is the same as the INDEX# pin of FDC. It is pulled high internally.

Multi-Mode Parallel Port, continued.

SYMBOL	PIN	I/O	FUNCTION
SLIN#	43	OD_{12}	PRINTER MODE： SLIN# Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
STEP2#		OD_{12}	EXTENSION FDD MODE： This pin is for Extension FDD B; its function is the same as the STEP# pin of FDC. EXTENSION 2FDD MODE： This pin is for Extension FDD A and B; its function is the same as the STEP# pin of FDC.
INIT#	44	OD_{12}	PRINTER MODE： Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DIR2#		OD_{12}	EXTENSION FDD MODE： This pin is for Extension FDD B; its function is the same as the DIR# pin of FDC. EXTENSION 2FDD MODE： This pin is for Extension FDD A and B; its function is the same as the DIR# pin of FDC.
ERR#	45	IN_{ts}	PRINTER MODE： An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
HEAD2#		OD_{12}	EXTENSION FDD MODE： This pin is for Extension FDD B; its function is the same as the HEAD# pin of FDC. EXTENSION 2FDD MODE： This pin is for Extension FDD A and B; its function is the same as the HEAD# pin of FDC.

Multi-Mode Parallel Port, continued.

SYMBOL	PIN	I/O	FUNCTION
AFD#	46	OD_{12}	PRINTER MODE： An active low output from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DRVDEN0		OD_{12}	EXTENSION FDD MODE： This pin is for Extension FDD B; its function is the same as the DRVDEN0 pin of FDC. EXTENSION 2FDD MODE： This pin is for Extension FDD A and B; its function is the same as the DRVDEN0 pin of FDC.
STB#	47	OD_{12}	PRINTER MODE： An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE： This pin is a tri-state output EXTENSION 2FDD MODE： This pin is a tri-state output.

6.4 Serial Port Interface

SYMBOL	PIN	I/O	FUNCTION
CTSA# CTSB#	49 78	IN_t	Clear To Send. It is the modem control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
DSRA# DSRB#	50 79	IN_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
RTSA#	51	O_{8C}	UART A Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
HEFRAS		IN_{cd}	During power-on reset, this pin is pulled down internally and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 （HEFRAS）. A 4.7 k ohm is recommended if intends to pull up. （select 4EH as configuration I/O port's address）
DTRA#	52	O_{8C}	UART B Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
PNPCVS#		IN_{cd}	During power-on reset, this pin is pulled down internally and is defined as PNPCVS# , which provides the power-on value for CR24 bit 0, A 4.7k ohm is recommended if intends to pull up.（This bit is used to clear the default value of FDC, UARTs, and LPT setting）
RTSB#	80	O_{8C}	UART B Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
DTRB#	81	O_{8C}	UART B Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
SINA SINB#	53 82	IN_t	Serial Input. It is used to receive serial data through the communication link.
SOUTA	54	O_{8C}	UART A Serial Output. It is used to transmit serial data out to the communication link.
PENKBC		IN_{cd}	During power-on reset, this pin is pulled down internally and is defined as PENKBC, which provides the power-on value for CR24 bit 2 （PENKBC）. A 4.7 k ohm resistor is recommended if intends to pull up. （ enable KBC）
SOUTB	83	O_{8C}	UART B Serial Output. During power-on reset, this pin is pulled down internally and is defined as PEN48, which provides the power-on value for CR24 bit 6 （EN48）. A 4.7 k ohm resistor is recommended if intends to pull up.
PEN48		IN_{cd}	
DCDA# DCDB#	56 84	IN_t	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
RIA# RIB#	57 85	IN_t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.