



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



**W83627UHG
NCT6627UD
NUVOTON LPC I/O**

Date: April 1st, 2010 Revision: 1.6

TABLE OF CONTENTS –

1.	GENERAL DESCRIPTION	1
2.	FEATURES	3
3.	BLOCK DIAGRAM	6
4.	PIN LAYOUT	7
5.	PIN DESCRIPTION.....	8
5.1	LPC Interface	9
5.2	FDC Interface.....	9
5.3	Multi-Mode Parallel Port.....	11
5.4	Serial Port & Infrared Port Interface.....	12
5.5	KBC Interface.....	17
5.6	Hardware Monitor Interface	18
5.7	PECI Interface.....	19
5.8	SST Interface	19
5.9	Advanced Configuration and Power Interface	19
5.10	General Purpose I/O Port	19
5.10.1	GPIO Power Source	19
5.10.2	GPIO-1 Interface	20
5.10.3	GPIO-2 Interface	20
5.10.4	GPIO-3 Interface	20
5.10.5	GPIO-4 Interface	20
5.10.6	GPIO-5 Interface	20
5.10.7	GPIO-6 Interface	21
5.10.8	WDTO# and SUSLED Pins	21
5.11	POWER PINS	21
6.	CONFIGURATION REGISTER ACCESS PROTOCOL	22
6.1	Configuration Sequence.....	24
6.1.1	Enter the Extended Function Mode.....	24
6.1.2	Configure the Configuration Registers	25
6.1.3	Exit the Extended Function Mode	25
6.1.4	Software Programming Example.....	25
7.	HARDWARE MONITOR	27
7.1	General Description	27
7.2	Access Interfaces.....	28
7.2.1	LPC Interface	28
7.2.2	I ² C Interface	30
7.3	Analog Inputs	32
7.3.1	Voltages Over 2.048 V or Less Than 0 V.....	33
7.3.2	Voltage Detection.....	34
7.3.3	Temperature Sensing.....	34
7.4	SST Command Summary	36
7.4.1	Command Summary	37
7.4.2	Combination Sensor Data Format.....	38

7.5	PECI.....	39
7.6	Fan Speed Measurement and Control.....	42
7.6.1	Fan Speed Measurement.....	42
7.6.2	Fan Speed Control.....	43
7.6.3	SMART FAN™ Control.....	44
7.7	Interrupt Detection.....	52
7.7.1	SMI# Interrupt Mode.....	52
7.7.2	OVT# Interrupt Mode.....	55
7.7.3	Caseopen Detection.....	55
7.7.4	BEEP Alarm Function.....	56
8.	HARDWARE MONITOR REGISTER SET.....	58
8.1	Address Port (Port x5h).....	58
8.2	Data Port (Port x6h).....	58
8.3	SYSFANOUT PWM Output Frequency Configuration Register - Index 00h (Bank 0).....	59
8.4	SYSFANOUT Output Value Select Register - Index 01h (Bank 0).....	59
8.5	CPUFANOUT PWM Output Frequency Configuration Register - Index 02h (Bank 0).....	60
8.6	CPUFANOUT Output Value Select Register - Index 03h (Bank 0).....	61
8.7	FAN Configuration Register I - Index 04h (Bank 0).....	61
8.8	SYSTIN Target Temperature Register/ SYSFANIN Target Speed Register - Index 05h (Bank 0).....	62
8.9	CPUTIN Target Temperature Register/ CPUFANIN Target Speed Register - Index 06h (Bank 0).....	62
8.10	Tolerance of Target Temperature or Target Speed Register - Index 07h (Bank 0).....	63
8.11	SYSFANOUT Stop Value Register - Index 08h (Bank 0).....	63
8.12	CPUFANOUT Stop Value Register - Index 09h (Bank 0).....	63
8.13	SYSFANOUT Start-up Value Register - Index 0Ah (Bank 0).....	64
8.14	CPUFANOUT Start-up Value Register - Index 0Bh (Bank 0).....	64
8.15	SYSFANOUT Stop Time Register - Index 0Ch (Bank 0).....	65
8.16	CPUFANOUT Stop Time Register - Index 0Dh (Bank 0).....	65
8.17	Fan Output Step Down Time Register - Index 0Eh (Bank 0).....	65
8.18	Fan Output Step Up Time Register - Index 0Fh (Bank 0).....	66
8.19	Reserved Registers - Index 10h (Bank 0).....	66
8.20	Reserved Registers - Index 11h (Bank 0).....	66
8.21	FAN Configuration Register II - Index 12h (Bank 0).....	66
8.22	Reserved Registers - Index 13h (Bank 0).....	67
8.23	Reserved Registers - Index 14h (Bank 0).....	67
8.24	Reserved Registers - Index 15h (Bank 0).....	67
8.25	Reserved Registers - Index 16h (Bank 0).....	67
8.26	Reserved Registers - Index 17h (Bank 0).....	67
8.27	OVT# Configuration Register - Index 18h (Bank 0).....	67
8.28	Reserved Registers - Index 19h ~ 1Fh (Bank 0).....	67
8.29	Value RAM — Index 20h ~ 3Fh (Bank 0).....	68
8.30	Configuration Register - Index 40h (Bank 0).....	69
8.31	Interrupt Status Register 1 - Index 41h (Bank 0).....	70

8.32	Interrupt Status Register 2 - Index 42h (Bank 0)	70
8.33	SMI# Mask Register 1 - Index 43h (Bank 0).....	71
8.34	SMI# Mask Register 2 - Index 44h (Bank 0).....	71
8.35	Reserved Register - Index 45h (Bank 0)	72
8.36	SMI# Mask Register 3 - Index 46h (Bank 0).....	72
8.37	Fan Divisor Register I - Index 47h (Bank 0).....	72
8.38	Serial Bus Address Register - Index 48h (Bank 0).....	72
8.39	CPUFANOUT monitor Temperature source select register - Index 49h (Bank 0).....	73
8.40	SYSFANOUT monitor Temperature source select register - Index 4Ah (Bank 0).....	73
8.41	Fan Divisor Register II - Index 4Bh (Bank 0)	74
8.42	SMI#/OVT# Control Register - Index 4Ch (Bank 0).....	75
8.43	FAN IN/OUT Control Register - Index 4Dh (Bank 0).....	75
8.44	Register 50h ~ 5Fh Bank Select Register - Index 4Eh (Bank 0)	77
8.45	Nuvoton Vendor ID Register - Index 4Fh (Bank 0).....	77
8.46	Reserved Register - Index 50h ~ 55h (Bank 0)	78
8.47	BEEP Control Register 1 - Index 56h (Bank 0).....	78
8.48	BEEP Control Register 2 - Index 57h (Bank 0).....	79
8.49	Chip ID - Index 58h (Bank 0)	79
8.50	Reserved Register - Index 59h (Bank 0)	79
8.51	Reserved Register - Index 5Ah ~ 5Ch (Bank 0)	80
8.52	VBAT Monitor Control Register - Index 5Dh (Bank 0).....	80
8.53	Critical Temperature enable register - Index 5Eh (Bank 0)	80
8.54	Reserved Register - Index 5Fh (Bank 0)	81
8.55	Reserved Registers - Index 60h (Bank 0).....	81
8.56	Reserved Registers - Index 61h (Bank 0).....	81
8.57	Reserved Registers - Index 62h (Bank 0).....	81
8.58	Reserved Registers - Index 63h (Bank 0).....	81
8.59	Reserved Registers - Index 64h (Bank 0).....	81
8.60	Reserved Registers - Index 65h (Bank 0).....	81
8.61	Reserved Registers - Index 66h (Bank 0).....	82
8.62	CPUFANOUT Maximum Output Value Register - Index 67h (Bank 0).....	82
8.63	CPUFANOUT Output Step Value Register - Index 68h (Bank 0).....	83
8.64	Reserved Registers - Index 69h (Bank 0).....	83
8.65	Reserved Registers - Index 6Ah (Bank 0)	83
8.66	SYSFANOUT Critical Temperature register - Index 6Bh (Bank 0).....	83
8.67	CPUFANOUT Critical Temperature register - Index 6Ch (Bank 0)	83
8.68	Reserved Registers - Index 6Dh (Bank 0)	83
8.69	Reserved Registers - Index 6Eh (Bank 0)	84
8.70	CPUTIN/PECI Temperature (High Byte) Register - Index 50h (Bank 1).....	84
8.71	CPUTIN/PECI Temperature (Low Byte) Register - Index 51h (Bank 1).....	84
8.72	CPUTIN Configuration Register - Index 52h (Bank 1).....	84
8.73	CPUTIN Hysteresis (High Byte) Register - Index 53h (Bank 1)	85
8.74	CPUTIN Hysteresis (Low Byte) Register - Index 54h (Bank 1).....	85
8.75	CPUTIN Over-temperature (High Byte) Register - Index 55h (Bank 1).....	85

8.76	CPUTIN Over-temperature (Low Byte) Register - Index 56h (Bank 1).....	86
8.77	SYSTIN/CPUTIN/PECI Temperature (High Byte) Register - Index 50h (Bank 2).....	86
8.78	SYSTIN/CPUTIN/PECI Temperature (Low Byte) Register – Index 51h (Bank 2).....	86
8.79	Reserved Registers – Index 52h (Bank 2).....	87
8.80	Reserved Registers – Index 53h (Bank 2).....	87
8.81	Reserved Registers – Index 54h (Bank 2).....	87
8.82	Reserved Registers – Index 55h (Bank 2).....	87
8.83	Reserved Registers – Index 56h (Bank 2).....	87
8.84	Interrupt Status Register 3 – Index 50h (Bank 4)	87
8.85	SMI# Mask Register 4 – Index 51h (Bank 4).....	87
8.86	Reserved Register - Index 52h (Bank 4)	88
8.87	BEEP Control Register 3 - Index 53h (Bank 4).....	88
8.88	SYSTIN Temperature Sensor Offset Register - Index 54h (Bank 4).....	89
8.89	CPUTIN Temperature Sensor Offset Register - Index 55h (Bank 4).....	89
8.90	Reserved Registers - Index 56h (Bank 4).....	89
8.91	Reserved Register - Index 57h-58h (Bank 4)	89
8.92	Real Time Hardware Status Register I - Index 59h (Bank 4)	89
8.93	Real Time Hardware Status Register II - Index 5Ah (Bank 4).....	90
8.94	Real Time Hardware Status Register III - Index 5Bh (Bank 4).....	91
8.95	Reserved Register - Index 5Ch - 5Fh (Bank 4)	91
8.96	Value RAM 2 — Index 50h-59h (Bank 5)	91
8.97	Reserved Register - Index 50h - 57h (Bank 6).....	92
9.	FLOPPY DISK CONTROLLER.....	93
9.1	FDC Functional Description	93
9.1.1	FIFO (Data).....	93
9.1.2	Data Separator.....	94
9.1.3	Write Precompensation	94
9.1.4	Perpendicular Recording Mode.....	94
9.1.5	FDC Core.....	94
9.1.6	FDC Commands	95
9.2	Register Descriptions.....	103
9.2.1	Status Register A (SA Register) (Read base address + 0)	103
9.2.2	Status Register B (SB Register) (Read base address + 1)	104
9.2.3	Digital Output Register (DO Register) (Write base address + 2).....	105
9.2.4	Tape Drive Register (TD Register) (Read base address + 3)	106
9.2.5	Main Status Register (MS Register) (Read base address + 4)	107
9.2.6	Data Rate Register (DR Register) (Write base address + 4).....	108
9.2.7	FIFO Register (R/W base address + 5).....	109
9.2.8	Digital Input Register (DI Register) (Read base address + 7)	112
9.2.9	Configuration Control Register (CC Register) (Write base address + 7).....	113
10.	UART PORT	115
10.1	Universal Asynchronous Receiver/Transmitter (UART A, B, C, D, E, F)	115
10.2	Register Address	115
10.2.1	UART Control Register (UCR) (Read/Write).....	115

10.2.2	UART Status Register (USR) (Read/Write)	118
10.2.3	Handshake Control Register (HCR) (Read/Write)	119
10.2.4	Handshake Status Register (HSR) (Read/Write)	119
10.2.5	This register is used to control the FIFO functions of the UART	120
10.2.6	Interrupt Status Register (ISR) (Read only)	121
10.2.7	Interrupt Control Register (ICR) (Read/Write)	122
11.	PARALLEL PORT	124
11.1	Printer Interface Logic	124
11.2	Enhanced Parallel Port (EPP)	124
11.2.1	Data Port (Data Swapper)	125
11.2.2	Printer Status Buffer	125
11.2.3	Printer Control Latch and Printer Control Swapper	126
11.2.4	EPP Address Port	126
11.2.5	EPP Data Port 0-3	127
11.2.7	EPP Operation	127
11.3	Extended Capabilities Parallel (ECP) Port	128
11.3.1	ECP Register and Bit Map	129
11.3.2	Data and ecpAFifo Port	130
11.3.3	Device Status Register (DSR)	130
11.3.4	Device Control Register (DCR)	130
11.3.5	CFIFO (Parallel Port Data FIFO) Mode = 010	131
11.3.6	ECPDFIFO (ECP Data FIFO) Mode = 011	131
11.3.7	TFIFO (Test FIFO Mode) Mode = 110	131
11.3.8	CNFGA (Configuration Register A) Mode = 111	131
11.3.9	CNFGB (Configuration Register B) Mode = 111	132
11.3.10	ECR (Extended Control Register) Mode = all	132
11.3.11	ECP Pin Descriptions	134
11.3.12	ECP Operation	135
11.3.13	DMA Transfers	136
11.3.14	Programmed I/O (NON-DMA) Mode	136
12.	KEYBOARD CONTROLLER	137
12.1	Output Buffer	137
12.2	Input Buffer	137
12.3	Status Register	138
12.4	Commands	138
12.5	Hardware GATEA20/Keyboard Reset Control Logic	140
12.5.1	KB Control Register (Logic Device 5, CR-F0)	140
12.5.2	Port 92 Control Register (Default Value = 0x24)	142
13.	POWER MANAGEMENT EVENT	143
13.1	Power Control Logic	143
13.1.1	PSON# Logic	144
13.1.2	AC Power Failure Resume	145
13.2	Wake Up the System by Keyboard and Mouse	146
13.2.1	Waken up by Keyboard events	146
13.2.2	Waken up by Mouse events	147

13.3	Resume Reset Logic.....	148
13.4	PWROK Generation.....	149
14.	SERIALIZED IRQ.....	151
14.1	Start Frame	151
14.2	IRQ/Data Frame.....	152
14.3	Stop Frame	153
15.	WATCHDOG TIMER.....	154
16.	GENERAL PURPOSE I/O.....	155
16.1	GPIO Architecture.....	155
16.2	Access Channels	155
17.	CONFIGURATION REGISTER.....	157
17.1	Chip (Global) Control Register.....	157
17.2	Logical Device 0 (FDC).....	165
17.3	Logical Device 1 (Parallel Port).....	169
17.4	Logical Device 2 (UART A).....	170
17.5	Logical Device 3 (UART B).....	171
17.6	Logical Device 5 (Keyboard Controller).....	172
17.7	Logical Device 6 (UART C).....	175
17.8	Logical Device 7 (GPIO3, GPIO4).....	176
17.9	Logical Device 8 (WDTO#, PLED, GPIO5, 6 & GPIO Base Address).....	178
17.10	Logical Device 9 (GPIO1, GPIO2 and SUSLED)	182
17.11	Logical Device A (ACPI)	184
17.12	Logical Device B (Hardware Monitor).....	192
17.13	Logical Device C (PECI, SST).....	193
17.14	Logical Device D (UART D).....	199
17.15	Logical Device E (UART E).....	199
17.16	Logical Device F (UART F).....	201
18.	SPECIFICATIONS	202
18.1	Absolute Maximum Ratings	202
18.2	DC CHARACTERISTICS.....	202
18.3	AC CHARACTERISTICS	207
18.3.1	Power On / Off Timing	207
18.3.2	AC Power Failure Resume Timing	208
18.3.3	Clock Input Timing.....	211
18.3.4	PECI and SST Timing.....	212
18.3.5	SMBus Timing	213
18.3.6	Floppy Disk Drive Timing.....	213
18.3.7	UART/Parallel Port	215
18.3.8	Parallel Port Mode Parameters.....	217
18.3.9	Parallel Port.....	218
18.3.10	KBC Timing Parameters	227
18.3.11	GPIO Timing Parameters.....	230
18.4	LRESET Timing	231
19.	TOP MARKING SPECIFICATION	232

20.	ORDER INFORMATION	233
21.	PACKAGE SPECIFICATION	234
22.	REVISION HISTORY	236
	APPENDIX – ABBREVIATIONS	239

新唐科技 NUVOTON
INTELLECTUAL PROPERTY

新唐科技 NUVOTON
INTELLECTUAL PROPERTY

List of Figures

Figure 3-1 W83627UHG Block Diagram	6
Figure 4-1 W83627UHG Pin Layout	7
Figure 6-1 Structure of the Configuration Register	22
Figure 6-2 Configuration Register	24
Figure 7-1 LPC Bus' Reads from / Writes to Internal Registers.....	29
Figure 7-2 Serial Bus Write to Internal Address Register Followed by the Data Byte	30
Figure 7-3 Serial Bus Read from Internal Address Register.....	31
Figure 7-4 Analog Inputs and Application Circuit of the W83627UHG	32
Figure 7-5 Monitoring Temperature from Thermistor	35
Figure 7-6 Monitoring Temperature from Thermal Diode (Voltage Mode).....	35
Figure 7-7 Monitoring Temperature from Thermal Diode	36
Figure 7-8 PECL Illustration	41
Figure 7-9 FANOUT and Corresponding Temperature Sensors in SMART FAN™ I	44
Figure 7-10 Mechanism of Thermal Cruise™ Mode (PWM Duty Cycle)	45
Figure 7-11 Mechanism of Thermal Cruise™ Mode (DC Output Voltage)	45
Figure 7-12 Mechanism of Fan Speed Cruise™ Mode.....	46
Figure 7-13 FANOUT and Corresponding Temperature Sensor in SMART FAN™ III	48
Figure 7-14 Setting of SMART FAN™ III.....	48
Figure 7-15 SMART FAN™ III Mechanism (Current Temp. > Target Temp. + Tol.).....	49
Figure 7-16 SMART FAN™ III Mechanism (Current Temp. < Target Temp. – Tol.).....	50
Figure 7-17 SMI Mode of Voltage and Fan Inputs	52
Figure 7-18 SMI Mode of SYSTIN I	53
Figure 7-19 SMI Mode of SYSTIN II	54
Figure 7-20 SMI Mode of CPUTIN	54
Figure 7-21 OVT# Modes of Temperature Inputs	55
Figure 7-22 Caseopen Mechanism	56
Figure 12-1 Keyboard and Mouse Interface.....	137
Figure 13-1 Power Control Mechanism.....	144
Figure 13-2 Power Sequence from S5 to S0, then back to S5.	145
Figure 13-3 Mechanism of Resume Reset Logic.....	148
Figure 14-1 Start Frame Timing with Source Sampled A Low Pulse on IRQ1	151
Figure 14-2 Stop Frame Timing with Host Using 17 SERIRQ Sampling Period.....	153

List of Tables

Table 6-1 Devices of I/O Base Address	23
Table 6-2 Chip (Global) Control Registers	26
Table 7-1 Temperature Data Format	34
Table 7-2 SST Command Summary	37
Table 7-3 Typical Temperature Values	38
Table 7-4 Fan Divisor Definition	42
Table 7-5 Divisor, RPM, and Count Relation	42
Table 7-6 Display Registers – at SMART FAN™ I Mode	46
Table 7-7 Relative Registers – at Thermal Cruise™ Mode	47
Table 7-8 Relative Registers – at Speed Cruise™ Mode	47
Table 7-9 Display Register – at SMART FAN™ III Mode	50
Table 7-10 Relative Register – at SMART FAN™ III Control Mode	51
Table 9-1 The Delays of the FIFO	93
Table 9-2 FDC Registers	103
Table 10-1 Register Summary for UART	117
Table 11-1 Pin Descriptions for SPP, EPP, and ECP Modes	124
Table 11-2 EPP Register Addresses	124
Table 11-3 Address and Bit Map for SPP and EPP Modes	125
Table 11-4 ECP Mode Description	128
Table 11-5 ECP Register Addresses	129
Table 11-6 Bit Map of the ECP Registers	129
Table 12-1 Bit Map of Status Register	138
Table 12-2 KBC Command Sets	138
Table 13-1 Bit Map of Logical Device A, CR[E4h], bits [6:5]	145
Table 13-2 Definitions of Mouse Wake-Up Events	148
Table 13-3 Timing and Voltage Parameters of RSMRST#	148
Table 14-1 SERIRQ Sampling Periods	152
Table 16-1 Relative Control Registers of GPIO 25, 26 and 27 that Support Wake-Up Function .	155
Table 16-2 GPIO Register Addresses	156

1. GENERAL DESCRIPTION

The W83627UHG is a member of Nuvoton's Super I/O product line. This family features the LPC (Low Pin Count) interface. This interface is more economical than its ISA counterpart because it has approximately forty pins fewer, yet still provides as great performance. In addition, the improvement allows even more efficient operation of software, BIOS and device drivers.

In addition to providing an LPC interface for I/O, the W83627UHG monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures. In terms of temperature monitoring, the W83627UHG adopts the Current Mode (dual current source) approach. The W83627UHG also supports the Smart Fan control system, including "SMART FAN™ I and SMART FAN™ III, which makes the system more stable and user-friendly.

The W83627UHG supports four -- 360K, 720K, 1.2M, 1.44M, or 2.88M -- disk drives and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s, 1 Mb/s, and 2 Mb/s. The disk drive adapter supports the functions of floppy disk drive controller (compatible with the industry standard 82077/ 765), data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. Such a wide range of functions integrated into one W83627UHG greatly reduces the number of required components to interface with floppy disk drives.

The W83627UHG provides six high-speed serial communication ports (UARTs), one of which provides IR functions IrDA 1.0 (SIR for 1.152K bps). Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem-control capability, and a processor interrupt system. All of the UARTs support legacy speeds up to 115.2K bps as well as higher baud rates of 230K, 460K, or 921K bps to support higher speed modems.

The W83627UHG supports the PC-compatible printer port (SPP), the bi-directional printer port (BPP), the enhanced parallel port (EPP) and the extended capabilities port (ECP).

The W83627UHG provides flexible I/O control functions through a set of 45 general purpose I/O (GPIO) ports. These GPIO ports may serve as simple I/O ports or may be individually configured to provide alternative functions.

The W83627UHG supports the SST (Simple Serial Transport) interface and Intel® PECEI (Platform Environment Control Interface).

The W83627UHG fully complies with the Microsoft© PC98 and PC99 Hardware Design Guide and meets the requirements of ACPI.

The configuration registers inside the W83627UHG support mode selection, function enable and disable, and power-down selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature in Windows 95/98/2000/XP™, making the allocation of the system resources more efficient than ever.

One special characteristic of the Super I/O product line is the separation of the power supply in normal operation from that in standby operation. Please pay attention to the layout of these two power supplies to avoid short circuits. Otherwise, the feature will not function.

There is NCT6627UD, which is exactly the same as W83627UHG, except the package dimension. NCT6627UD is thin package type, LQFP-128, 14mm x 14mm body size; W83627UHG is QFP-128, 14mm x 20mm body size.

2. FEATURES

General

- Meet LPC Spec. 1.0
- Support LDRQ# (LPC DMA), SERIRQ (Serialized IRQ)
- Integrated hardware monitor functions
- Compliant with Microsoft PC2000/PC2001 Hardware Design Guide
- Support DPM (Device Power Management), ACPI (Advanced Configuration and Power Interface)
- Programmable configuration settings
- Single 24- or 48-MHz clock input

FDC

- Variable write pre-compensation with track-selection capability
- Support vertical recording format
- DMA-enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detect all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD-write enable signal (write data signal forced to be inactive)
- Support 3.5-inch or 5.25-inch floppy disk drives
- Compatible with industry standard 82077
- 360K / 720K / 1.2M / 1.44M / 2.88M formats
- 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support 3-mode FDD and its Windows driver

UART

- W83627UHG supports Six high-speed, 16550-compatible UARTs with 16-byte send / receive FIFOs
- Fully programmable serial-interface characteristics:
 - 5, 6, 7 or 8-bit characters
 - Even, odd or no parity bit generation/detection
 - 1, 1.5 or 2 stop-bit generation
- Internal diagnostic capabilities:
 - Loop-back controls for communications link fault isolation
 - Break, parity, overrun, framing error simulation
- Programmable baud rate generator allows division of clock source by any value from 1 to ($2^{16}-1$)
- Maximum baud rate for clock source 14.769 MHz is up to 921K bps. The baud rate at 24 MHz is 1.5M bps.
- Support RS485 auto flow control of four UARTs. (UARTA, UARTC, UARTD and UARTE) --- for rev. E only

Parallel Port

- Compatible with IBM parallel port
- Support PS/2-compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) - Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) - Compatible with IEEE 1284 specification
- Enhanced printer port back-drive current protection

Keyboard Controller

- 8042-based keyboard controller
- Support Phoenix MultiKey/42™ firmware
- Asynchronous Access to two data registers and one status register
- Software-compatible with 8042
- Support PS/2 mouse
- Support port 92
- Support both interrupt and polling modes
- Fast Gate A20 and Hardware Keyboard Reset
- 8-bit timer / counter
- Support binary and BCD arithmetic
- 12MHz operating frequency

Hardware Monitor Functions

- Smart Fan control system, supporting the functions of SMART FAN™ I - “Thermal Cruise™” and “Fan Speed Cruise™” modes and SMART FAN™ III functions
- Programmable threshold temperature to speed fan fully while current temperature exceeds this temperature during Thermal Cruise™ mode
- Two thermal inputs from optionally-remote thermistors or thermal diode output
- Support Current Mode (dual current source) temperature sensing method
- Eight voltage inputs (CPUVCORE, VIN[0..2] and 5VCC, AVCC, 5VSB, VBAT)
- Two fan-speed monitoring inputs
- Two fan-speed controls
- Dual mode for fan control (PWM and DC)
- Built-in case open detection circuit
- Programmable hysteresis and setting points for all monitored items
- Over-temperature indicator output
- Issue SMI#, OVT# to activate system protection
- Nuvoton Hardware Doctor™ Support

- Provide I²C interface to read / write registers

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps

General Purpose I/O Ports

- 45 programmable general purpose I/O ports
- GP25, GP26 and GP27 can distinguish whether the input pins have any transitions by reading the registers and all of the 3 GPIOs also can assert PSOUT# or PME# to wake up the system if each them has any transition.

OnNow Functions

- Keyboard Wake-Up by programmable keys
- Mouse Wake-Up by programmable buttons
- On Now Wake-Up from all of the ACPI sleeping states (S1-S5)

Simple Serial Transport™ Interface

- SST temperature and voltage Combination Sensor command support
- Support SST 0.9 Specification

PECI Interface

- PECI Host
- Support PECI 1.0 Specification
- Support 4 CPU addresses and 2 domains per CPU address

Package

- W83627UHG 128-pin QFP, 14mm x 20mm x 2.75mm
- NCT6627UD 128-pin LQFP, 14mm x 14mm x 1.4mm
- Green / RoHS

3. BLOCK DIAGRAM

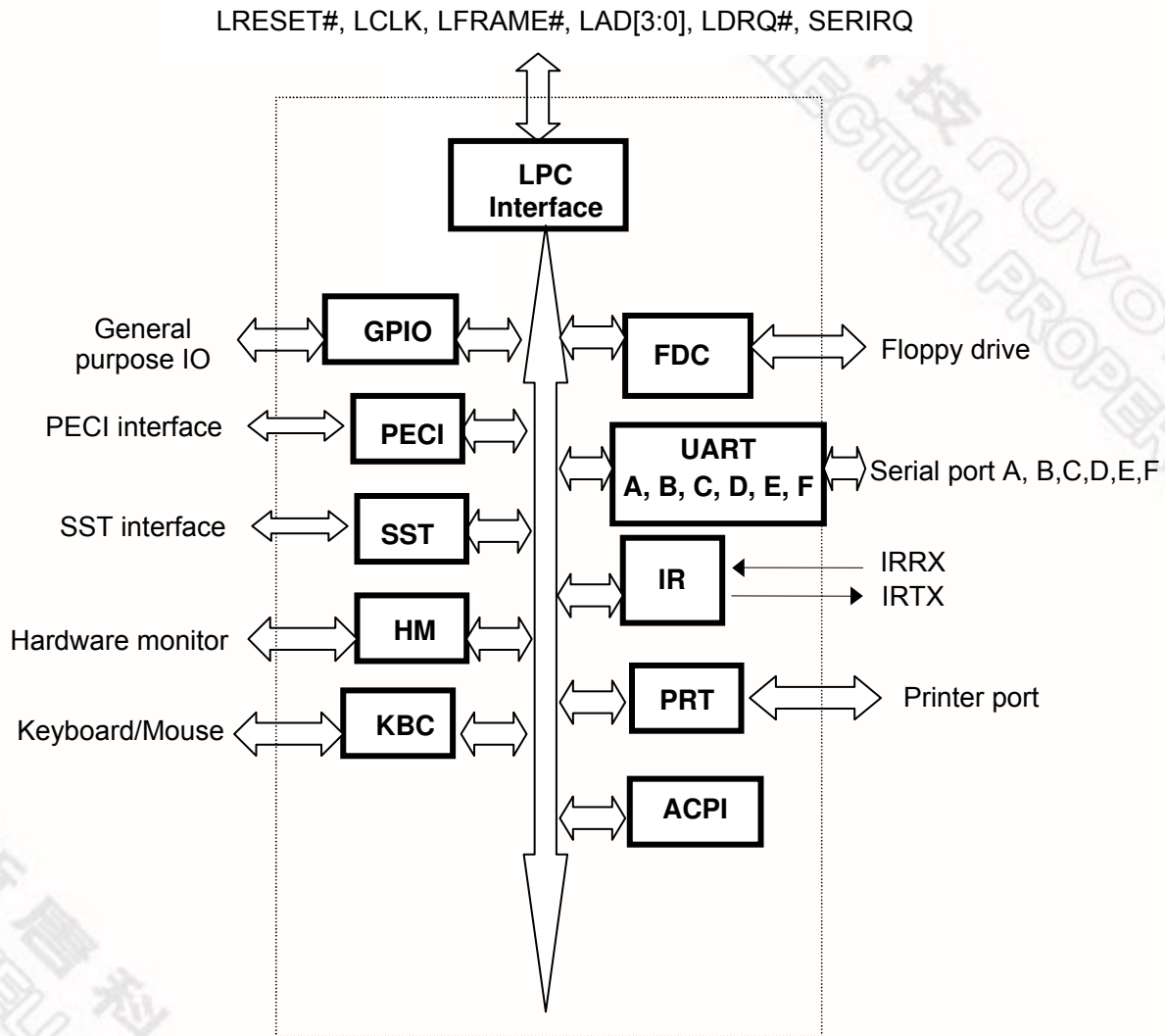


Figure 3-1 W83627UHG and NCT6627UD Block Diagram

4. PIN LAYOUT

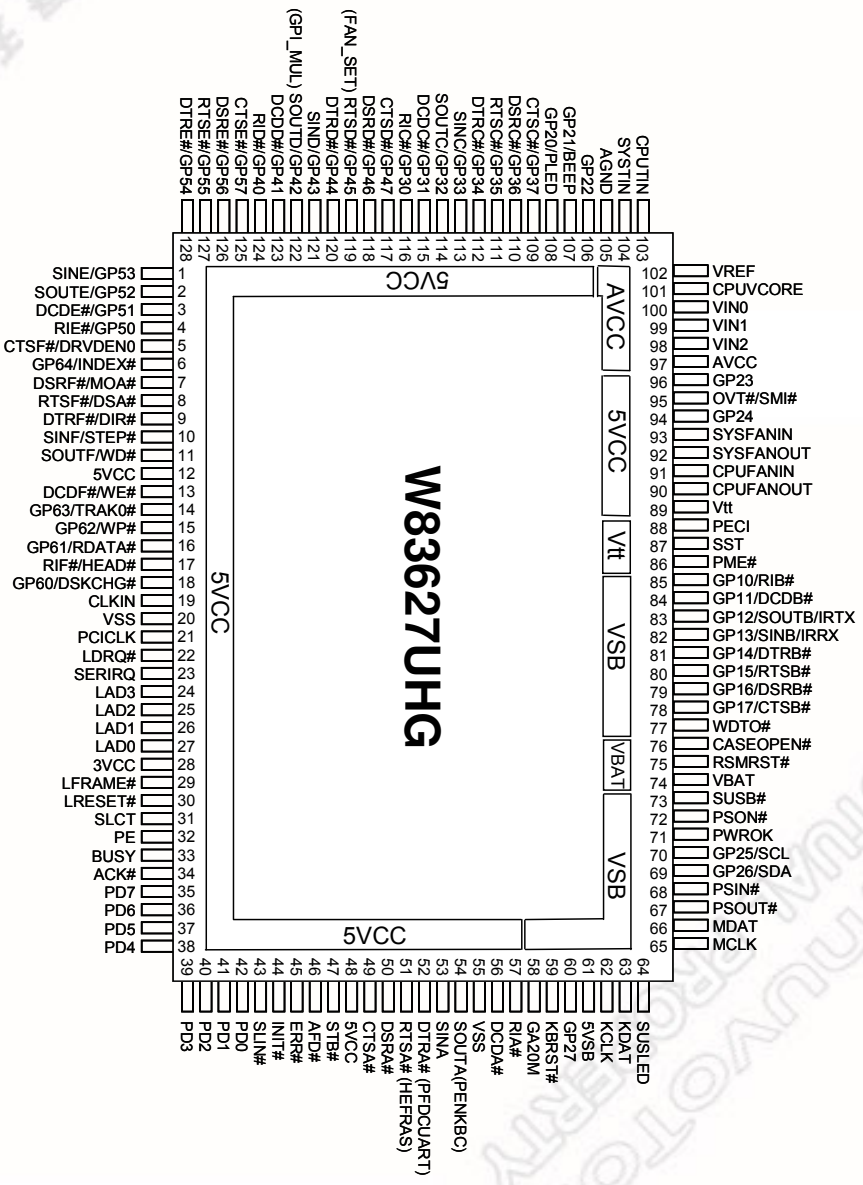


Figure 4-1 W83627UHG Pin Layout

5. PIN DESCRIPTION

Note: Please refer to 18.2 DC CHARACTERISTICS for details.

AOUT	- Analog output pin
AIN	- Analog input pin
I/O _{12tp3}	- 3.3-V, TTL-level, bi-directional pin with 12mA source-sink capability
I/O _{12ts}	- TTL-level Schmitt-trigger bi-directional pin with 12mA source-sink capability
I/OD ₈	- Bi-directional pin. Open-drain output with 8mA sink capability.
I/OD _{8t}	- TTL-level, bi-directional pin. Open-drain output with 8mA sink capability.
I/OD _{12t}	- TTL-level, bi-directional pin and open-drain output with 12mA sink capability
I/OD _{16ts}	- TTL-level Schmitt-trigger bi-directional pin and open-drain output with 16mA sink capability
I/OD _{12ts}	- TTL-level Schmitt-trigger bi-directional pin and open-drain output with 12mA sink capability
I/OD _{12tsu}	- TTL-level, bi-directional, Schmitt-trigger pin with internal pull-up resistor - Open-drain output with 12-mA sink capability.
I/O _{v3}	- Bi-direction pin with source capability of 6 mA and sink capability of 1 mA
I/O _{v4}	- Bi-direction pin with source capability of 6 mA and sink capability of 1 mA
IN _{ts}	- TTL-level Schmitt-trigger input pin
IN _{tsu}	- TTL-level Schmitt-trigger input pin with internal pull-up resistor
IN _{tsp3}	- 3.3-V, TTL-level Schmitt-trigger input pin
IN _t	- TTL-level input pin
IN _{tu}	- TTL-level input pin with internal pull-up resistor
IN _{cd}	- CMOS-level input pin with internal pull-down resistor
O _{12p3}	- 3.3-V, output pin with 12mA source-sink capability
OD ₁₂	- Open-drain output pin with 12mA sink capability
OD ₂₄	- Open-drain output pin with 24mA sink capability
O ₈	- Output pin with 8mA source-sink capability
O ₁₂	- Output pin with 12mA source-sink capability
O ₂₄	- Output pin with 24mA source-sink capability

5.1 LPC Interface

SYMBOL	PIN	I/O	DESCRIPTION
CLKIN	19	IN _t	System clock input, either 24MHz or 48MHz. The actual frequency must be specified in register. The default value is 48MHz.
PME#	86	OD ₁₂	Generated PME event.
PCICLK	21	IN _{tsp3}	PCI-clock 33-MHz input.
LDRQ#	22	O _{12p3}	Encoded DMA Request signal.
SERIRQ	23	I/O _{12tp3}	Serialized IRQ input / output.
LAD[3:0]	24-27	I/O _{12tp3}	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
LFRAME#	29	IN _{tsp3}	Indicates the start of a new cycle or the termination of a broken cycle.
LRESET#	30	IN _{tsp3}	Reset signal. It can be connected to the PCIRST# signal on the host.

5.2 FDC Interface

SYMBOL	PIN	I/O	DESCRIPTION
DRVDEN0	5	OD ₂₄	Drive Density Select bit 0.
CTSF#		IN _t	Clear To Send. It is the modem control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
INDEX#	6	IN _{tsu}	This Schmitt-trigger input from the disk drive is active-low when the head is positioned over the beginning of a track marked by an index hole. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
GP64		I/OD _{12ts}	General purpose I/O port 6 bit 4.
MOA#	7	OD ₂₄	Motor A On. When set to 0, this pin enables disk drive A. This is an open-drain output.
DSRF#		IN _t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
DSA#	8	OD ₂₄	Drive Select A. When set to 0, this pin enables disk drive A. This is an open-drain output.
RTSF#		O ₂₄	UART F Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.

SYMBOL	PIN	I/O	DESCRIPTION
DIR#	9	OD ₂₄	Direction of the head step motor. An open-drain output. Logic 1 = outward motion Logic 0 = inward motion
DTRF#		O ₂₄	UART F Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate.
STEP#	10	OD ₂₄	Step output pulses. This active-low open-drain output produces a pulse to move the head to another track.
SINF		IN _t	Serial Input. This pin is used to receive serial data through the communication link.
WD#	11	OD ₂₄	Write data. This logic-low open-drain writes pre-compensation serial data to the selected FDD. An open-drain output.
SOUTF		O ₂₄	UART F Serial Output. This pin is used to transmit serial data out to the communication link.
WE#	13	OD ₂₄	Write enable. An open-drain output.
DCDF#		IN _t	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
TRAK0#	14	IN _{tsu}	Track 0. This Schmitt-trigger input from the disk drive is active-low when the head is positioned over the outermost track. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
GP63		I/OD _{12ts}	General purpose I/O port 6 bit 3.
WP#	15	IN _{tsu}	Write Protected. This active-low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
GP62		I/OD _{12ts}	General purpose I/O port 6 bit 2.
RDATA#	16	IN _{tsu}	The read-data input signal from the FDD. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
GP61		I/OD _{12ts}	General purpose I/O port 6 bit 1.
HEAD#	17	OD ₂₄	Head Select. This open-drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
RIF#		IN _t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.

SYMBOL	PIN	I/O	DESCRIPTION
DSKCHG#	18	IN _{tsu}	Diskette Change. This signal is active-low at power-on and whenever the diskette is removed. This input pin needs to connect a pulled-up 1-K Ω resistor to 5V for Floppy Drive compatibility.
GP60		I/OD _{12ts}	General purpose I/O port 6 bit 0.

5.3 Multi-Mode Parallel Port

SYMBOL	PIN	I/O	DESCRIPTION
SLCT	31	IN _{ts}	PRINTER MODE: An active-high input on this pin indicates that the printer is selected. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
PE	32	IN _{ts}	PRINTER MODE: An active-high input on this pin indicates that the printer has detected the end of the paper. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
BUSY	33	IN _{ts}	PRINTER MODE: An active-high input indicates that the printer is not ready to receive data. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
ACK#	34	IN _{ts}	PRINTER MODE: ACK# An active-low input on this pin indicates that the printer has received data and is ready to accept more data. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
ERR#	45	IN _{ts}	PRINTER MODE: ERR# An active-low input on this pin indicates that the printer has encountered an error. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
SLIN#	43	OD ₁₂	PRINTER MODE: SLIN# Output line for detection of printer selection. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
INIT#	44	OD ₁₂	PRINTER MODE: INIT# Output line for the printer initialization. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
AFD#	46	OD ₁₂	PRINTER MODE: AFD# An active-low output from this pin causes the printer to auto feed a line after a line is printed. See the description of the parallel port for the definition of this pin in ECP and EPP modes.

SYMBOL	PIN	I/O	DESCRIPTION
STB#	47	OD ₁₂	PRINTER MODE: STB# An active-low output is used to latch the parallel data into the printer. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
PD0	42	I/O _{12ts}	PRINTER MODE: PD0 Parallel port data bus bit 0. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
PD1	41	I/O _{12ts}	PRINTER MODE: PD1 Parallel port data bus bit 1. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
PD2	40	I/O _{12ts}	PRINTER MODE: PD2 Parallel port data bus bit 2. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
PD3	39	I/O _{12ts}	PRINTER MODE: PD3 Parallel port data bus bit 3. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
PD4	38	I/O _{12ts}	PRINTER MODE: PD4 Parallel port data bus bit 4. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
PD5	37	I/O _{12ts}	PRINTER MODE: PD5 Parallel port data bus bit 5. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
PD6	36	I/O _{12ts}	PRINTER MODE: PD6 Parallel port data bus bit 6. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
PD7	35	I/O _{12ts}	PRINTER MODE: PD7 Parallel port data bus bit 7. See the description of the parallel port for the definition of this pin in ECP and EPP modes.

5.4 Serial Port & Infrared Port Interface

SYMBOL	PIN	I/O	DESCRIPTION
CTSA#	49	IN _t	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
CTSB#	78	IN _t	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register. (This is for W83627UHG only)
GP17		I/OD _{12t}	General-purpose I/O port 1 bit 7.

SYMBOL	PIN	I/O	DESCRIPTION
CTSC#	109	IN _t	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
GP37		I/OD _{12t}	General-purpose I/O port 3 bit 7.
CTSD#	117	IN _t	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
GP47		I/OD _{12t}	General-purpose I/O port 4 bit 7.
CTSE#	125	IN _t	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
GP57		I/OD _{12t}	General-purpose I/O port 5 bit 7.
CTSF#	5	IN _t	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register. (This is for W83627UHG only)
DRVDE#		OD ₂₄	Drive Density Select bit 0.
DSRA#	50	IN _t	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
DSRB#	79	IN _t	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART. (This is for W83627UHG only)
GP16		I/OD _{12t}	General-purpose I/O port 1 bit 6.
DSRC#	110	IN _t	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
GP36		I/OD _{12t}	General-purpose I/O port 3 bit 6.
DSRD#	118	IN _t	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
GP46		I/OD _{12t}	General-purpose I/O port 4 bit 6.
DSRE#	126	IN _t	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
GP56		I/OD _{12t}	General-purpose I/O port 5 bit 6.
DSRF#	7	IN _t	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART. (This is for W83627UHG only)
MOA#		OD ₂₄	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.

SYMBOL	PIN	I/O	DESCRIPTION
RTSA#	51	O ₈	UART A Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
HEFRAS		IN _{cd}	During power-on reset, this pin is pulled down internally and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). The PCB layout should reserve space for a 1-kΩ resistor to pull down this pin so as to ensure the selection of I/O port's configuration address to 2EH, and a 1-kΩ resistor is recommended to pull it up if 4EH is selected as I/O port's configuration address.
RTSB#	80	O ₈	UART B Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data. (This is for W83627UHG only)
GP15		I/OD ₈	General-purpose I/O port 1 bit 5.
RTSC#	111	O ₈	UART C Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
GP35		I/OD ₈	General-purpose I/O port 3 bit 5.
RTSD#	119	O ₈	UART D Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
FAN_SET		IN _{cd}	Determines the initial FAN speed. Power-on configuration for 2 fan speeds, 50% or 100%. During power-on reset, this pin needs a pulled-up or a pull-down resistor to decide whether the fan speed is 50% or 100%.
GP45		I/OD ₈	General-purpose I/O port 4 bit 5.
RTSE#	127	O ₁₂	UART E Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
GP55		I/OD _{12t}	General-purpose I/O port 5 bit 5.
RTSF	8	O ₂₄	UART F Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data. (This is for W83627UHG only)
DSA#		OD ₂₄	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
DTRA#	52	O ₈	UART A Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
PFDCUART		IN _{cd}	During power-on reset, this pin is pulled down internally and is defined as FDC enable, which provides the power-on value for CR24 bit 1. A 1 kΩ is reserved to pull down and a 1 kΩ resistor is recommended if intends to pull-up to enable UART F.
DTRB#	81	O ₈	UART B Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate. (This is for W83627UHG only)
GP14		I/OD _{12t}	General-purpose I/O port 1 bit 4.

SYMBOL	PIN	I/O	DESCRIPTION
DTRC#	112	O ₈	UART C Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
GP34		I/OD _{12t}	General-purpose I/O port 3 bit 4.
DTRD#	120	O ₈	UART D Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
GP44		I/OD _{8t}	General-purpose I/O port 4 bit 4.
DTRE#	128	O ₈	UART E Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
GP54		I/OD _{12t}	General-purpose I/O port 5 bit 4.
DTRF#	9	O ₂₄	UART F Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate. (This is for W83627UHG only)
DIR#		OD ₂₄	Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
SINA	53	IN _t	Serial Input. This pin is used to receive serial data through the communication link.
SINB	82	IN _t	Serial Input. This pin is used to receive serial data through the communication link. (This is for W83627UHG only)
IRRX			IR Receiver input.
GP13		I/OD _{12t}	General-purpose I/O port 1 bit 3.
SINC	113	IN _t	Serial Input. This pin is used to receive serial data through the communication link.
GP33		I/OD _{12t}	General-purpose I/O port 3 bit 3.
SIND	121	IN _t	Serial Input. This pin is used to receive serial data through the communication link.
GP43		I/OD _{12t}	General-purpose I/O port 4 bit 3.
SINE	1	IN _t	Serial Input. This pin is used to receive serial data through the communication link.
GP53		I/OD _{12t}	General-purpose I/O port 5 bit 3.
SINF	10	IN _t	Serial Input. This pin is used to receive serial data through the communication link. (This is for W83627UHG only)
STEP#		OD ₂₄	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
SOUTA	54	O ₈	UART A Serial Output. This pin is used to transmit serial data out to the communication link.