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Nuvoton

PCI TO ISA BRIDGE

W83628AG

W83629AG

Revision: 1.2

Date: January, 2008

W83628AG & W83629AG Datasheet Revision History

	PAGES	DATES	VERSION	MAIN CONTENTS
1	N.A.	07/30/2007	0.5	1. First published version.
2	34, 38	08/02/2007	0.51	1. Update the information of Chapter 10 Absolute Maximum Ratings. 2. Modify the description of Chapter 12 AC Characteristics.
3	N.A.	11/01/2007	1.0	1. All versions before 1.0 are preliminary versions.
4	1	11/28/2007	1.1	1. Add the ordering information
5	11	31/1/2008	1.2	1. Modify DC characteristics

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Table of Contents –

1. GENERAL DESCRIPTION

The W83628AG is a PCI-to-ISA bus conversion IC. The W83629AG is a condensed centralizer IC for IRQ and DMA control. W83628AG and W83629AG together form a complete set for the PCI-to-ISA bridge.

For the new generation Intel chipsets featuring LPC bus but not supporting ISA bus and slots, the W83628AG plus the W83629AG are the best companion solution for the non-ISA chipset. Also the packages of the W83628AG (128-QFP) and the W83629AG (48-LQFP) are the most cost-effective solution that minimizes the M/B board layout size and cost.

For the new generation chipsets featuring LPC interface but not supporting ISA bus, the best and the most complete solution will be the combination of the W83627 (Nuvoton LPC I/O) family and the set of the W83628AG and the W83629AG.

2. FEATURES

PCI to ISA Bridge

- Full ISA Bus Support, including ISA Masters

- 5V ISA and 3.3V PCI interfaces

- PC/PCI DMA protocol for Software Transparent

- IRQ Serializer for ISA Parallel IRQ transfer to Serial IRQ

- Supports 3 fully ISA Compatible Slots without Buffering

- PCI Bus at 25MHz, 33MHz and up to 40MHz

- Supports Programmable ISA Bus Divide the PCI Bus Clock into 3 or 4

- All ISA Signals can be Isolated

- Supports Configuration registers for performance programming

3. PACKAGE

- 128-pin QFP for the W83628AG

- 48-pin LQFP for the W83629AG

4. ORDERING INFORMATION

PART NUMBER	DESCRIPTION	PRODUCTION FLOW
W83628AG	128-PIN QFP, Pb-free	Commercial, 0°C to +70°C
W83629AG	48-PIN LQFP, Pb-free	Commercial, 0°C to +70°C
W83628AGEVB	W83628/629AG Evaluation board	

5. BLOCK DIAGRAM OF W83628AG
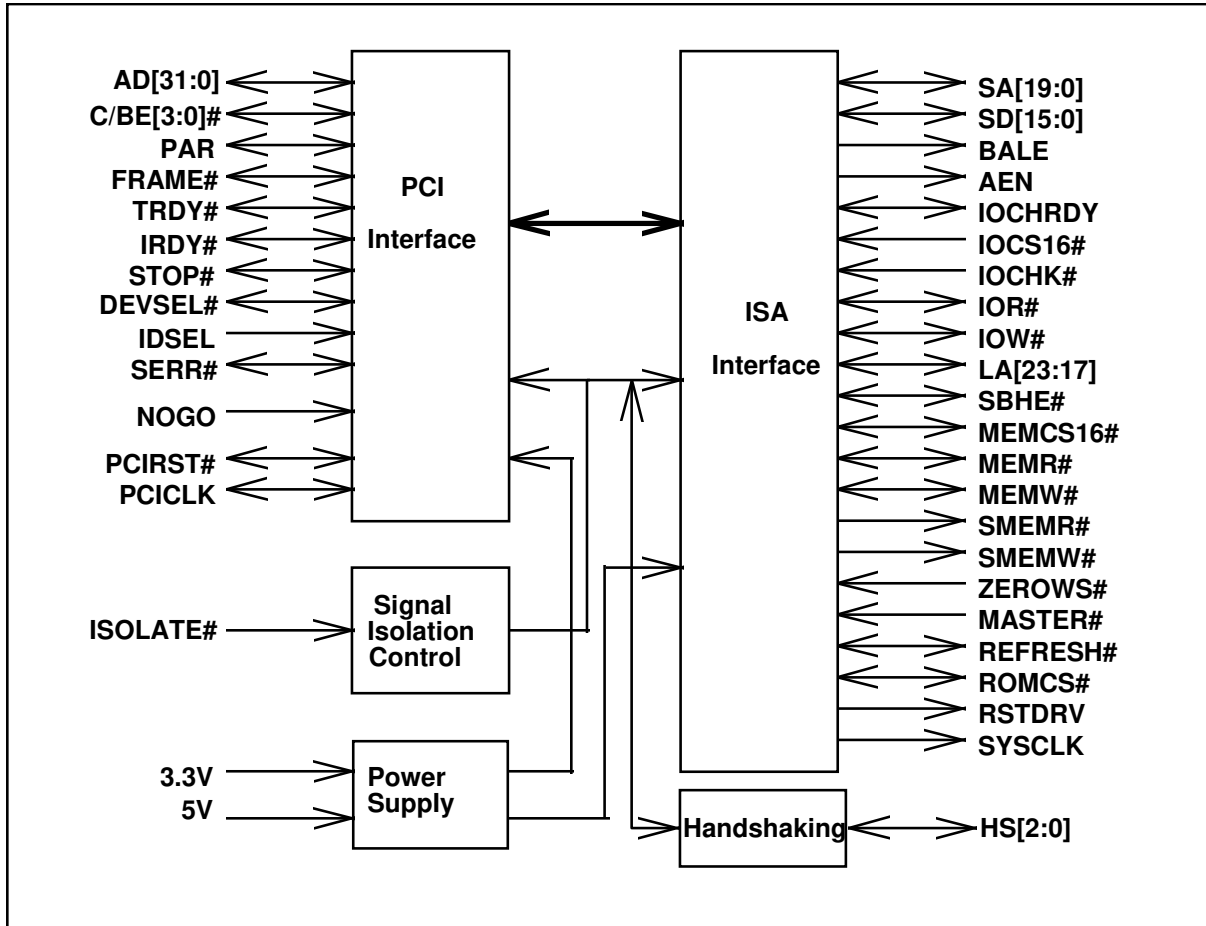
6. BLOCK DIAGRAM OF W83629AG
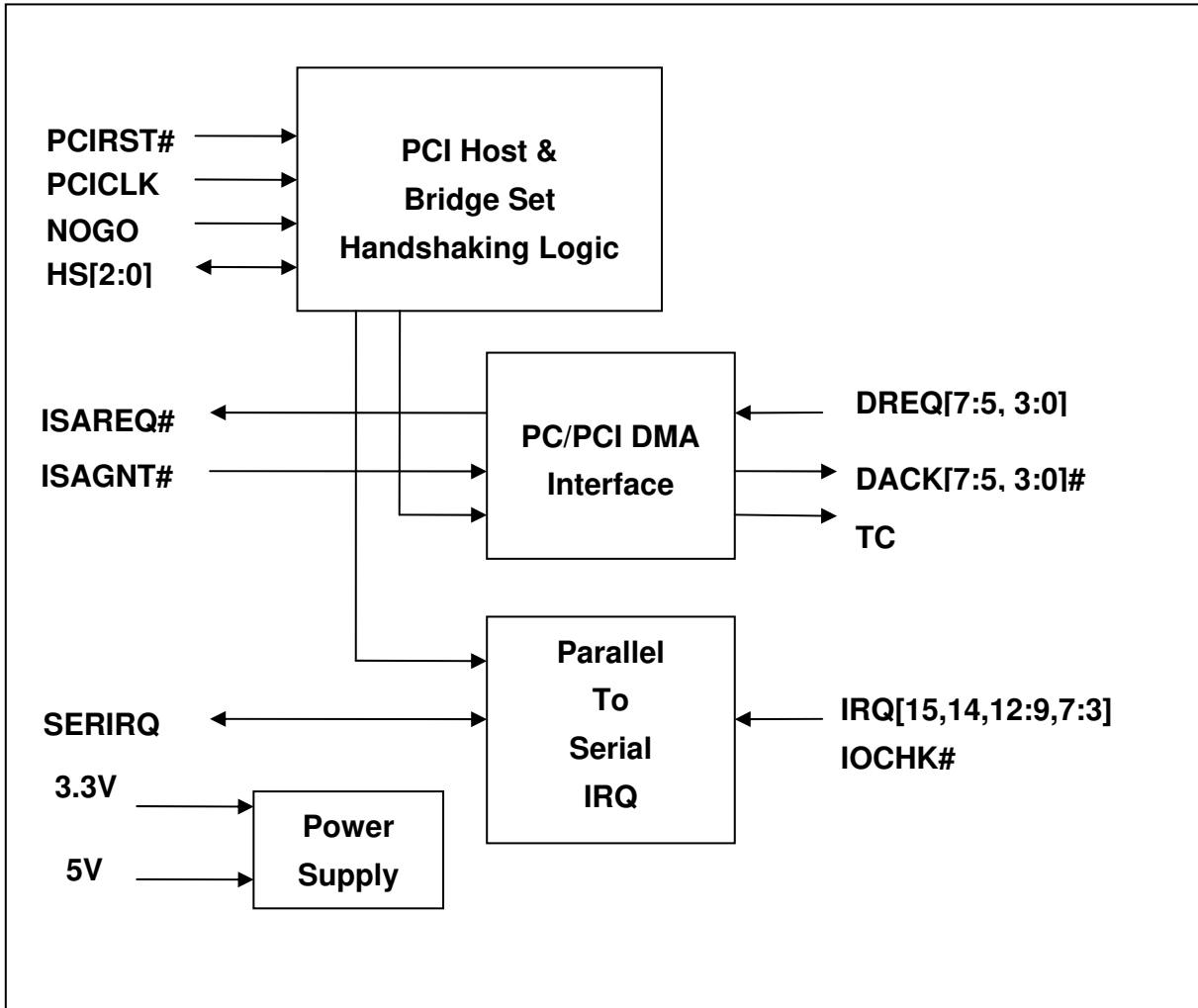
7. FUNCTION DESCRIPTION

The W83628AG and W83629AG support the functional sub-block interfaces described below:

7.1 PCI Interface

The W83628AG provides a PCI slave/master interface. The slave mode means the PCI cycles are initiated by the PCI Host Bridge or South Bridge chipset. Default is PCI bus cycle information from PCI Host Bridge being received in PCI slave mode. When ISA bus's MASTER# signal is asserted, the W83628A's PCI interface as slave mode will be switched to PCI master mode to drive/initiate PCI bus cycles to PCI bus. The W83628AG supports some positive decodes and implements subtractive decodes for unclaimed PCI accesses.

The PCI slave interface supports the positive decodes as below:

- PCI configuration register spaces which are positively decode with medium DEVSEL# timing speed on the Type0 PCI configuration cycle.
- Eight IO positively decode space which can be programmed to claim PCI I/O cycle with Fast/Medium/Slow/Subtractive DEVSEL# timing speed.
- Four Memory positively decode spaces which can be programmed to claim PCI Memory cycle with Fast/Medium/Slow/Substractive DEVSEL# timing speed.
- PC/PCI DMA (PPDMA) cycle space:The I/O portion of the DMA cycle generates a PCI I/O cycle to one of the four I/O addresses of 0000h/0004h/00C0h/00C4h
- ISA BIOS ROM boot up scheme: upload boot ROM on ISA bus during system boot up. Enable/disbale optionally the function through the external pull-up resistor on signal ROMCS# of the W83628AG. When PCIRST# is asserted, the signal ROMCS# will be detected and latched. After PCIRST# is released, the latched signal High(1)/Low(0) means to enable(1)/disable(0) the ISA BIOS ROM boot up function, respectively. The latched bit can also be disabled/enabled through Type0 PCI configuration cycle.

The PCI master interface will issue PCI cycle for ISA bus master cycle.

The W83628AG and the W83629AG together support PC/PCI DMA. The W83629AG uses dedicated ISAREQ# and ISAGNT# signals to permit ISA devices' transfer requests associated with specific DMA channels. Upon receiving a request and getting control of the PCI bus, South Bridge chipset performs a two-cycle transfer. For example, if data is to be moved from the peripheral to the main memory, the chipset will first read data from the peripheral and then write it to the main memory.

When in PC/PCI DMA cycle, the W83629AG DACKn# is decoded from ISAGNT#. As long as the ISAGNT# and MASTER# signals are asserted and are with an ISA command issued by ISA master, then the W83628AG PCI master interface will issues a PCI cycle for ISA master.

7.2 ISA Interface

The W83628AG provides an ISA bus interface for the subtractive decoded memory and I/O cycles on PCI. Default is driving/issuing relative legacy ISA bus cycle to ISA bus in ISA master mode. Generally if a valid PCI memory or I/O cycle is received by the W83628AG PCI slave interface, it will be passed to the internal ISA interface and the ISA interface will convert it to correspond to the ISA bus cycle. When ISA bus's MASTER# signal is asserted, the W83628AG ISA interface as master mode will be switched to ISA slave mode to receive legacy ISA bus cycles from the ISA bus. That means there is an ISA command issued by ISA master. The related ISA bus cycle will be passed to PCI master interface to drive/issue corresponding PCI bus cycle.

7.3 Serial IRQ Interface

The W83629AG supports a serialized IRQ slave which conforms to the specification of "Serialized IRQ Support for PCI system, rev. 6.0, September 1, 1995". Two modes, continuous and quiet, are supported.

The serial IRQ interface provides signal filtering and encoding logic for all legacy parallel ISA IRQ channels (IRQ15-14, 12-9, 7-3 and IOCHK#) to convert them to serial IRQ on the SERIRQ line. The IRQ/Data serializer is a Wired-OR structure that simply passes the state of one or more device's IRQ(s) and/or Data to the host controller. The transfer can be initiated by either a device or the host controller. A transfer, called an IRQSER Cycle, consists of three frame types: one Start Frame, several IRQ/Data Frames, and one Stop Frame.

This protocol uses the PCI Clock as its clock source and conforms to the PCI bus electrical specification.

- Start Frame timing with source sampled a low pulse on IRQ1
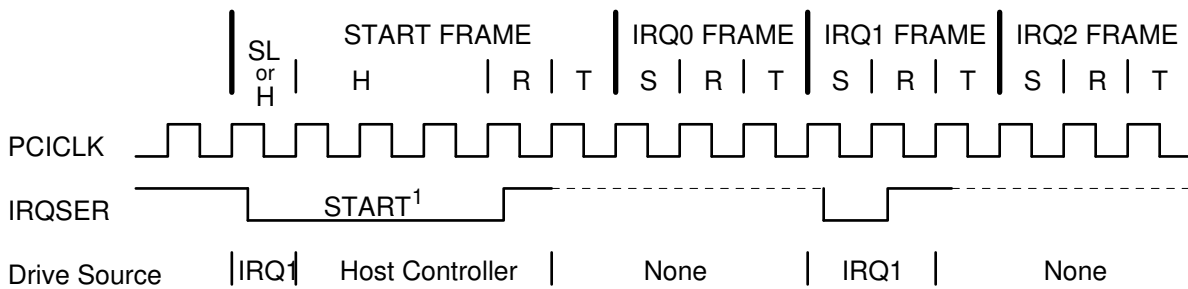
H=Host Control   SL=Slave Control   R=Recovery   T=Turn-around   S=Sample

Start Frame pulse can be 4-8 clocks wide

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● Stop Frame Timing with Host using 17 IRQSER sampling period

	IRQ14 FRAME			IRQ15 FRAME			IOCHCK# FRAME				STOP FRAME			NEXT CYCLE
	S	R	T	S	R	T	S	R	T	I [2]	H	R	T	

PCICLK

IRQSER   STOP[1]   START[3]

Driver	None		IRQ15		None		Host Controller	
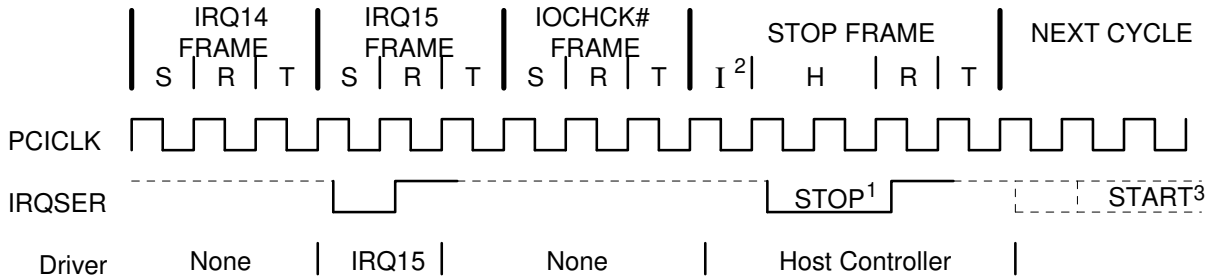
H=Host Control   R=Recovery   T=Turn-around   S=Sample   I= Idle.

1. Stop pulse is 2 clocks wide for Quiet mode, 3 clocks wide for Continuous mode.
2. There may be none, one or more Idle states during the Stop Frame.
3. The next IRQSER cycle's Start Frame pulse <u>may</u> or may not start immediately after the turn-around clock of the Stop Frame.

The main difference between the quite mode and the continuous mode for the IRQSER Frame is:

● Quiet (Active) Mode: Any device may initiate a Start Frame by driving the IRQSER low for one clock, while the IRQSER is Idle.

● Continuous (Idle) Mode: Only the Host controller can initiate a Start Frame to update IRQ/Data line information.

7.4   PC/PCI DMA Interface

The W83629AG supports PC/PCI DMA Serial Channel Passing Protocol interface as shown in Figure 6-1.
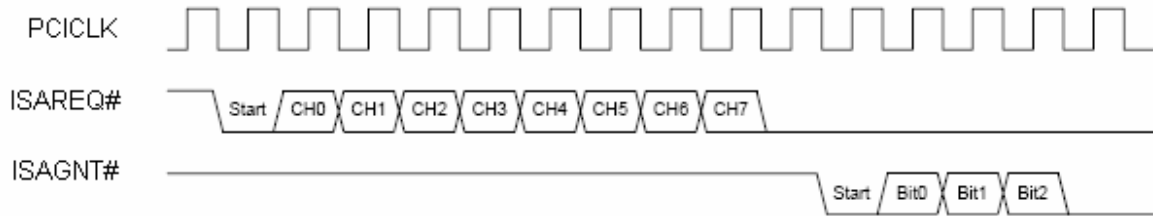
Figure 6-1: PC/PCI DMA Serial Channel Passing Protocol

When the W83629AG receives the legacy ISA DMA requesting DRQn, the DMA interface must encode the channel request information, where CH0-CH7 will be active high, depending on which is requested as the DMA channel.

The South Bridge chipset encodes the granted channel on the ISAGNT# line, where the bits have the same meaning. For example, the sequence [start, bit0, bit1, bit2] = [0, 1, 0, 0] grants DMA channel 1 to the requesting device, and the sequence [start, bit0, bit1, bit2] = [0, 0, 1, 1] grants DMA channel 6 to the requesting device.

After receiving a valid grant and detecting ISAGN# start bit, the W83629AG will decode and convert the ISAGNT# signal information to corresponding legacy ISA DMA acknowledge DACKn# signal.

Table 6-1 below shows the I/O portion of the DMA cycle generates a PCI I/O cycle to one of the four I/O addresses. The W83628AG will recognize the PCI I/O cycle with the DMA I/O address. These cycles must be qualified by an active ISAGNT# signal to the requesting device. A2 of DMA I/O address bit 2 is used to indicate DMA Terminal Count cycle.

DMA CYCLE TYPE	DMA I/O ADDRESS	TC(A2)	PCI CYCLE TYPE
Normal	00h	0	I/O Read/Write
Normal TC	04h	1	I/O Read/Write
Verify	0C0h	0	I/O Read
Verify TC	0C4h	1	I/O Read

Table 6-1: DMA Cycle Type and I/O Address

7.5   ISA Bus SYSCLK Clock Generation

The W83628AG generates the ISA SYSCLK clock using PCI clock signal. A PCICLK divisor (3, 4) is programmable through PCI configuration register to generate the ISA SYSCLK clock signal. This provides ISA SYSCLK frequencies 8.33MHz and 11MHz of a typical 33MHz PCICLK.

7.6   ISA Bus I/O Recovery Time

The W83628AG supports 8-bit/16-bit I/O recovery time for back-to-back ISA I/O cycles. The register can be programmed through Type0 PCI configuration cycle.

7.7   NOGO

The W83628AG and W83629AG also support NOGO function. The NOGO signal generally connected to South Bridge chipset's NOGO signal is used to disable the subtractive decode function when NOGO signal is asserted high during system boot-up, since there is only one subtractive decode device presented on the PCI bus .

8. PIN CONFIGURATION

8.1   PIN CONFIGURATION FOR W83628AG

W83628AG

Left side pins:

SD5	103
SD4	104
IOCHK#	105
ZEROWS#	106
SD3	107
SD2	108
SD1	109
SD0	110
GND	111
HS2	112
HS1	113
HS0	114
VCC	115
IOCHRDY	116
SMEMR#	117
AEN	118
SMEMW#	119
IOR#	120
IOW#	121
BALE	122
MEMCS16#	123
IOCS16#	124
LA17	125
LA18	126
LA19	127
GND	128

Right side pins:

64	3VCC
63	AD5
62	AD6
61	AD7
60	C/BE0#
59	AD8
58	AD9
57	AD10
56	AD11
55	AD12
54	AD13
53	AD14
52	AD15
51	C/BE1#
50	GND
49	PAR
48	NC
47	PCICLK
46	3VCC
45	SERR#
44	C/BE2#
43	DEVSEL#
42	TRDY#
41	IRDY#
40	FRAME#
39	STOP#

8.2   PIN CONFIGURATION FOR W83629AG

9. PIN DESCRIPTION

Note: Please refer to Section 10 DC CHARACTERISTICS for details.

I/O$_{10t}$ - TTL level bi-directional pin with 10 mA source-sink capability

I/O$_{18t}$ - TTL level bi-directional pin with 18 mA source-sink capability

I/O$_{10tp3}$ - 3.3V TTL level bi-directional pin with 10 mA source-sink capability

I/O$_{18tp3}$ - 3.3V TTL level bi-directional pin with 18 mA source-sink capability

I/OD$_{10t}$ - TTL level bi-directional pin open drain output with 10 mA sink capability

I/OD$_{18t}$ - TTL level bi-directional pin open drain output with 18 mA sink capability

OUT$_{10t}$ - TTL level output pin with 10 mA source-sink capability

OUT$_{18t}$ - TTL level output pin with 18 mA source-sink capability

OD$_{10}$ - Open-drain output pin with 10 mA sink capability

IN$_t$ - TTL level input pin

IN$_{ts}$ - TTL level Schmitt-trigger input pin

9.1   W83628AG PIN DESCRIPTION

9.1.1 PCI Interface

SYMBOL	PIN	I/O	FUNCTION	LEVEL
AD[31:0]	19-26 30-37 52-59 61-63 66-70	I/O$_{18tp3}$	**PCI Bus Address and Data Signals.** The standard PCI address and data lines. The address is driven with FRAME# assertion; the data is driven or received in following clocks.	3.3V
C/BE[3:0]#	28,44 51,60	I/O$_{18tp3}$	**PCI Bus Command and Byte Enables.** During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase, C/BE[3:0]# are used as Byte Enables.	3.3V
PCICLK	47	IN$_{ts}$	**PCI Bus System Clock**. PCICLK provides timing for all transactions on the PCI bus. All the other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge.	3.3V

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8.1.1 PCI Interface, contiuned

SYMBOL	PIN	I/O	FUNCTION	LEVEL
FRAME#	40	I/O$_{18tp3}$	**Frame Signal**. FRAME# is driven by the current PCI bus master to indicate the beginning and duration of an access.	3.3V
IDSEL	29	IN$_{ts}$	**Initialization Device Select.** IDSEL is used as a chip select during configuration read and write transactions. This signal should be externally tied to one of the upper 21 address signals.	3.3V
STOP#	39	I/O$_{10tp3}$	**Bus Stop#.** STOP# indicates the current target is requesting the master to stop the current PCI bus transaction.	3.3V
IRDY#	41	I/O$_{10tp3}$	**Initiator Ready.** IRDY# indicates the initiating agent's ability to complete the current data phase of the PCI bus transaction.	3.3V
TRDY#	42	I/O$_{10tp3}$	**Target Ready.** TRDY# indicates the target agent's ability to complete the current data phase of the PCI bus transaction.	3.3V
DEVSEL#	43	I/O$_{10tp3}$	**Device Select.** The W83628AG drives DEVSEL# to indicate that it is the target of the current PCI bus transaction. The W83628AG uses subtractive decoding and the NOGO protocol to claim PCI transactions.	3.3V
SERR#	45	OD$_{10}$	**System Error.** SERR# can be pulsed active by any PCI agent that detects a system error condition.	3.3V
PAR	49	I/O$_{10tp3}$	**Parity Signal.** The W83628AG generates even parity across AD[31:0] and C/BE[3:0]#.	3.3V
PCIRST#	71	IN$_{ts}$	**PCI Reset.** The W83628AG receives PCIRST# as a reset from the PCI Bus.	3.3V

9.1.2 Control Logic and Handshaking Signals

SYMBOL	PIN	I/O	FUNCTION	LEVEL
HS[2:0]	112-114	I/O$_{10t}$	**Handshaking Signals.** HS[2:0] are connected to the W83629AG for PCI to ISA SET handshaking signals. **HS1 is handshaking Signal 1; this pin is weak pulled-down while PCIRST# is asserted. Applying a pull-up resistor (4.7Kohm) to this pin disables ISA bridge subtraction decoder.**	5V
ISOLATE#	72	IN$_{ts}$	**Isolation Control Input. Isolate#** is an active low signal by user programming to control all of the output signals of the W83628AG to Isolation and Tri-state.	3.3V
NOGO	76	IN$_t$	**NOGO,** This signal indicates which master initiates the current transaction and whether or not the current bus cycle is targeted for the ISA bus. This signal is a point-to-point connection between PCI HOST Bridge and the W83628AG.	5V

9.1.3 ISA Interface Signals

SYMBOL	PIN	I/O	FUNCTION	LEVEL
SA[19:17]	98-96	I/O$_{18t}$	**System Address Bus.** These are the upper address lines that define the ISA's byte granular address space (up to 1 Mbyte). SA[19:17] are at an unknown state upon PCIRST#.	5V
SA[16:0]	94-83 81-77	I/O$_{18t}$	**System Address Bus.** These are the bi-directional lower address lines that define the ISA's byte granular address space (up to 1 Mbyte). SA[16:0] are at an unknown state upon PCIRST#.	5V
SD[15:0]	110-107, 104,103, 101,100, 8-15	I/O$_{18t}$	**System Data.** SD[15:0] provide the 16-bit data path for devices residing on the ISA Bus. The W83628AG tri-states SD[15:0] during PCIRST#.	5V
AEN	118	OUT$_{18t}$	**Address Enable.** AEN is asserted during DMA cycles. This signal is also driven high when the W83628AG initiates refresh cycles. AEN is driven low upon PCIRST#.	5V
IOR#	120	I/O$_{18t}$	**I/O Read.** IOR# is the command to an ISA I/O slave device that the slave may drive data on to the ISA data bus (SD[15:0]).	5V

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SYMBOL	PIN	I/O	FUNCTION	LEVEL
IOW#	121	I/O$_{18t}$	**I/O Write.** IOW# is the command to an ISA I/O slave device that the slave may latch data from the ISA data bus (SD[15:0]).	5V
IOCHRDY	116	I/O$_{18t}$	**I/O Channel Ready.** Resources on the ISA Bus negate IOCHRDY to indicate that additional time (wait states) is required to complete the cycle.	5V
SYSCLK	99	OUT$_{18t}$	**ISA System Clock.** SYSCLK is the reference clock for the ISA bus. The SYSCLK is generated by dividing PCICLK by 3 or 4.	5V
RSTDRV	74	OUT$_{18t}$	**Reset Drive.** The W83628AG asserts RSTDRV to reset devices that reside on the ISA Bus. The W83628AG asserts this signal while the PCIRST# is asserted.	5V
IOCS16#	124	IN$_t$	**16-bit I/O Chip Select.** This signal is driven by I/O devices on the ISA Bus to indicate that they support 16-bit I/O bus cycles.	5V
SBHE#	18	I/O$_{18t}$	**System Byte High Enable.** SBHE# asserted indicates that a byte is being transferred on the upper byte (SD[15:8]) of the data bus. SBHE# is at an unknown state upon PCIRST#.	5V
IOCHK#	105	IN$_t$	**I/O Channel Check.** IOCHK# can be driven by any resource on the ISA bus during the detection of an error.	5V
MEMR#	6	I/O$_{18t}$	**Memory Read.** MEMR# asserted indicates the current ISA bus cycle is a memory read.	5V
MEMW#	7	I/O$_{18t}$	**Memory Write.** MEMW# asserted indicates the current ISA bus cycle is a memory write.	5V
MASTER#	17	IN$_t$	**MASTER#.** This signal is used with a DREQ line by an ISA master to gain control over the ISA Bus.	5V
LA[23:17]	5-2 127-125	I/O$_{18t}$	**Unlatched Address.** The LA[23:17] address lines are bi-directional. These address lines allow accesses to physical memory on the ISA Bus up to 16 Mbytes. LA[23:17] are outputs when the W83628AG owns the ISA Bus.	5V

SYMBOL	PIN	I/O	FUNCTION	LEVEL
ROMCS#	73	I/O$_{10t}$	**ROMCS#. This pin is weak pulled-down while PCIRST is asserted. Applying a pull-up resistor (4.7K ohm) to this pin enables positive decoder of BIOS address range (depending on Configure register 70, bit 3,2). When the BIOS access range is enabled, the pin is BIOS ROMCS# output.**	5V
REFRESH#	75	I/O$_{18t}$	**Refresh.** REFRESH# asserted indicates that a refresh cycle is in progress, or that an ISA master is requesting the W83628AG to generate a refresh cycle. Upon PCIRST#, this signal is tri-stated.	5V
ZEROWS#	106	IN$_t$	**Zero Wait States.** An ISA slave asserts ZEROWS# after its address and command signals are decoded to indicate that the current cycle can be executed as an ISA zero wait state cycle. ZEROWS# has no effect during 16-bit I/O cycles.	5V
SMEMR#	117	OUT$_{18t}$	**Standard Memory Read.** SMEMR# asserted indicates the current ISA bus cycle is a memory read cycle to an address below 1 Mbyte.	5V
SMEMW#	119	OUT$_{18t}$	**Standard Memory Write.** SMEMW# asserted indicates the current ISA bus cycle is a memory write cycle to an address below 1 Mbyte.	5V
BALE	122	OUT$_{18t}$	**Bus Address Latch Enable.** BALE is an active high signal asserted by the W83628AG to indicate that the address (SA[19:0], LA[23:17]) and SBHE# signal lines are valid. The LA[23:17] address lines are latched on the trailing edge of BALE. BALE remains asserted throughout DMA and ISA master cycles. BALE is driven low upon PCIRST#.	5V
MEMCS16#	123	I/OD$_{18t}$	**Memory Chip Select 16.** MEMCS16# asserted indicates that the memory slave supports 16-bit accesses.	5V

9.1.4 Power Signals

SYMBOL	PIN	I/O	FUNCTION	LEVEL
VCC	1, 82, 102, 115	PWR	**5V Supply.**	5V
3VCC	27, 46, 64	PWR	**3.3V Supply.**	3.3V
GND	16, 38, 50, 65, 95, 111, 128	PWR	**Ground.**	0V

9.1.5 NC Pins

SYMBOL	PIN	I/O	FUNCTION	LEVEL
NC	48		**No Connection.**	

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9.2 W83629AG PIN DESCRIPTION

9.2.1 Control Logic and Handshaking Signals

SYMBOL	PIN	I/O	FUNCTION	LEVEL
HS[2:0]	17-15	I/O$_{10t}$	**Handshaking Signals.** HS[2:0] are connected to the W83628AG for PCI to ISA SET handshaking signals.	5V
NOGO	40	IN$_{ts}$	**NO GO.** This signal indicates which master initiates the current transaction and whether or not the current bus cycle is targeted for the ISA bus. This signal is a point-to-point connection between PCI HOST Bridge and the W83628AG.	5V
PCICLK	44	IN$_{ts}$	**PCI Bus System Clock**. PCICLK provides timing for all transactions on the PCI bus. All the other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge.	3.3V
PCIRST#	47	IN$_{ts}$	**PCI Reset.** The W83628AG receives PCIRST# as a reset from the PCI Bus.	3.3V

9.2.2 PC/PCI Interface

SYMBOL	PIN	I/O	FUNCTION	LEVEL
ISAREQ#	41	OUT$_{18t}$	**ISA Bus Request.** This signal is a point-to-point signal between the W83629AG and a PCI HOST arbiter. The W83629AG asserts this signal according to the PC/PCI protocol.	3.3V
ISAGNT#	42	IN$_{ts}$	**ISA Bus Grant.** This signal is a point-to-point signal between the W83629AG and a PCI HOST Bridge's secondary bus PCPCIGNT# signal. The W83629AG asserts this signal according to the PC/PCI protocol.	3.3V
DRQ [7:5,3:0]	35,33,31, 28,26,23, 21	IN$_t$	**DMA Request.** The DREQ signal indicates that either a slave DMA device is requesting DMA services, or an ISA bus master is requesting to use the ISA bus.	5V

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SYMBOL	PIN	I/O	FUNCTION	LEVEL
DACK [7:5,3:0]#	34,32,30, 27,24,22, 20	OUT$_{18t}$	**DMA Acknowledge.** The DACK# signal indicates that either a DMA channel or an ISA bus master is granted to the ISA bus.	5V
TC	19	OUT$_{18t}$	**Terminal Count.** The W83628AG asserts TC to DMA slaves as a terminal count indicator.	5V

9.2.3   IRQ Serializer Interface

SYMBOL	PIN	I/O	FUNCTION	LEVEL
SERIRQ	46	I/OD$_{10t}$	**Serial Interrupt Requested Signals.** This signal is to transfer IRQ from the parallel IRQ mode to the serial IRQ mode.	3.3V
IRQ[3:7,9:12,14,15]	2-6 8-13	IN$_t$	**Parallel Interrupt Requested Input.**	5V
IOCHK#	36	IN$_t$	**I/O Channel Check.** IOCHK# can be driven by any resource on the ISA bus with the detection of an error.	5V

9.2.4   Power Signals

SYMBOL	PIN	I/O	FUNCTION	LEVEL
VCC	7, 14, 25	PWR	**5V Supply.**	5V
3VCC	48	PWR	**3.3V Supply.**	3.3V
GND	1, 18, 29, 43	PWR	**Ground.**	0V

9.2.5   NC Pins

SYMBOL	PIN	I/O	FUNCTION	LEVEL
NC	37, 38, 39, 45		**No Connection**	

10. PCI CONFIGURATION REGISTERS

10.1 VID-VENDOR IDENTIFICATION REGISTER

Address Offset: 01h_00h
Default Value: 10h_50h
Attribute: Read only

This register is read-only and contains Nuvoton vendor identification number (1050h).

10.2 DID-DEVICE IDENTIFICATION REGISTER

Address Offset: 03h_02h
Default Value: 06h_28h
Attribute: Read only

This register is read-only and contains the device identification number (0628h).

10.3 PCICMD-PCI COMMAND REGISTER

Address Offset: 05h_04h
Default Value: 00h_07h
Attribute: Read/Write

This register provides control over the ISA bridge to generate and respond to PCI cycles properly. When a 0 is written to this register, the ISA bridge is to be disconnected from the PCI bus for all accesses except configuration accesses.

Bit 15:10   **Reserved.**

Bit 9   **Fast Back to Back.** This bit always returns a zero.

Bit 8   **SERR# Enable.**

    =1   Enable.
    =0   Disable.

Bit 7   **Wait Cycle Control (Not supported).**

    Hardwired to zero.

Bit 6   **Parity Error Response (Not supported).**

    Hardwired to zero.

Bit 5   **VGA Palette Snoop Enable (Not supported).**

    Hardwired to zero.

Bit 4   **Memory Write and Invalidate Enable (Not supported).**

Hardwired to zero.

Bit 3   **Parity Error Response (Not supported).**

Hardwired to zero.

Bit 2   **Bus Master Enable**

Hardwired to one. The ISA bridge Bus Masters are always supported to generate a PCI Bus master cycle.

Bit 1   **Memory Space Enable**

Hardwired to one. The ISA bridge Memory space is always enabled.

Bit 0   **I/O Space Enable**

Hardwired to one. The ISA bridge I/O space is always enabled.

10.4   PCISTS-PCI STATUS REGISTER

Address Offset: 07h_06h
Default Value: 02h_00h
Attribute: Read/Write

This register shows status information for PCI bus related events.

Bit 15   **Detected Parity Error**

Hardwired to zero. The ISA bridge does not check bus parity.

Bit 14   **Signaled System Error**

This bit is set when ISA bridge asserts SERR# on PCI bus.

Bit 13   **Received Master Abort Status**

This bit is set when the ISA bridge is target aborted as a master on the PCI bus.
Software sets this bit to 0 by writing a 1 to it.

Bit 12   **Received Target Abort Status**

This bit is set when the ISA bridge target aborts a PCI transaction as a target.
Software sets this bit to 0 by writing a 1 to it.

Bit 11   **Signaled Target Abort Status**

This bit is set when the ISA bridge signals a target abortion for a PCI transaction. Software sets this bit to 0 by writing a 1 to it.

Bit 10:9 **DEVSEL# Timing.** This 2 bits always return a 01b (medium decode).

Bit 8   **Data Parity Detected (Not supported)**

Hardwired to zero.