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Email & Skype: info@chipsmall.com Web: www.chipsmall.com
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Winbond
LPC I/O
W83637HF
W83637HG

Revision: 1.6 Date: 2006/03/22

Winbond Electronics Corp.

Revision History

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2		08/09/2001	0.60	First published.
3		02/18/2002	0.70	Update Chapter 10. (Hardware Monitor Device)
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5		09/27/2002	1.1	ADD Secure Digital Function Description
6	7 100~101	04/15/2003	1.2	ADD Block Digram ADD Chapter 4.1 Plug and Play Configuration
7	130~137	06/25/2003	1.3	Add Chapter 9 DC Specification
8	N.A.	11/23/2005	1.4	Add Pb-free package
9	N.A.	02/10/2006	1.5	Remove 5VSB H/W monitor sensor function.
10	Page.5	03/23/2006	1.6	Correct GPIO pins to 21-pin, not 40-pin

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

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Winbond Electronics Corp.

1. GENERAL DESCRIPTION

W83637HF/HG is the new generation of Winbond's LPC I/O products. It is an evolving product from Winbond's most popular LPC I/O chip W83627HF/HG – which integrates the disk driver adapter, serial port (UART), keyboard controller (KBC), SIR, CIR, game port, MIDI port, hardware monitor, ACPI, On Now Wake-Up – plus additional new features: the Smart Card reader interface and Memory Stick ™ reader interface.

The Smart Card application is gaining more and more attention; it provides a very high-grade security and convenience in Internet transaction, banking, telephony, electronic payments, etc. W83637HF/HG supports a smart card reader interface featuring Smart wake-up function. This smart card reader interface fully meets the ISO7816 and PC/SC (Personal Computer/Smart Card Workgroup) standards. W83637HF/HG provides a minimum external components and lowest cost solution for smart card applications.

W83637HF/HG implements a standard Memory Stick™ reader interface. The Memory Stick™ has been a new mainstream media for storing and transferring data. It's ultra-small size and high storage capacity make it can be used in very wide variety products, including the Audio, Video and PC.

The disk drive adapter functions of W83637HF/HG include a floppy disk drive controller compatible with the industry standard 82077/765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. The wide range of functions integrated onto the W83637HF/HG greatly reduces the number of components required for interfacing with floppy disk drives. W83637HF/HG supports four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s, 1 Mb/s, and 2 Mb/s.

W83637HF/HG provides two high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupts system. Both UARTs provide legacy speed with baud rate up to 115.2k bps and also advanced speed with baud rates of 230k, 460k, or 921k bps, which support higher speed modems. In addition, W83637HF/HG provides IR functions: IrDA 1.0 (SIR for 1.152K bps) and TV remote IR (Consumer IR, supporting NEC, RC-5, extended RC-5, and RECS-80 protocols).

W83637HF/HG supports one PC-compatible printer port (SPP), Bi-directional Printer port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). Through the printer port interface pins, also available are: Extension FDD Mode and Extension 2FDD Mode allowing one or two external floppy disk drives to be connected.

The configuration registers support mode selection, function enable/disable, and power down function selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature demand of Windows 95/98™, which makes system resource allocation more efficient than ever.

W83637HF/HG provides functions that comply with ACPI (*Advanced Configuration and Power Interface*), which includes support of legacy and ACPI power management through PME# or PSOUT# function pins. For OnNow keyboard Wake-Up, OnNow mouse Wake-Up, and OnNow CIR Wake-Up. W83637HF/HG also has auto power management to reduce the power consumption.

The keyboard controller is based on 8042 compatible instruction set with a 2K Byte programmable ROM and a 256-Byte RAM bank. Keyboard BIOS firmware are available with optional AMIKEY™ -2, Phoenix MultiKey/42™, or customer code.

W83637HF/HG provides a set of flexible I/O control functions to the system designer through a set of General Purpose I/O port. These GPIO ports may serve as simple I/O or may be individually configured to provide a predefined alternate function.

W83637HF/HG is made to fully comply with Microsoft PC98 and PC99 Hardware Design Guide. Moreover, W83637HF/HG is made to meet the specification of PC2001's requirement in the power management: ACPI 1.0/1.0b/2.0 and DPM (Device Power Management).

W83637HF/HG contains a game port and a MIDI port. The game port is designed to support 2 joysticks and can be applied to all standard PC game control devices. They are very important for an entertainment or consumer computer.

W83637HF/HG supports hardware status monitoring for personal computers. It can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system to work stably and properly. Moreover, W83637HF/HG support the Smart Fan control system, including the "Thermal Cruise™" and "Speed Cruise™" functions. Smart Fan can make system more stable and user friendly.

2. FEATURES

General

- Meet LPC Spec. 1.01
- Support LDRQ#(LPC DMA), SERIRQ (serial IRQ)
- Compliant with Microsoft PC2000/PC2001 Hardware Design Guide
- Support DPM (Device Power Management), ACPI
- Programmable configuration settings
- Single 24 or 48 MHz clock input

FDC

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- Support vertical recording format
- DMA enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detects all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD write enable signal (write data signal was forced to be inactive)
- Support up to four 3.5-inch or 5.25-inch floppy disk drives
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support 3-mode FDD, and its Win95/98 driver

UART

- Two high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs
- MIDI compatible
- Fully programmable serial-interface characteristics:
  - --- 5, 6, 7 or 8-bit characters
  - --- Even, odd or no parity bit generation/detection
  - --- 1, 1.5 or 2 stop bits generation
- Internal diagnostic capabilities:
  - --- Loop-back controls for communications link fault isolation
  - --- Break, parity, overrun, framing error simulation
- Programmable baud generator allows division of 1.8461 MHz and 24 MHz by 1 to (2^{16}-1)
- Maximum baud rate up to 921k bps for 14.769 MHz and 1.5M bps for 24 MHz

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps
- Support Consumer IR

Parallel Port

- Compatible with IBM parallel port
- Support PS/2 compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- Extension FDD mode supports disk drive B; and Extension 2FDD mode supports disk drives A and B through parallel port
- Enhanced printer port back-drive current protection

Keyboard Controller

- 8042 based with optional F/W from AMIKKEY™-2, Phoenix MultiKey/42™ or customer code with 2K bytes of programmable ROM, and 256 bytes of RAM
- Asynchronous Access to Two Data Registers and One status Register
- Software compatibility with the 8042
- Support PS/2 mouse
- Support port 92
- Support both interrupt and polling modes
- Fast Gate A20 and Hardware Keyboard Reset
- 8 Bit Timer/ Counter
- Support binary and BCD arithmetic
- 6 MHz, 8 MHz, 12 MHz, or 16 MHz operating frequency

Game Port

- Support two separate Joysticks
- Support every Joystick two axis (X, Y) and two button (A, B) controllers

MIDI Port

- The baud rate is 31.25 K baud
- 16-byte input FIFO
- 16-byte output FIFO

General Purpose I/O Ports

- 21 programmable general purpose I/O ports
- General purpose I/O ports can serve as simple I/O ports, interrupt steering inputs, watching dog timer output, power LED output, infrared I/O pins, KBC control I/O pins, suspend LED output, RSMRST# signal, PWROK signal, STR (suspend to DRAM) function, VID control function,

OnNow Functions

- Keyboard Wake-Up by programmable keys
- Mouse Wake-Up by programmable buttons
- CIR Wake-Up by programmable keys
- SMART Card Wake-up by SCPSNT
- On Now Wake-Up from all of the ACPI sleeping states (S1-S5)

Smart Card Reader Interface

- PC/SC T=0, T=1 compliant
- ISO7816 protocol compliant
- With 16-byte send/receive FIFOs
- Programmable baud generator
- Standard drivers for Windows 98 ME™, Windows 2000™

Memory Stick™ Reader Interface

- Meet SONY Memory Stick™ Specification Version 1.03

Hardware Monitor Functions

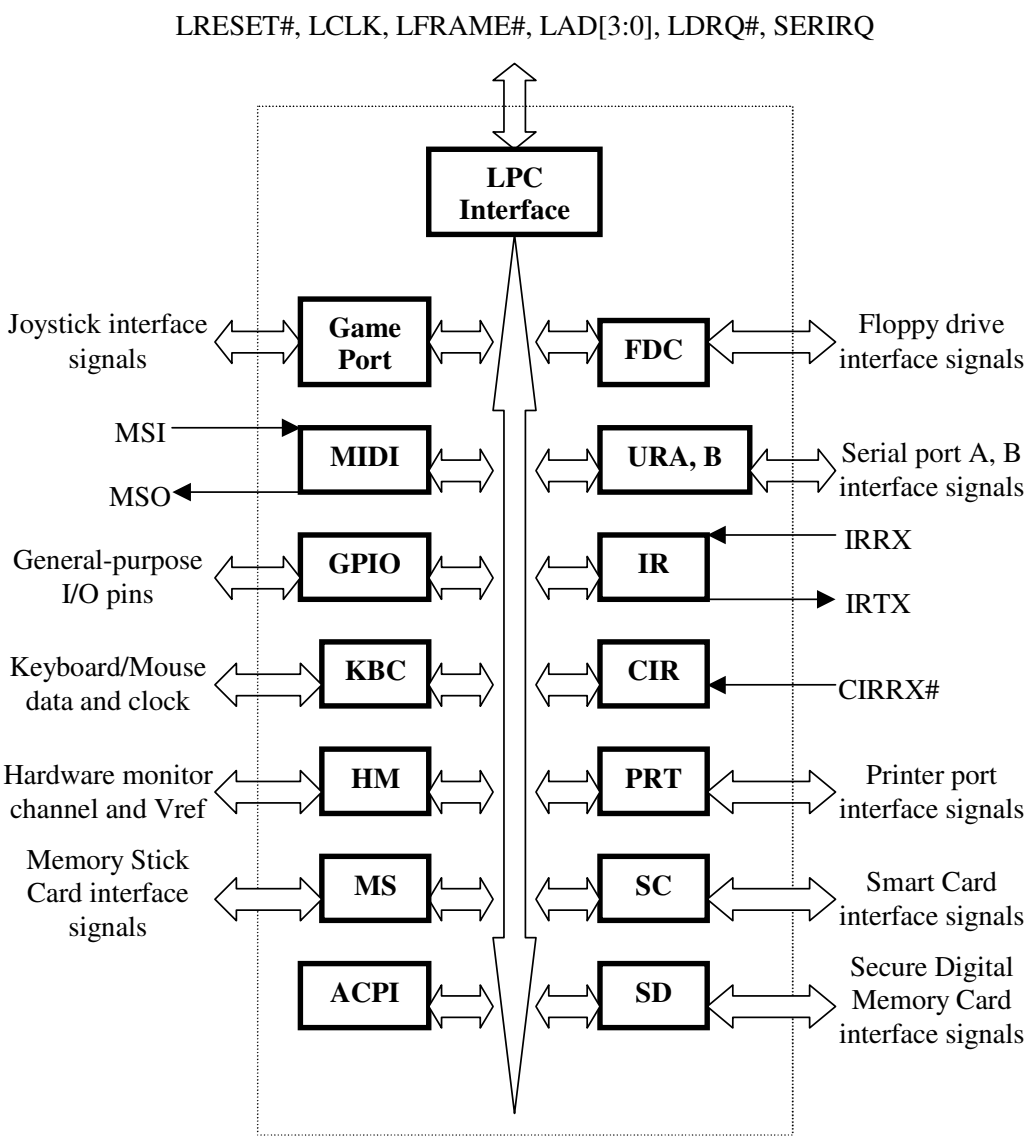
- Smart fan control system, support "Thermal Cruise™" and "Speed Cruise™"
- 3 thermal inputs from optionally remote thermistors or 2N3904 transistors or Pentium™ II/III/4 thermal diode output
- 3 positive voltage inputs (typical for +5V, +3.3V, Vcore)
- 1 intrinsic voltage monitoring (typical for Vbat)
- 3 fan speed monitoring inputs
- 3 fan speed control
- Build in Case open detection circuit
- WATCHDOG comparison of all monitored values
- Programmable hysteresis and setting points for all monitored items
- Over temperature indicate output

- Automatic Power On voltage detection Beep
- Issue SMI#, IRQ, OVT# to activate system protection
- Winbond Hardware Doctor™ Support
- Intel LDCM™ / Acer ADM™ compatible

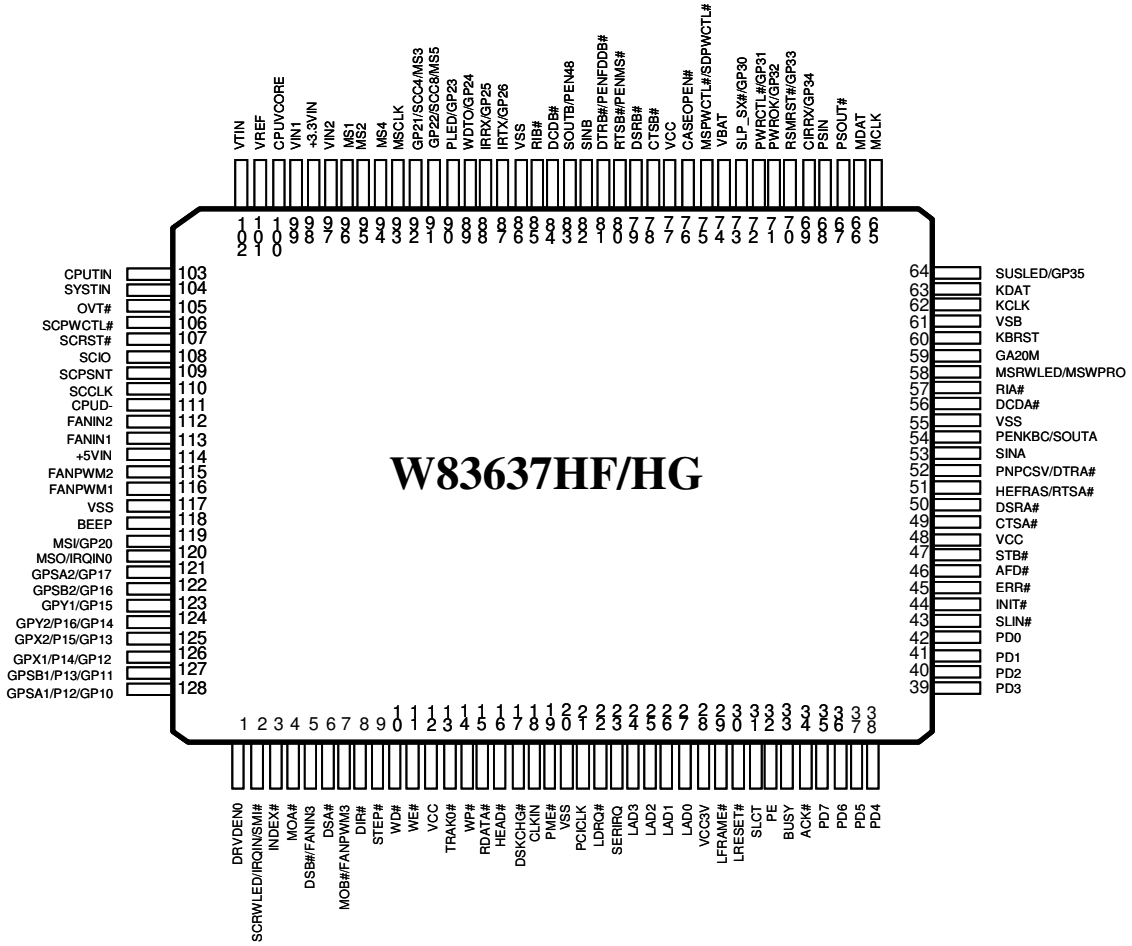
Package

- 128-pin PQFP

3. BLOCK DIAGRAM



4. PIN CONFIGURATION



5. PIN DESCRIPTION

PIN DESCRIPTION	
I/O12t	TTL level bi-directional pin with 12 mA source-sink capability.
I/O24t	TTL level bi-directional pin with 24 mA source-sink capability.
I/O12ts	TTL level Schmitt-trigger bi-directional pin with 12 mA source-sink capability.
I/O24ts	TTL level Schmitt-trigger bi-directional pin with 24 mA source-sink capability.
I/OD12t	TTL level bi-directional pin and open drain output with 12 mA sink capability.
I/OD24t	TTL level bi-directional pin and open drain output with 24 mA sink capability.
I/OD12ts	TTL level Schmitt-trigger bi-directional pin and open drain output with 12 mA sink capability.
I/OD24ts	TTL level Schmitt-trigger bi-directional pin and open drain output with 24 mA sink capability.
I/OD12cs	CMOS level Schmitt-trigger bi-directional pin and open drain output with 12 mA sink capability.
I/OD16cs	CMOS level Schmitt-trigger bi-directional pin and open drain output with 16 mA sink capability.
I/OD12csd	CMOS level Schmitt-trigger bi-directional pin with internal pull down resistor and open drain output with 12 mA sink capability.
I/OD12csu	CMOS level Schmitt-trigger bi-directional pin with internal pull up resistor and open drain output with 12 mA sink capability.
O4t	TTL level output pin with 4 mA source-sink capability.
O12t	TTL level output pin with 12 mA source-sink capability.
O16t	TTL level output pin with 16 mA source-sink capability.
O24t	TTL level output pin with 24 mA source-sink capability.
O24ts	TTL level Schmitt-trigger output pin with 24 mA source-sink capability.
OD12t	TTL level open drain output pin with 12 mA sink capability.
OD24t	TTL level open drain output pin with 24 mA sink capability.
O8c	CMOS level output pin with 8 mA source-sink capability.
INt	TTL level input pin.
INts	TTL level Schmitt-trigger input pin.
INtu	TTL level input pin with internal pull up resistor.
INc	CMOS level input pin.
INcd	CMOS level input pin with internal pull down resistor.
INcsu	CMOS level Schmitt-trigger input pin with internal pull up resistor.

5.1 LPC Interface

SYMBOL	PIN	I/O	FUNCTION
CLKIN	18	IN_t	System clock input. According to the input frequency 24MHz or 48MHz, it is selectable through register. Default is 24MHz input.
PME#	19	OD_{12t}	Generated PME event.
PCICLK	21	IN_{ts}	PCI clock input.
LDRQ#	22	O_{12t}	Encoded DMA Request signal.
SERIRQ	23	I/O_{12t}	Serial IRQ input/Output.
LAD[3:0]	24-27	I/O_{12t}	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
LFRAME#	29	IN_{ts}	Indicates start of a new cycle or termination of a broken cycle.
LRESET#	30	IN_{ts}	Reset signal. It can connect to PCIRST# signal on the host.

5.2 FDC Interface

SYMBOL	PIN	I/O	FUNCTION
DRVDEN0	1	OD_{24t}	Drive Density Select bit 0.
INDEX#	3	IN_{csu}	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
MOA#	4	OD_{24t}	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
DSB# FANIN3	5	OD_{24t} I/O24ts	Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output. 0V to +5V amplitude fan tachometer input
DSA#	6	OD_{24t}	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
MOB# FANPWM3	7	OD_{24t} OD_{24t}	Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output. Fan speed control. Use the Pulse Width Modulation (**PWM**) technical knowledge to control the Fan's RPM.
DIR#	8	OD_{24t}	Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
STEP#	9	OD_{24t}	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
WD#	10	OD_{24t}	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
WE#	11	OD_{24t}	Write enable. An open drain output.
TRACK0#	13	IN_{csu}	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
WP#	14	IN_{csu}	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
RDATA#	15	IN_{csu}	The read data input signal from the FDD. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
HEAD#	16	OD_{24t}	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1

FDC Interface, continued

SYMBOL	PIN	I/O	FUNCTION
DSKCHG#	17	IN_{csu}	Diskette change. This signal is active low at power on and whenever the diskette is removed. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).

5.3 Multi-Mode Parallel Port

The following pins have alternate functions, which are controlled by CR28 and L3-CRF0.

SYMBOL	PIN	I/O	FUNCTION
SLCT WE2#	31	IN_{ts} OD_{12t}	PRINTER MODE: An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: WE2# This pin is for Extension FDD B; its function is the same as the WE# pin of FDC. EXTENSION 2FDD MODE: WE2# This pin is for Extension FDD A and B; its function is the same as the WE# pin of FDC.
PE WD2#	32	IN_{ts} OD_{12t}	PRINTER MODE: An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: WD2# This pin is for Extension FDD B; its function is the same as the WD# pin of FDC. EXTENSION 2FDD MODE: WD2# This pin is for Extension FDD A and B; its function is the same as the WD# pin of FDC.
BUSY MOB2#	33	IN_{ts} OD_{12t}	PRINTER MODE: An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: MOB2# This pin is for Extension FDD B; its function is the same as the MOB# pin of FDC. EXTENSION 2FDD MODE: MOB2# This pin is for Extension FDD A and B; its function is the same as the MOB# pin of FDC.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
ACK#	34	IN_{ts}	PRINTER MODE: ACK# An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DSB2#		OD_{12t}	EXTENSION FDD MODE: DSB2# This pin is for the Extension FDD B; its functions is the same as the DSB# pin of FDC. EXTENSION 2FDD MODE: DSB2# This pin is for Extension FDD A and B; its function is the same as the DSB# pin of FDC.
PD7	35	I/O_{12ts}	PRINTER MODE: PD7 Parallel port data bus bit 7. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DSA2#		OD_{12t}	EXTENSION FDD MODE: This pin is a tri-state output. EXTENSION 2FDD MODE: DSA2# This pin is for Extension FDD A; its function is the same as the DSA# pin of FDC.
PD6	36	I/O_{12ts}	PRINTER MODE: PD6 Parallel port data bus bit 6. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
MOA2#		OD_{12t}	EXTENSION FDD MODE: This pin is a tri-state output. EXTENSION. 2FDD MODE: MOA2# This pin is for Extension FDD A; its function is the same as the MOA# pin of FDC.
PD5	37	I/O_{12ts}	PRINTER MODE: PD5 Parallel port data bus bit 5. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: This pin is a tri-state output. EXTENSION 2FDD MODE: This pin is a tri-state output.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
PD4 DSKCHG2#	38	I/O_{12ts} IN_{ts}	PRINTER MODE: PD4 Parallel port data bus bit 4. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: DSKCHG2# This pin is for Extension FDD B; the function of this pin is the same as the DSKCHG# pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: DSKCHG2# This pin is for Extension FDD A and B; this function of this pin is the same as the DSKCHG# pin of FDC. It is pulled high internally.
PD3 RDATA2#	39	I/O_{12ts} IN_{ts}	PRINTER MODE: PD3 Parallel port data bus bit 3. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: RDATA2# This pin is for Extension FDD B; its function is the same as the RDATA# pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: RDATA2# This pin is for Extension FDD A and B; its function is the same as the RDATA# pin of FDC. It is pulled high internally.
PD2 WP2#	40	I/O_{12ts} IN_{ts}	PRINTER MODE: PD2 Parallel port data bus bit 2. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: WP2# This pin is for Extension FDD B; its function is the same as the WP# pin of FDC. It is pulled high internally. EXTENSION. 2FDD MODE: WP2# This pin is for Extension FDD A and B; its function is the same as the WP# pin of FDC. It is pulled high internally.
PD1 TRAK02#	41	I/O_{12ts} IN_{ts}	PRINTER MODE: PD1 Parallel port data bus bit 1. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: TRAK02# This pin is for Extension FDD B; its function is the same as the TRAK0# pin of FDC. It is pulled high internally. EXTENSION. 2FDD MODE: TRAK02# This pin is for Extension FDD A and B; its function is the same as the TRAK0# pin of FDC. It is pulled high internally.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
PD0	42	I/O_{12ts}	PRINTER MODE: PD0 Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
INDEX2#		IN_{ts}	EXTENSION FDD MODE: INDEX2# This pin is for Extension FDD B; its function is the same as the INDEX# pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: INDEX2# This pin is for Extension FDD A and B; its function is the same as the INDEX# pin of FDC. It is pulled high internally.
SLIN#	43	OD_{12t}	PRINTER MODE: SLIN# Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
STEP2#		OD_{12t}	EXTENSION FDD MODE: STEP2# This pin is for Extension FDD B; its function is the same as the STEP# pin of FDC. EXTENSION 2FDD MODE: STEP2# This pin is for Extension FDD A and B; its function is the same as the STEP# pin of FDC.
INIT#	44	OD_{12t}	PRINTER MODE: INIT# Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DIR2#		OD_{12t}	EXTENSION FDD MODE: DIR2# This pin is for Extension FDD B; its function is the same as the DIR# pin of FDC. EXTENSION 2FDD MODE: DIR2# This pin is for Extension FDD A and B; its function is the same as the DIR# pin of FDC.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
ERR#	45	IN_{ts}	PRINTER MODE: ERR# An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
HEAD2#		OD_{12t}	EXTENSION FDD MODE: HEAD2# This pin is for Extension FDD B; its function is the same as the HEAD# pin of FDC. EXTENSION 2FDD MODE: HEAD2# This pin is for Extension FDD A and B; its function is the same as the HEAD# pin of FDC.
AFD#	46	OD_{12t}	PRINTER MODE: AFD# An active low output from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DRVDEN0		OD_{12t}	EXTENSION FDD MODE: DRVDEN0 This pin is for Extension FDD B; its function is the same as the DRVDEN0 pin of FDC. EXTENSION 2FDD MODE: DRVDEN0 This pin is for Extension FDD A and B; its function is the same as the DRVDEN0 pin of FDC.
STB#	47	OD_{12t}	PRINTER MODE: STB# An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: This pin is a tri-state output EXTENSION 2FDD MODE: This pin is a tri-state output.

5.4 Serial Port Interface

SYMBOL	PIN	I/O	FUNCTION
CTSA# CTSB#	49 78	IN_t	Clear To Send. It is the modem control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
DSRA# DSRB#	50 79	IN_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
RTSA# HEFRAS	51	O_{8c} INcd	UART A Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. During power-on reset, this pin is pulled down internally and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). A 4.7 kΩ is recommended if intends to pull up. (select 4EH as configuration I/O port's address)
RTSB# ENGMTO	80	O_{8c} INcd	UART B Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. Watch Dog Time-Out enable.
DTRA PNPCVS	52	O_{8c} INcd	UART A Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate. During power-on reset, this pin is pulled down internally and is defined as PNPCVS, which provides the power-on value for CR24 bit 0 (PNPCVS). A 4.7 kΩ is recommended if intends to pull up. (clear the default value of FDC, UARTs, PRT, Game port and MIDI port)

Serial Port Interface, continued

SYMBOL	PIN	I/O	FUNCTION
DTRB#	81	O_{8c}	UART B Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
SINA SINB	53 82	IN_t	Serial Input. It is used to receive serial data through the communication link.
SOUTA PENKBC	54	O_{8c} IN_{cd}	UART A Serial Output. It is used to transmit serial data out to the communication link. During power-on reset, this pin is pulled down internally and is defined as PENKBC, which provides the power-on value for CR24 bit 2 (PENKBC). A 4.7 kΩ resistor is recommended if intends to pull up. (enable KBC)
SOUTB PEN48	83	O_{8c} IN_{cd}	UART B Serial Output. During power-on reset, this pin is pulled down internally and is defined as PEN48, which provides the power-on value for CR24 bit 6 (EN48). A 4.7 kΩ resistor is recommended if intends to pull up.
DCDA# DCDB#	56 84	IN_t	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
RIA# RIB#	57 85	IN_t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.

5.5 KBC Interface

SYMBOL	PIN	I/O	FUNCTION
GA20M	59	O_{16t}	Gate A20 output. This pin is high after system reset. (KBC P21)
KBRST	60	O_{16t}	Keyboard reset. This pin is high after system reset. (KBC P20)
KCLK	62	I/OD_{16cs}	Keyboard Clock.
KDAT	63	I/OD_{16cs}	Keyboard Data.
MCLK	65	I/OD_{16cs}	PS2 Mouse Clock.
MDAT	66	I/OD_{16cs}	PS2 Mouse Data.

5.6 ACPI Interface

SYMBOL	PIN	I/O	FUNCTION
PSOUT#	67	OD_{12t}	Panel Switch Output. This signal is used for Wake-Up system from $S5_{cold}$ state. This pin is pulse output, active low.
PSIN	68	IN_{cd}	Panel Switch Input. This pin is high active with an internal pull down resistor.
VBAT	74	pvdf_rc1000_vbat	Battery voltage input.

5.7 Hardware Monitor Interface

SYMBOL	PIN	I/O	FUNCTION
CASEOPEN#	76	IN_t	CASE OPEN. An active low input from an external device when case is opened. This signal can be latched if pin VBAT is connect to battery, even W83637HF is power off.
VIN2	97	AIN	0V to 4.096V FSR Analog Inputs.
VIN1	99	AIN	0V to 4.096V FSR Analog Inputs.
CPUVCORE	100	AIN	0V to 4.096V FSR Analog Inputs.
VREF	101	AOUT	Reference Voltage for temperature maturation.
VTIN	102	AIN	Temperature sensor 3 inputs. It is used for temperature maturation.
CPUTIN	103	AIN	Temperature sensor 2 inputs. It is used for CPU1 temperature maturation.
SYSTIN	104	AIN	Temperature sensor 1 input. It is used for system temperature maturation.
OVT# SMI#	105	OD_{24t}	Over temperature Shutdown Output. It indicated the temperature is over temperature limit. System Management Interrupt channel input.
FANIN2 FANIN1	112 113	I/O_{12ts}	0V to +5V amplitude fan tachometer input.
FANPWM1 FANPWM2	116 115	O_{12t} (OD_{12t})	Fan speed control. Use the Pulse Width Modulation (PWM) technical knowledge to control the Fan's RPM.
BEEP	118	OD_{12t}	Beep function for hardware monitor. This pin is low after system reset.

5.8 Game Port & MIDI Port

SYMBOL	PIN	I/O	FUNCTION
MSI	119	INtu	MIDI serial data input .(Default)
GP20		I/OD_{12t}	General purpose I/O port 2 bit 0.
MSO	120	O_{8c}	MIDI serial data output. (Default)
IRQIN0		INc	Alternate Function input: Interrupt channel input.
GPSA2	121	Incsu	Active-low, Joystick I switch input 2. This pin has an internal pull-up resistor. (Default)
GP17		I/OD_{12csu}	General purpose I/O port 1 bit 7.
GPSB2	122	Incsu	Active-low, Joystick II switch input 2. This pin has an internal pull-up resistor. (Default)
GP16		I/OD_{12csu}	General purpose I/O port 1 bit 6.
GPY1	123	I/OD_{12csd}	Joystick I timer pin. This pin connects to Y positioning variable resistors for the Joystick. (Default)
GP15		I/OD_{12cs}	General purpose I/O port 1 bit 5.
GPY2	124	I/OD_{12csd}	Joystick II timer pin. This pin connects to Y positioning variable resistors for the Joystick. (Default)
GP14		I/OD_{12cs}	General purpose I/O port 1 bit 4.
P16			Alternate Function Output: KBC P16 I/O port.
GPX2	125	I/OD_{12csd}	Joystick II timer pin. This pin connects to X positioning variable resistors for the Joystick. (Default)
GP13		I/OD_{12cs}	General purpose I/O port 1 bit 3.
P15			Alternate Function Output: KBC P15 I/O port.
GPX1	126	I/OD_{12csd}	Joystick I timer pin. This pin connects to X positioning variable resistors for the Joystick. (Default)
GP12		I/OD_{12cs}	General purpose I/O port 1 bit 2.
P14			Alternate Function Output: KBC P14 I/O port.
GPSB1	127	Incsu	Active-low, Joystick II switch input 1. (Default)
GP11		I/OD_{12csu}	General purpose I/O port 1 bit 1.
P13			Alternate Function Output: KBC P13 I/O port.
GPSA1	128	Incsu	Active-low, Joystick I switch input 1. (Default)
GP10		I/OD_{12csu}	General purpose I/O port 1 bit 0.
P12			Alternate Function Output: KBC P12 I/O port.