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WINBOND LPC I/O

W83697UF

W83697UG

Date: May 26, 2005 Revision: A1

Table of Contents-

1. GENERAL DESCRIPTION 4
2. FEATURES 5
3. BLOCK DIAGRAM FOR W83697UF 7
4. PIN CONFIGURATION FOR W83697UF 8
5. PIN DESCRIPTION 9
   - 5.1 LPC Interface 10
   - 5.2 FDC Interface 11
   - 5.3 Multi-Mode Parallel Port 12
   - 5.4 Serial Port Interface 17
   - 5.5 Infrared Port 18
   - 5.6 Flash ROM Interface 19
   - 5.7 General Purpose I/O Port 19
   - 5.8 Smart Card Interface 20
   - 5.9 PWM & General Purpose I/O Port 8 21
   - 5.10 Game Port & MIDI Port 21
   - 5.11 POWER PINS 22
6. CONFIGURATION REGISTER 22
   - 6.1 Plug and Play Configuration 22
   - 6.2 Compatible PnP 23
     - 6.2.1 Extended Function Registers 23
     - 6.2.2 Extended Functions Enable Registers (EFERs) 23
     - 6.2.3 Extended Function Index Registers (EFIRs), Extended Function Data Registers (EFDRs) 23
   - 6.3 Configuration Sequence 23
     - 6.3.1 Enter the extended function mode 24
     - 6.3.2 Configurate the configuration registers 24
     - 6.3.3 Exit the extended function mode 24
     - 6.3.4 Software programming example 24
   - 6.4 Chip (Global) Control Register 25
   - 6.5 Logical Device 0 (FDC) 31
   - 6.6 Logical Device 1 (Parallel Port) 34
   - 6.7 Logical Device 2 (UART A) 35
   - 6.8 Logical Device 3 (UART B) 36
   - 6.9 Logical Device 7 (Game Port and GPIO Port 1) 38
   - 6.10 Logical Device 8 (MIDI Port and GPIO Port 5) 38
   - 6.11 Logical Device 9 (GPIO Port 2 ~ GPIO Port 4) 40
   - 6.12 Logical Device A (ACPI) 41

6.13 Logical Device B (PWM) 46
6.14 Logical Device C (SMART CARD) 46
6.15 Logical Device D (URC & GPIO Port 6) 46
6.16 Logical Device E (URD & GPIO Port 7) 48
6.17 Logical Device F (GPIO Port 8) 49
7. SPECIFICATIONS 49
7.1 Absolute Maximum Ratings 49
7.2 DC CHARACTERISTICS 50
8. APPLICATION CIRCUITS 58
8.1 Parallel Port Extension FDD 58
8.2 Parallel Port Extension 2FDD 59
8.3 Four FDD Mode 59
9. ORDERING INSTRUCTION 60
10. HOW TO READ THE TOP MARKING 60
11. PACKAGE DIMENSIONS 61
12. APPENDIX A: DEMO CIRCUIT 62
13. REVISION HISTORY 67

1. GENERAL DESCRIPTION

The W83697UF is evolving product from Winbond's most popular I/O family. They feature a whole new interface, namely LPC (Low Pin Count) interface, which will be supported in the new generation chip-set. This interface as its name suggests is to provide an economical implementation of I/O's interface with lower pin count and still maintains equivalent performance as its ISA interface counterpart. Approximately 40 pin counts are saved in LPC I/O comparing to ISA implementation. With this additional freedom, we can implement more devices on a single chip as demonstrated in W83697UF's integration of Game Port and MIDI Port. It is fully transparent in terms of software which means no BIOS or device driver update is needed except chip-specific configuration.

The disk drive adapter functions of W83697UF include a floppy disk drive controller compatible with the industry standard 82077/ 765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. The wide range of functions integrated onto the W83697UF greatly reduces the number of components required for interfacing with floppy disk drives. The W83697UF supports four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data tranufer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s,1 Mb/s, and 2 Mb/s.

The W83697UF provides four high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. All UARTs provide legacy speed with baud rate up to 115.2k bps and also advanced speed with baud rates of **230k**, **460k**, or **921k bps** which support higher speed modems. In addition, the W83697UF provides IR functions: **IrDA 1.0** (**SIR** for 1.152K bps) and TV remote IR (**Consumer IR**, supporting NEC, RC-5, extended RC-5, and RECS-80 protocols).

The W83697UF supports one PC-compatible printer port (SPP), Bi-directional Printer port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). Through the printer port interface pins, also available are: Extension FDD Mode and Extension 2FDD Mode allowing one or two external floppy disk drives to be connected.

The configuration registers support mode selection, function enable/disable, and power down function selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature demand of Windows 95/98™, which makes system resource allocation more efficient than ever.

The W83697UF provides a set of flexible I/O control functions to the system designer through a set of General Purpose I/O ports. These GPIO ports may serve as simple I/O or may be individually configured to provide a predefined alternate function. General Purpose Port 1 is designed to be functional even in power down mode (VCC is off).

The W83697UF is made to fully comply with **Microsoft© PC98 and PC99 Hardware Design Guide, and meet the requirements of ACPI.**

The W83697UF contains a game port and a MIDI port. The game port is designed to support 2 joysticks and can be applied to all standard PC game control devices. They are very important for a entertainment or consumer computer.

The W83697UF provides Flash ROM interface. That can support up to 4M legacy flash ROM.

2. FEATURES

General

- Meet LPC Spec. 1.1
- Support LDRQ#(LPC DMA), SERIRQ (serial IRQ)
- Include all the features of Winbond I/O W83877TF
- Integrate Smart Card functions
- Compliant with Microsoft PC98/PC99 Hardware Design Guide
- Support DPM (Device Power Management), ACPI
- Programmable configuration settings
- Single 24 or 48 MHz clock input

FDC

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- Support vertical recording format
- DMA enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detects all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD write enable signal (write data signal was forced to be inactive)
- Support up to four 3.5-inch or 5.25-inch floppy disk drives
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support **3-mode FDD, and its Win95/98 driver**

UART

- Four high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs
- MIDI compatible
- Fully programmable serial-interface characteristics:
  --- 5, 6, 7 or 8-bit characters
  --- Even, odd or no parity bit generation/detection
  --- 1, 1.5 or 2 stop bits generation
- Internal diagnostic capabilities:
  --- Loop-back controls for communications link fault isolation
  --- Break, parity, overrun, framing error simulation

- Programmable baud generator allows division of 1.8461 MHz and 24 MHz by 1 to (2^{16}-1)
- Maximum baud rate up to **921k bps** for 14.769 MHz and 1.5M bps for 24 MHz

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps
- Support Consumer IR with Wake-Up function.

Parallel Port

- Compatible with IBM parallel port
- Support PS/2 compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- Extension FDD mode supports disk drive B; and Extension 2FDD mode supports disk drives A and B through parallel port
- Enhanced printer port back-drive current protection

Game Port

- Support two separate Joysticks
- Support every Joystick two axes (X,Y) and two buttons (S1,S2) controllers

MIDI Port

- The baud rate is 31.25 Kbaud
- 16-byte input FIFO
- 16-byte output FIFO

Flash ROM Interface

- Support up to 4M flash ROM

Fan Speed Control

- Support 3 sets of PWM Fan Speed Control

General Purpose I/O Ports

- 60 programmable general purpose I/O ports
- General purpose I/O ports can serve as simple I/O ports, watch dog timer output, power LED output, infrared I/O pins, suspend LED output, Beep output
- Functional in power down mode

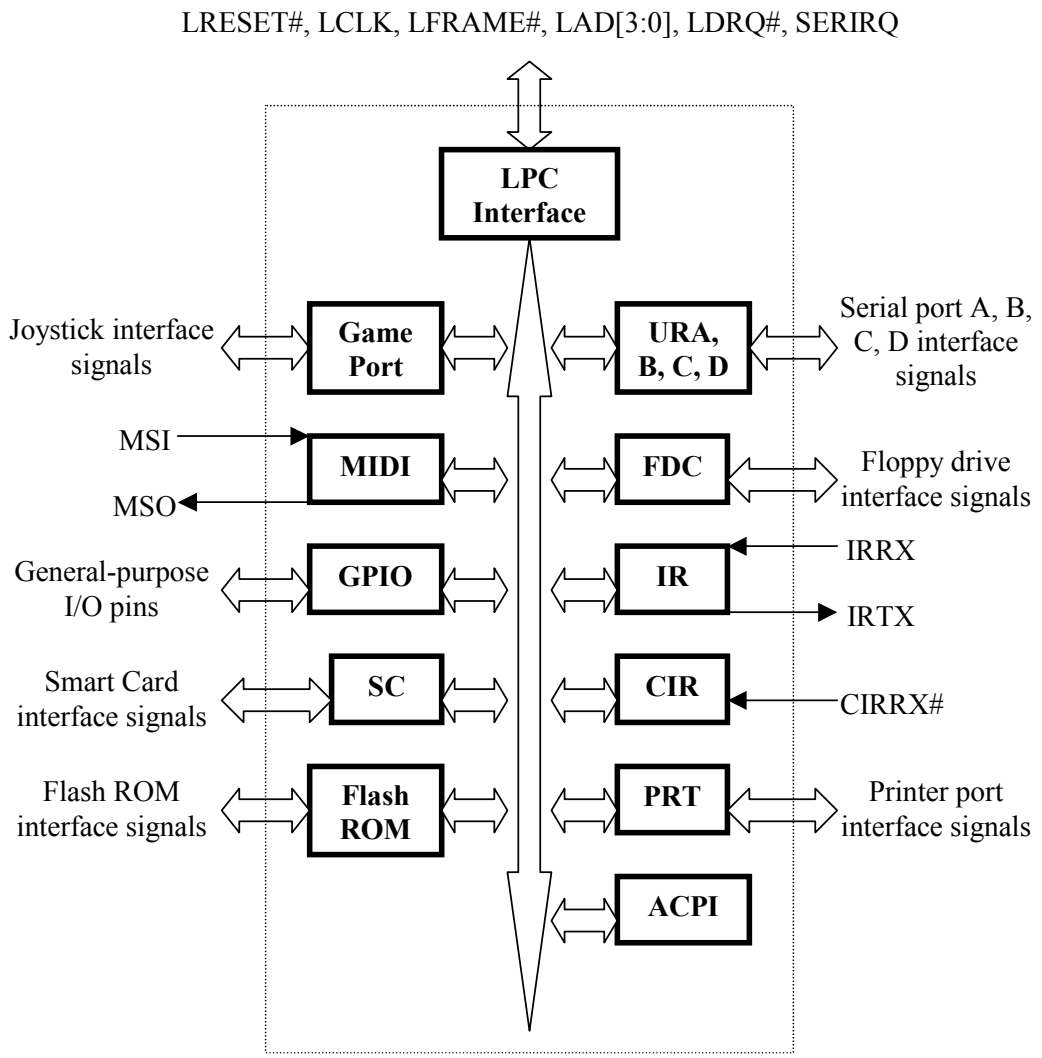
Smart Card Reader Interface

- ISO7816 protocol compliant
- PC/SC T=0 , T=1 compliant

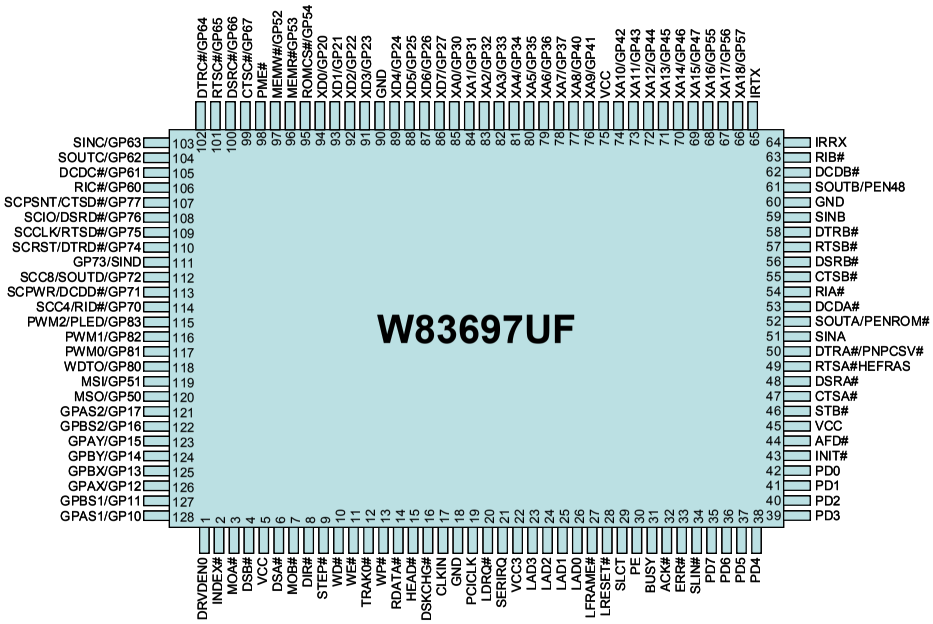
Package

- 128-pin PQFP

3. BLOCK DIAGRAM FOR W83697UF



4. PIN CONFIGURATION FOR W83697UF



5. PIN DESCRIPTION

Note: Please refer to Section DC CHARACTERISTICS for details

PIN DESCRIPTION	
I/O8t	TTL level bi-directional pin with 8mA source-sink capability
I/O12t	TTL level bi-directional pin with 12mA source-sink capability
I/O24t	TTL level bi-directional pin with 24 mA source-sink capability
I/O12tp3	3.3V TTL level bi-directional pin with 12mA source-sink capability
I/O12ts	TTL level Schmitt-trigger bi-directional pin with 12mA source-sink capability
I/O24ts	TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability
I/O24tsp3	3.3V TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability
I/OD12t	TTL level bi-directional pin and open-drain output with 12mA sink capability
I/OD24t	TTL level bi-directional pin and open-drain output with 24mA sink capability
I/OD24c	CMOS level bi-directional pin and open-drain output with 24mA sink capability
I/OD24a	Bi-directional pin with analog input and open-drain output with 24mA sink capability
I/OD12ts	TTL level Schmitt-trigger bi-directional pin and open-drain output with 12mA sink capability
I/OD24ts	TTL level Schmitt-trigger bi-directional pin and open-drain output with 24mA sink capability
I/OD12cs	CMOS level Schmitt-trigger bi-directional pin and open-drain output with 12mA sink capability
I/OD16cs	CMOS level Schmitt-trigger bi-directional pin and open-drain output with 16mA sink capability
I/OD24cs	CMOS level Schmitt-trigger bi-directional pin and open-drain output with 24mA sink capability
I/OD12csd	CMOS level Schmitt-trigger bi-directional pin with internal pull down resistor and open-drain output with 12mA sink capability
I/OD12csu	CMOS level Schmitt-trigger bi-directional pin with internal pull up resistor and open-drain output with 12mA sink capability
O4	Output pin with 4 mA source-sink capability
O8	Output pin with 8 mA source-sink capability
O12	Output pin with 12 mA source-sink capability
O16	Output pin with 16 mA source-sink capability
O24	Output pin with 24 mA source-sink capability
O12p3	3.3V output pin with 12 mA source-sink capability

Pin description, continued

PIN DESCRIPTION	
O_{24p3}	3.3V output pin with 24 mA source-sink capability
OD_{12}	Open-drain output pin with 12 mA sink capability
OD_{24}	Open-drain output pin with 24 mA sink capability
OD_{12p3}	3.3V open-drain output pin with 12 mA sink capability
IN_{t}	TTL level input pin
IN_{tp3}	3.3V TTL level input pin
IN_{td}	TTL level input pin with internal pull down resistor
IN_{tu}	TTL level input pin with internal pull up resistor
IN_{ts}	TTL level Schmitt-trigger input pin
IN_{tsp3}	3.3V TTL level Schmitt-trigger input pin
IN_{c}	CMOS level input pin
IN_{cu}	CMOS level input pin with internal pull up resistor
IN_{cd}	CMOS level input pin with internal pull down resistor
IN_{cs}	CMOS level Schmitt-trigger input pin
IN_{csu}	CMOS level Schmitt-trigger input pin with internal pull up resistor

5.1 LPC Interface

SYMBOL	PIN	I/O	FUNCTION
CLKIN	17	IN_{tp3}	System clock input. According to the input frequency 24MHz or 48MHz, it is selectable through register. Default is 24MHz input.
PME#	98	OD_{12p3}	Generated PME event.
PCICLK	19	IN_{tsp3}	PCI clock input.
LDRQ#	20	O_{12p3}	Encoded DMA Request signal.
SERIRQ	21	I/O_{12tp3}	Serial IRQ input/Output.
LAD[3:0]	23-26	I/O_{12tp3}	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
LFRAME#	27	IN_{tsp3}	Indicates start of a new cycle or termination of a broken cycle.
LRESET#	28	IN_{tsp3}	Reset signal. It can connect to PCIRST# signal on the host.

5.2 FDC Interface

SYMBOL	PIN	I/O	FUNCTION
DRVDEN0	1	OD_{24}	Drive Density Select bit 0.
INDEX#	2	IN_{csu}	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
MOA#	3	OD_{24}	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
DSB#	4	OD_{24}	Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output.
DSA#	6	OD_{24}	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
MOB#	7	OD_{24}	Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output.
DIR#	8	OD_{24}	Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
STEP#	9	OD_{24}	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
WD#	10	OD_{24}	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
WE#	11	OD_{24}	Write enable. An open drain output.
TRAK0#	12	INcsu	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
WP#	13	INcsu	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
RDATA#	14	INcsu	The read data input signal from the FDD. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
HEAD#	15	OD24	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
DSKCHG#	16	INcsu	Diskette change. This signal is active low at power on and whenever the diskette is removed. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).

5.3 Multi-Mode Parallel Port

The following pins have alternate functions, which are controlled by CR28 and L3-CRF0.

SYMBOL	PIN	I/O	FUNCTION
SLCT	29	IN_{ts}	PRINTER MODE: An active high input on this pin indicates that the printer is selected. This pin is pulled high internally. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
WE2#		OD_{12}	EXTENSION FDD MODE: WE2# This pin is for Extension FDD B; its function is the same as the WE# pin of FDC. EXTENSION 2FDD MODE: WE2# This pin is for Extension FDD A and B; its function is the same as the WE# pin of FDC.
PE	30	IN_{ts}	PRINTER MODE: An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
WD2#		OD_{12}	EXTENSION FDD MODE: WD2# This pin is for Extension FDD B; its function is the same as the WD# pin of FDC. EXTENSION 2FDD MODE: WD2# This pin is for Extension FDD A and B; its function is the same as the WD# pin of FDC.
BUSY	31	IN_{ts}	PRINTER MODE: An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
MOB2#		OD_{12}	EXTENSION FDD MODE: MOB2# This pin is for Extension FDD B; its function is the same as the MOB# pin of FDC. EXTENSION 2FDD MODE: MOB2# This pin is for Extension FDD A and B; its function is the same as the MOB# pin of FDC.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
ACK#	32	IN_{ts}	PRINTER MODE: ACK# An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DSB2#		OD_{12}	EXTENSION FDD MODE: DSB2# This pin is for the Extension FDD B; its functions is the same as the DSB# pin of FDC. EXTENSION 2FDD MODE: DSB2# This pin is for Extension FDD A and B; its function is the same as the DSB# pin of FDC.
ERR#	33	IN_{ts}	PRINTER MODE: ERR# An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
HEAD2#		OD_{12}	EXTENSION FDD MODE: HEAD2# This pin is for Extension FDD B; its function is the same as the HEAD#pin of FDC. EXTENSION 2FDD MODE: HEAD2# This pin is for Extension FDD A and B; its function is the same as the HEAD# pin of FDC.
SLIN#	34	OD_{12}	PRINTER MODE: SLIN# Output line for detection of printer selection. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
STEP2#		OD_{12}	EXTENSION FDD MODE: STEP2# This pin is for Extension FDD B; its function is the same as the STEP# pin of FDC. EXTENSION 2FDD MODE: STEP2# This pin is for Extension FDD A and B; its function is the same as the STEP# pin of FDC.

Multi-mode parallel port, continued

SYMBOL	PIN	I/O	FUNCTION
INIT#	43	OD_{12}	PRINTER MODE: INIT# Output line for the printer initialization. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DIR2#		OD_{12}	EXTENSION FDD MODE: DIR2# This pin is for Extension FDD B; its function is the same as the DIR# pin of FDC. EXTENSION 2FDD MODE: DIR2# This pin is for Extension FDD A and B; its function is the same as the DIR# pin of FDC.
AFD#	44	OD_{12}	PRINTER MODE: AFD# An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DRVDEN0		OD_{12}	EXTENSION FDD MODE: DRVDEN0 This pin is for Extension FDD B; its function is the same as the DRVDEN0 pin of FDC. EXTENSION 2FDD MODE: DRVDEN0 This pin is for Extension FDD A and B; its function is the same as the DRVDEN0 pin of FDC.
STB#	46	OD_{12}	PRINTER MODE: STB# An active low output is used to latch the parallel data into the printer. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		-	EXTENSION 2FDD MODE: This pin is a tri-state output.
PD0	42	I/O_{12ts}	PRINTER MODE: PD0 Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
INDEX2#		IN_{ts}	EXTENSION FDD MODE: INDEX2# This pin is for Extension FDD B; its function is the same as the INDEX# pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: INDEX2# This pin is for Extension FDD A and B; its function is the same as the INDEX# pin of FDC. It is pulled high internally.

Multi-mode parallel port, continued

SYMBOL	PIN	I/O	FUNCTION
PD1	41	I/O_{12ts}	PRINTER MODE: PD1 Parallel port data bus bit 1. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
TRAK02#		IN_{ts}	EXTENSION FDD MODE: TRAK02# This pin is for Extension FDD B; its function is the same as the TRAK0# pin of FDC. It is pulled high internally. EXTENSION. 2FDD MODE: TRAK02# This pin is for Extension FDD A and B; its function is the same as the TRAK0# pin of FDC. It is pulled high internally.
PD2	40	I/O_{12ts}	PRINTER MODE: PD2 Parallel port data bus bit 2. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
WP2#		IN_{ts}	EXTENSION FDD MODE: WP2# This pin is for Extension FDD B; its function is the same as the WP# pin of FDC. It is pulled high internally. EXTENSION. 2FDD MODE: WP2# This pin is for Extension FDD A and B; its function is the same as the WP# pin of FDC. It is pulled high internally.
PD3	39	I/O_{12ts}	PRINTER MODE: PD3 Parallel port data bus bit 3. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
RDATA2#		IN_{ts}	EXTENSION FDD MODE: RDATA2# This pin is for Extension FDD B; its function is the same as the RDATA# pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: RDATA2# This pin is for Extension FDD A and B; its function is the same as the RDATA# pin of FDC. It is pulled high internally.

Multi-mode parallel port, continued

SYMBOL	PIN	I/O	FUNCTION
PD4	38	I/O_{12ts}	PRINTER MODE: PD4 Parallel port data bus bit 4. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DSKCHG2#		IN_{ts}	EXTENSION FDD MODE: DSKCHG2# This pin is for Extension FDD B; the function of this pin is the same as the DSKCHG# pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: DSKCHG2# This pin is for Extension FDD A and B; this function of this pin is the same as the DSKCHG# pin of FDC. It is pulled high internally.
PD5	37	I/O_{12ts}	PRINTER MODE: PD5 Parallel port data bus bit 5. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		-	EXTENSION 2FDD MODE: This pin is a tri-state output.
PD6	36	I/O_{12ts}	PRINTER MODE: PD6 Parallel port data bus bit 6. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
MOA2#		OD_{12}	EXTENSION. 2FDD MODE: MOA2# This pin is for Extension FDD A; its function is the same as the MOA# pin of FDC.
PD7	35	I/O_{12ts}	PRINTER MODE: PD7 Parallel port data bus bit 7. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
DSA2#		OD_{12}	EXTENSION 2FDD MODE: DSA2# This pin is for Extension FDD A; its function is the same as the DSA# pin of FDC.

5.4 Serial Port Interface

SYMBOL	PIN	I/O	FUNCTION
CTSA# CTSB#	47 55	IN_t	Clear To Send. It is the modem control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
DSRA# DSRB#	48 56	IN_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
RTSA# HEFRAS	49	O_8 INcd	UART A Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. During power-on reset, this pin is pulled down internally and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). A 4.7 kΩ is recommended if intends to pull up. (select 4EH as configuration I/O port's address)
RTSB#	57	O_8	UART B Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
DTRA# PNPCSV#	50	O8 INcd	UART A Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate. During power-on reset, this pin is pulled down internally and is defined as PNPCSV#, which provides the power-on value for CR24 bit 0 (PNPCSV#). A 4.7 kΩ is recommended if intends to pull up. (clear the default value of FDC, UARTs, and PRT)
DTRB#	58	O_8	UART B Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
SINA SINB	51 59	INt	Serial Input. It is used to receive serial data through the communication link.
SOUTA PENROM#	52	O_8 INcd	UART A Serial Output. It is used to transmit serial data out to the communication link. During power on reset , this pin is pulled down internally and is defined as PENROM#, which provides the power on value for CR24 bit 1. A 4.7kΩ is recommended if intends to pull up .
SOUTB PEN48	61	O_8 INcd	UART B Serial Output. During power-on reset, this pin is pulled down internally and is defined as PEN48, which provides the power-on value for CR24 bit 6 (EN48). A 4.7 kΩ resistor is recommended if intends to pull up.
DCDA# DCDB#	53 62	IN_t	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
RIA# RIB#	54 63	IN_t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.

Serial Port Interface, continued

SYMBOL	PIN	I/O	FUNCTION
CTSC# GP67	99	IN_t I/OD_{12t}	Clear To Send. It is the modem control input. General purpose I/O port 6 bit7.
DSRC# GP66	100	IN_t I/OD_{12t}	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART. General purpose I/O port 6 bit6.
RTSC# GP65	101	O_{12} I/OD_{12t}	UART C Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. General purpose I/O port 6 bit5.
DTRC# GP64	102	O_{12} I/OD_{12t}	UART C Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate. General purpose I/O port 6 bit4.
SINC GP63	103	IN_t I/OD_{12t}	Serial Input. It is used to receive serial data through the communication link. General purpose I/O port 6 bit3.
SOUTC GP62	104	O_{12} I/OD_{12t}	UART B Serial Output. It is used to transmit serial data out to the communication link. General purpose I/O port 6 bit2.
DCDC# GP61	105	IN_t I/OD_{12t}	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier. General purpose I/O port 6 bit1.
RIC# GP60	106	IN_t I/OD_{12t}	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set. General purpose I/O port 6 bit0.

5.5 Infrared Port

SYMBOL	PIN	I/O	FUNCTION
IRRX	64	IN_{ts}	Alternate Function Input: Infrared Receiver input. General purpose I/O port 3 bit 6.
IRTX	65	O_{12}	Alternate Function Output: Infrared Transmitter Output. General purpose I/O port 3 bit 7.

5.6 Flash ROM Interface

SYMBOL	PIN	I/O	FUNCTION
XA18-XA16 GP57-GP55	66-68	O_{12} I/OD_{12t}	Flash ROM interface Address[18:16] General purpose I/O port 5 bit7-5
XA15-XA10 GP47-GP42	69-74	O_{12} I/OD_{12t}	Flash ROM interface Address[15:10] General purpose I/O port 4 bit7-2
XA9-XA8 GP41-GP40	76-77	O_{12} I/OD_{12t}	Flash ROM interface Address[9:8] General purpose I/O port 4 bit1-0
XA7-XA0 GP37-GP30	78-85	O_{12} I/OD_{12t}	Flash ROM interface Address[7:0] General purpose I/O port 3 bit7-0
XD7-XD4 GP27-GP24	86-89	I/O_{12t} I/OD_{12t}	Flash ROM interface Data Bus[7:4] General purpose I/O port 2 bit7-4
XD3-XD0 GP23-GP20	91-94	I/O_{12t} I/OD_{12t}	Flash ROM interface Data Bus [3:0] General purpose I/O port 2 bit3-0
ROMCS# GP54	95	O_{12} I/OD_{12t}	Flash ROM interface Chip Select General purpose I/O port 5 bit4
MEMR# GP53	96	O_{12} I/OD_{12t}	Flash ROM interface Memory Read Enable General purpose I/O port 5 bit3
MEMW# GP52	97	O_{12} I/OD_{12t}	Flash ROM interface Memory Write Enable General purpose I/O port 5 bit2

5.7 General Purpose I/O Port

SYMBOL	PIN	I/O	FUNCTION
GP73 SIND	111	I/OD_{12t} IN_t	General purpose I/O port 7 bit3 Serial Input. It is used to receive serial data through the communication link.
GP80 WDTO	118	I/OD_{12t} OD_{12}	General purpose I/O port 8 bit0 Watch dog timer output.

5.8 Smart Card Interface

SYMBOL	PIN	I/O	FUNCTION
SCPSNT	107	IN_{ts}	Smart card present detection Schmitt-trigger input.
CTSD#		IN_t	Clear To Send. It is the modem control.
GP77		I/OD_{24t}	General purpose I/O port 7 bit7.
SCIO	108	I/O_{24t}	Smart card data I/O channel.
DSRD#		IN_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
GP76		I/OD_{24t}	General purpose I/O port 7 bit6.
SCCLK	109	O_4	Smart card clock output.
RTSD#		O_4	UART C Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
GP75		I/OD_{4t}	General purpose I/O port 7 bit5.
SCRST	110	O_{24}	Smart card reset output.
DTRD#		O_{24}	UART C Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate.
GP74		I/OD_{24t}	General purpose I/O port 7 bit4.
SCC8	112	I/O_{24t}	Smart card General Purpose I/O channel.
SOUTC		O_{24t}	UART B Serial Output. It is used to transmit serial data out to the communication link.
GP72		I/OD_{24t}	General purpose I/O port 7 bit2.
SCPWR	113	O_{12}	Smart card power control.
DCDD#		IN_t	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
GP71		I/OD_{12t}	General purpose I/O port 7 bit1.
SCC4	114	I/O_{24t}	Smart card General Purpose I/O channel.
RID#		IN_t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
GP70		I/OD_{24t}	General purpose I/O port 7 bit0.

5.9 PWM & General Purpose I/O Port 8

SYMBOL	PIN	I/O	FUNCTION
PWM2 PLED GP83	115	O_{12} O_{12} I/OD_{12t}	Fan speed control . Use the Pulse Width Modulation (**PWM**) Power LED output, this signal is low after system reset. General purpose I/O port 8 bit2-1
PWM1-0 GP82-81	116-117	O_{12} I/OD_{12t}	Fan speed control . Use the Pulse Width Modulation (**PWM**) Technic knowledge to control the Fan's RPM. General purpose I/O port 8 bit2-1

5.10 Game Port & MIDI Port

SYMBOL	PIN	I/O	FUNCTION
MSI GP51	119	INcu I/OD_{24c}	MIDI serial data input . General purpose I/O port 5 bit 1.
MSO GP50	120	O_{12} I/OD_{12t}	MIDI serial data output. General purpose I/O port 5 bit 0.
GPAS2 GP17	121	INcs I/OD_{24cs}	Active-low, Joystick I switch input 2. This pin has an internal pull-up resistor. (Default) General purpose I/O port 1 bit 7.
GPBS2 GP16	122	INcs I/OD_{24cs}	Active-low, Joystick II switch input 2. This pin has an internal pull-up resistor. (Default) General purpose I/O port 1 bit 6.
GPAY GP15	123	I/OD_{24a} I/OD24cs	Joystick I timer pin. this pin connect to Y positioning variable resistors for the Josystick. (Default) General purpose I/O port 1 bit 5.
GPBY GP14	124	I/OD_{24a} I/OD_{24cs}	Joystick II timer pin. this pin connect to Y positioning variable resistors for the Josystick. (Default) General purpose I/O port 1 bit 4.
GPBX GP13	125	I/OD_{24a} I/OD_{24cs}	Joystick II timer pin. this pin connect to X positioning variable resistors for the Josystick. (Default) General purpose I/O port 1 bit 3.
GPAX GP12	126	I/OD24a I/OD_{24cs}	Joystick I timer pin. this pin connect to X positioning variable resistors for the Josystick. (Default) General purpose I/O port 1 bit 2.

Game Port & MIDI Port, continued

SYMBOL	PIN	I/O	FUNCTION
GPBS1	127	Incs	Active-low, Joystick II switch input 1. This pin has an internal pull-up resistor. (Default)
GP11		I/OD_{24csu}	General purpose I/O port 1 bit 1.
GPAS1	128	Incs	Active-low, Joystick I switch input 1. This pin has an internal pull-up resistor. (Default)
GP10		I/OD_{24cs}	General purpose I/O port 1 bit 0.

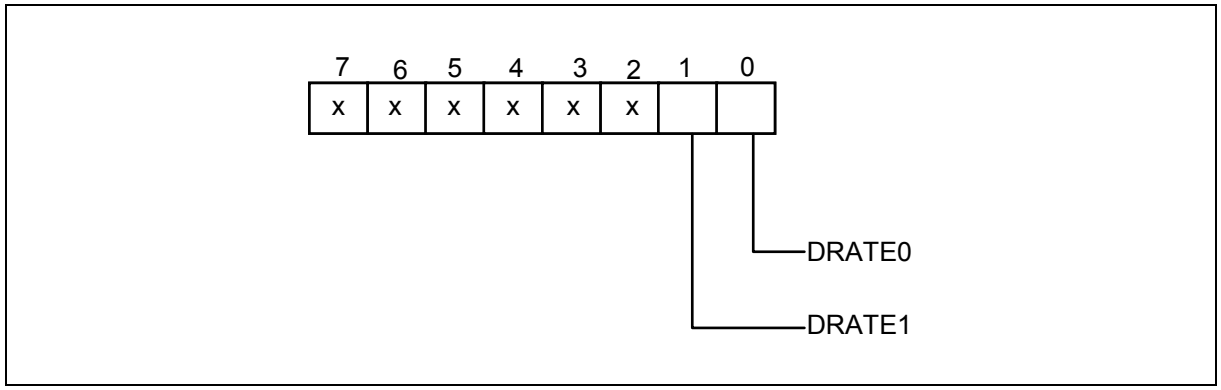
5.11 POWER PINS

SYMBOL	PIN	FUNCTION
VCC	5, 45, 75,	+5V power supply for the digital circuitry.
VCC3V	22	+3.3V power supply for driving 3V on host interface.
GND	18, 60, 90,	Ground.

6. CONFIGURATION REGISTER

6.1 Plug and Play Configuration

The W83697UF uses Compatible PNP protocol to access configuration registers for setting up different types of configurations. In W83697UF, there are eleven Logical Devices (from Logical Device 0 to Logical Device B with the exception of logical device 4 for backward compatibility) which correspond to eleven individual functions: FDC (logical device 0), PRT (logical device 1), UART1 (logical device 2), UART2 (logical device 3), CIR (Consumer IR, logical device 6), GPIO1 (logical device 7), GPIO5(logical device 8),GPIO2 ~GPIO4(logical device 9), ACPI ((logical device A), and Hardware monitor (logical device B). Each Logical Device has its own configuration registers (above CR30). Host can access those registers by writing an appropriate logical device number into logical device select register at CR7.



6.2 Compatible PnP

6.2.1 Extended Function Registers

In Compatible PnP, there are two ways to enter Extended Function and read or write the configuration registers. HEFRAS (CR26 bit 6) can be used to select one out of these two methods of entering the Extended Function mode as follows:

HEFRAS	ADDRESS AND VALUE
0	write 87h to the location 2Eh twice
1	write 87h to the location 4Eh twice

After Power-on reset, the value on RTSA# (pin 49) is latched by HEFRAS of CR26. In Compatible PnP, a specific value (87h) must be written twice to the Extended Functions Enable Register (I/O port address 2Eh or 4Eh). Secondly, an index value (02h, 07h-FFh) must be written to the Extended Functions Index Register (I/O port address 2Eh or 4Eh same as Extended Functions Enable Register) to identify which configuration register is to be accessed. The designer can then access the desired configuration register through the Extended Functions Data Register (I/O port address 2Fh or 4Fh).

After programming of the configuration register is finished, an additional value (AAh) should be written to EFERs to exit the Extended Function mode to prevent unintentional access to those configuration registers. The designer can also set bit 5 of CR26 (LOCKREG) to high to protect the configuration registers against accidental accesses.

The configuration registers can be reset to their default or hardware settings only by a cold reset (pin MR = 1). A warm reset will not affect the configuration registers.

6.2.2 Extended Functions Enable Registers (EFERs)

After a power-on reset, the W83697UF enters the default operating mode. Before the W83697UF enters the extended function mode, a specific value must be programmed into the Extended Function Enable Register (EFER) so that the extended function register can be accessed. The Extended Function Enable Registers are write-only registers. On a PC/AT system, their port addresses are 2Eh or 4Eh (as described in previous section).

6.2.3 Extended Function Index Registers (EFIRs), Extended Function Data Registers (EFDRs)

After the extended function mode is entered, the Extended Function Index Register (EFIR) must be loaded with an index value (02h, 07h-FEh) to access Configuration Register 0 (CR0), Configuration Register 7 (CR07) to Configuration Register FE (CRFE), and so forth through the Extended Function Data Register (EFDR). The EFIRs are write-only registers with port address 2Eh or 4Eh on PC/AT systems; the EFDRs are read/write registers with port address 2Fh or 4Fh on PC/AT systems.

6.3 Configuration Sequence

To program W83697UF configuration registers, the following configuration sequence must be followed:

(1). Enter the extended function mode

(2). Configure the configuration registers

(3). Exit the extended function mode

6.3.1 Enter the extended function mode

To place the chip into the extended function mode, two successive wrtites of 0x87 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

6.3.2 Configurate the configuration registers

The chip selects the logical device and activates the desired logical devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). EFIR is located at the same address as EFER, and EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e.,0x07) to the EFIR and then write the number of the desired logical device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required. Secondly, write the address of the desired configuration register within the logical device to the EFIR and then write (or read) the desired configuration register through EFDR.

6.3.3 Exit the extended function mode

To exit the extended function mode, one write of 0xAA to EFER is required. Once the chip exits the extended function mode, it is in the normal running mode and is ready to enter the configuration mode.

6.3.4 Software programming example

The following example is written in Intel 8086 assembly language. It assumes that the EFER is located at 2Eh, so EFIR is located at 2Eh and EFDR is located at 2Fh. If HEFRAS (CR26 bit 6) is set, 4Eh can be directly replaced by 4Eh and 2Fh replaced by 4Fh.

```
;--------------------------------------------------------------------------------
; Enter the extended function mode, interruptible double-write    |
;--------------------------------------------------------------------------------
MOV     DX,2EH
MOV AL,87H
OUT     DX,AL
OUT     DX,AL
;--------------------------------------------------------------------------------
; Configurate logical device 1, configuration register CRF0   |
;--------------------------------------------------------------------------------
MOV     DX,2EH
MOV     AL,07H
OUT     DX,AL           ; point to Logical Device Number Reg.
MOV     DX,2FH
MOV     AL,01H
OUT     DX,AL           ; select logical device 1
;
MOV     DX,2EH
```

```
MOV     AL,F0H
OUT     DX,AL           ; select CRF0
MOV     DX,2FH
MOV AL,3CH
OUT     DX,AL           ; update CRF0 with value 3CH
;----------------------------------------
; Exit extended function mode     |
;----------------------------------------
MOV     DX,2EH
MOV AL,AAH
OUT     DX,AL
```

6.4 Chip (Global) Control Register

CR02 (Default 0x00) (Write only)

Bit [7:1]: Reserved.

Bit 0 = 1 SWRST --> Soft Reset.

CR07

Bit [7:0]: LDNB7 - LDNB0 --> Logical Device Number Bit 7 - 0

CR20 (read only)

Bit [7:0]: DEVIDB7 - DEBIDB0 --> Device ID Bit 7 - Bit 0
= 0x 68 (for W83697UF)

CR21 (read only)

DEVREVB7 - DEBREVB0 --> Device Rev
= 0x1X (for W83697UF)

Bit [7:0]:

X : Version change number. (Bit [3:0]) --> begin from 1

CR22 (Default 0xef)

Bit 7: SCPWD

0 Power down

1 No Power down

Bit 6: URDPWD

0 Power down

1 No Power down