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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# W83781D/W83781G

# WINBOND
# H/W MONITORING IC

*Publication Release Date: April 14, 2005*
*Revision 2.0*

## *Table Of Contents-*

# 1. GENERAL DESCRIPTION

The W83781D/G is a hardware monitoring IC for personal computers, server computers, or microprocessor based systems. W83781D/G can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system to work stablely and properly. W83781D provides both ISA and $I^2C^{TM}$ serial bus interface.

A 8-bit analog-to-digital converter (ADC) was built inside W83781D/G. The W83781D/G can monitor 3 external thermistor temperature sensors, 5 positive analog voltage inputs, two inverting inputs (for monitoring negative voltages), and also three fan tachometer outputs. There is also one input for case open detection circuits.

With the application software, the users can read all the monitored parameters of system from time to time. The application software could be the popular Intel™ LDCM (LANDesk Client Management) or Winbond application software. Also the users can set up the upper and lower limits of these monitored parameters and to activate two programmable and maskable interrupts. An optional beep tone could be used as warning signal when the monitored parameters is out of the preset range.

Additionally, 5 VID inputs are provided to read the VID of CPU (such as Pentium™ II) if applicable. This is to provide the Vcore correction automatically. Also W83781D uniquely provides an optional feature: early stage (before BIOS was load) beep warning. This is to detect if the fatal elements present --- VcoreA, +3.3V voltage fail, and the system can not be boomed up.

# 2. FEATURES

## 2.1 Monitoring Items

- 3 thermal inputs from remote thermistors
- 5 positive voltage inputs (typical for +12V, +5V, +3.3V, VcoreA, VcoreB)
- 2 op amps for negative voltage monitoring (typical for -12V, -5V)
- 3 fan speed monitoring inputs
- Case open detection input
- WATCHDOG comparison of all monitored values
- Programmable hysteresis and setting points for all monitored items

## 2.2 Actions Enabling

- Warning signal pop up in application software
- Beep tone warning
- Fan ON/OFF control
- Issue SMI#, IRQ to activate system protection

## 2.3 General

- ISA and $I^2C^{TM}$ serial bus interface
- 5 VID input pins for CPU Vcore identification
- Initial power fault beep (for +3.3V, VcoreA)
- Master reset input to W83781D/G
- Independent power plane of digital Vcc and analog Vcc (input to IC)
- Intel LDCM™ compatible
- Winbond monitoring application software support
- Input clock rate optional for 24, 48, 14.318 MHz

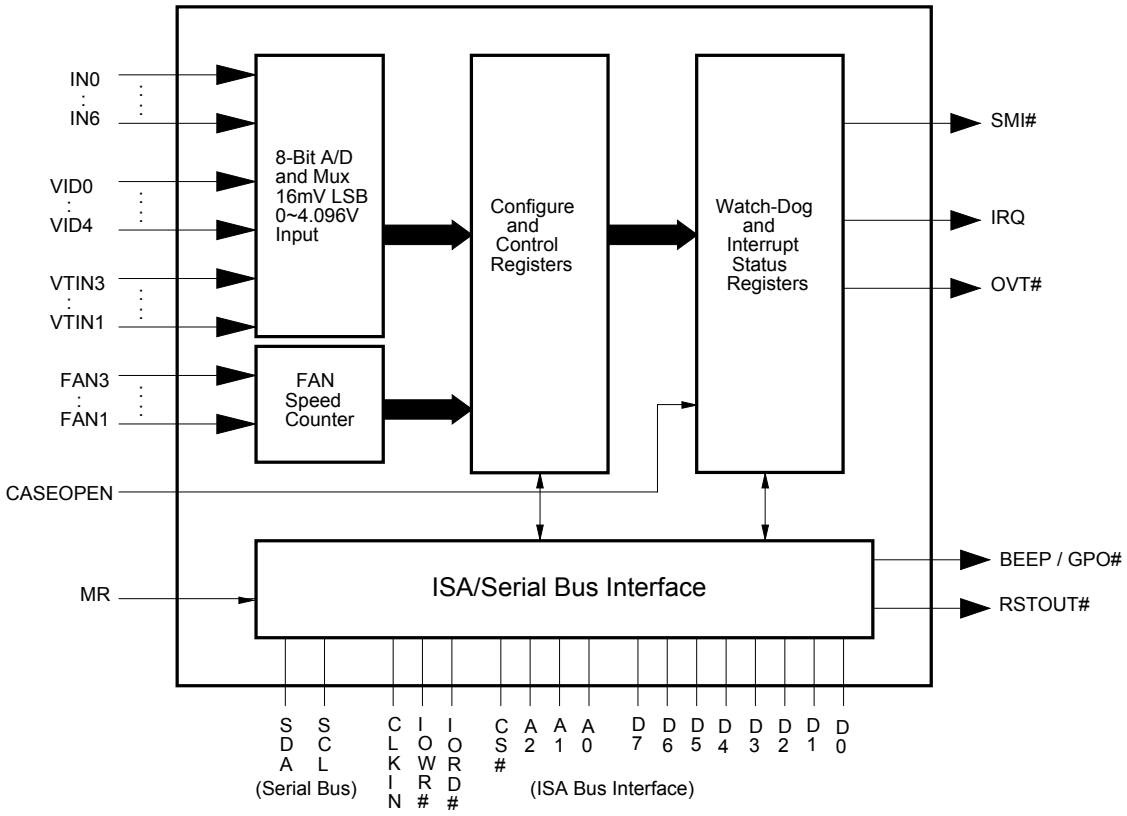
## 2.4 Package

- 48-pin LQFP

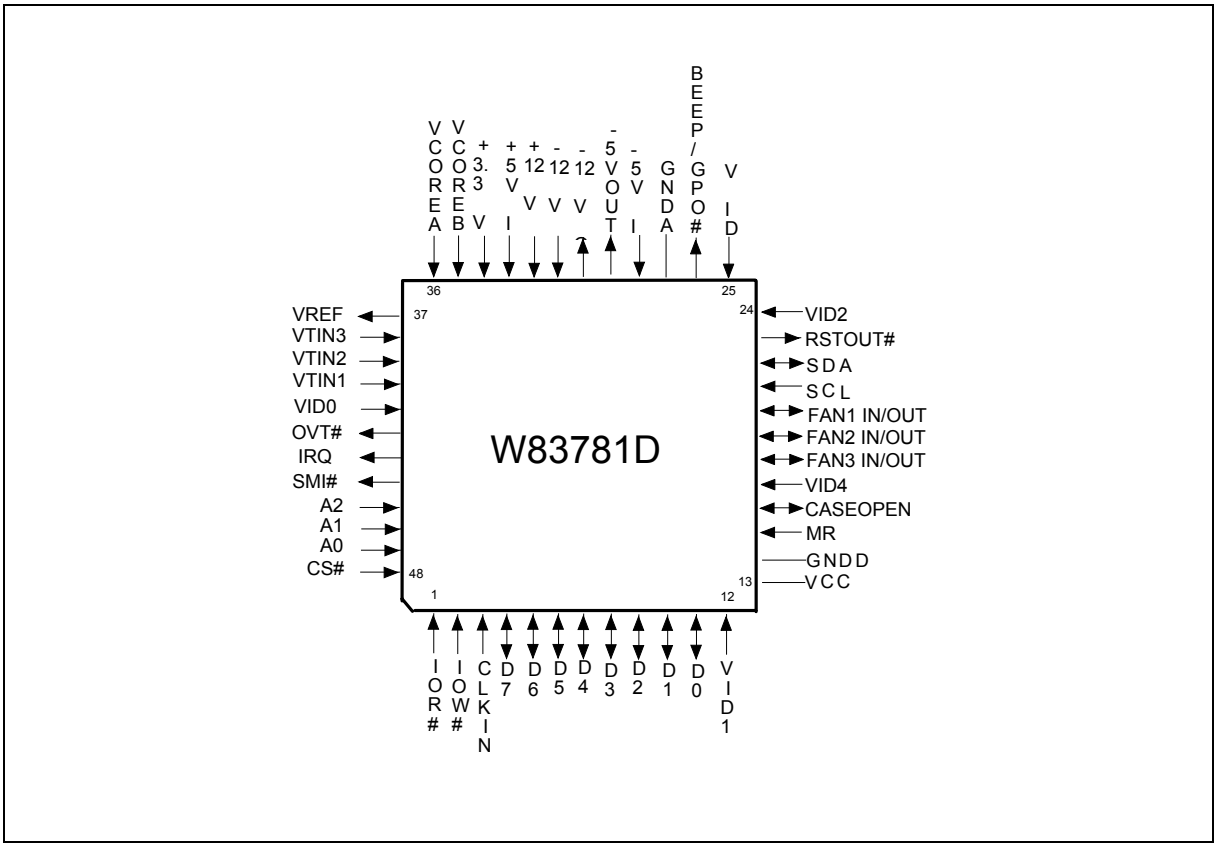
# 3. KEY SPECIFICATIONS

| | |
|---|---|
| • Voltage monitoring accuracy | ±1% (Max) |
| • Monitoring Temperature Range and Accuracy | |
| - 40°C to +120°C | ± 3°C(Max) |
| • Supply Voltage | 5V |
| • Supply Current | Operating: 1 mA typ. |
| | Shutdown: 10 μA typ. |
| • ADC Resolution | 8 Bits |

## 4. BLOCK DIAGRAM



## 5. PIN CONFIGURATION




## 6. PIN DESCRIPTION

$I/O_{12t}$ - TTL level bi-directional pin with 12 mA source-sink capability

$I/O_{12ts}$ - TTL level and schmitt trigger

$OUT_{12t}$ - TTL level output pin with 12 mA source-sink capability

$OUT_{8t}$ - TTL level output pin with 8 mA source-sink capability

AOUT - Output pin(Analog)

$OD_8$ - Open-drain output pin with 8 mA sink capability

$OD_{12}$ - Open-drain output pin with 12 mA sink capability

$OD_{48}$ - Open-drain output pin with 48 mA sink capability

$IN_t$ - TTL level input pin

$IN_{ts}$ - TTL level input pin and schmitt trigger

AIN - Input pin(Analog)

| PIN NAME | PIN NO. | TYPE | DESCRIPTION |
|---|---|---|---|
| IOR# | 1 | $IN_{ts}$ | An active low standard ISA bus I/O Read Control. |
| IOW# | 2 | $IN_{ts}$ | An active low standard ISA bus I/O Write Control. |
| CLKIN | 3 | $IN_{t}$ | System clock input. Can select 48MHz or 24MHz or 14.318MHz. The default is 24MHz. |
| D7~D0 | 4-11 | $I/O_{12t}$ | Bi-directional ISA bus Data lines. D0 corresponds to the low order bit, with D7 the high order bit. |
| VID1 | 12 | $IN_{t}$ | Voltage Supply readouts from P6.This value is read in the VID/Fan Divisor Register. |
| $V_{CC}$ (+5V) | 13 | POWER | +5V $V_{CC}$ power. Bypass with the parallel combination of 10μF (electrolytic or tantalum) and 0.1μF (ceramic) bypass capacitors. |
| GNDD | 14 | DGROUND | Internally connected to all digital circuitry. |
| MR | 15 | $IN_{ts}$ | Master reset input. |
| CASEOPEN | 16 | $I/O_{12t}$ | CASE OPEN. An active high input from an external circuit which latches a Case Open event. This line can go high without any clamping action intrusion regardless of the powered state of the W83781D/G. The W83781D/G provides an internal open drain on this line, controlled by Bit 7 of IRQ Mask Register 2, to provide a minimum 20 ms reset of this line. |
| VID4 | 17 | $IN_{t}$ | Voltage Supply readouts from P6.This value is read in the bit <0> of Device ID Register. |
| FAN3-FAN1 IN/OUT | 18-20 | $I/O_{12ts}$ | 0V to +5V amplitude fan tachometer input /<br>Fan on-off control output. These multifunctional pins can be programmable input or output. |
| SCL | 21 | $IN_{ts}$ | Serial Bus Clock. |
| SDA | 22 | $I/O_{12ts}$ | Serial Bus bi-directional Data. |
| RSTOUT# | 23 | $OUT_{8t}$ | 8 mA driver (open drain), active low output with a 20 ms minimum pulse width. Available when enabled via Bit 7 in SMI# Mask Register 2. |
| VID2 | 24 | $IN_{t}$ | Voltage Supply readouts from P6.This value is read in the VID/Fan Divisor Register. |
| VID3 | 25 | $IN_{t}$ | Voltage Supply readouts from P6.This value is read in the VID/Fan Divisor Register. |
| BEEP/GPO# | 26 | $OD_{48}$ | Beep function or General purpose output (active low). This pin is open drain driving 48 mA.<br>This multifunctional pin is programmable selected by CR4D bit 6. |
| GNDA | 27 | AGROUND | Internally connected to all analog circuitry. The ground reference for all analog inputs. |
| -5VIN | 28 | AIN | Ground-referred inverting op amp input. |
| -5VOUT | 29 | AOUT | Output of inverting op amp for Input 6. |
| -12VOUT | 30 | AOUT | Output of inverting op amp for Input 5. |

Continued

| PIN NAME | PIN NO. | TYPE | DESCRIPTION |
|---|---|---|---|
| -12VIN | 31 | AIN | Ground-referred inverting op amp input. |
| +12VIN | 32 | AIN | 0V to 4.096V FSR Analog Inputs. |
| +5VIN | 33 | AIN | This pin is Analog Vcc and connects internal monitor channel IN3 with fixed scale. |
| +3.3VIN | 34 | AIN | 0V to 4.096V FSR Analog Inputs. |
| VCOREB | 35 | AIN | 0V to 4.096V FSR Analog Inputs. |
| VCOREA | 36 | AIN | 0V to 4.096V FSR Analog Inputs. |
| VREF | 37 | AOUT | Reference Voltage. |
| VTIN3 | 38 | AIN | Thermistor 3 terminal input. |
| VTIN2 | 39 | AIN | Thermistor 2 terminal input. |
| VTIN1 | 40 | AIN | Thermistor 1 terminal input. |
| VID0 | 41 | $IN_t$ | Voltage Supply readouts from P6.This value is read in the VID/Fan Divisor Register. |
| OVT# | 42 | $OD_{12}$ | Over temperature Shutdown Output. |
| IRQ | 43 | $OUT_{12t}$ | Interrupt Request. |
| SMI# | 44 | $OD_{12}$ | System Management Interrupt (open drain). This output is enabled when Bit 1 in the Configuration Register (CR40) is set to 1. The default state is disabled. |
| A2-A0 | 45-47 | $IN_t$ | The three lowest order bits of the 16-bit ISA Address Bus. A0 corresponds to the lowest order bit. |
| CS# | 48 | $IN_t$ | Chip Select input from an external decoder which decodes high order address bits on the ISA Address Bus. This is an active low input. |

# Indicates Active Low("Not")

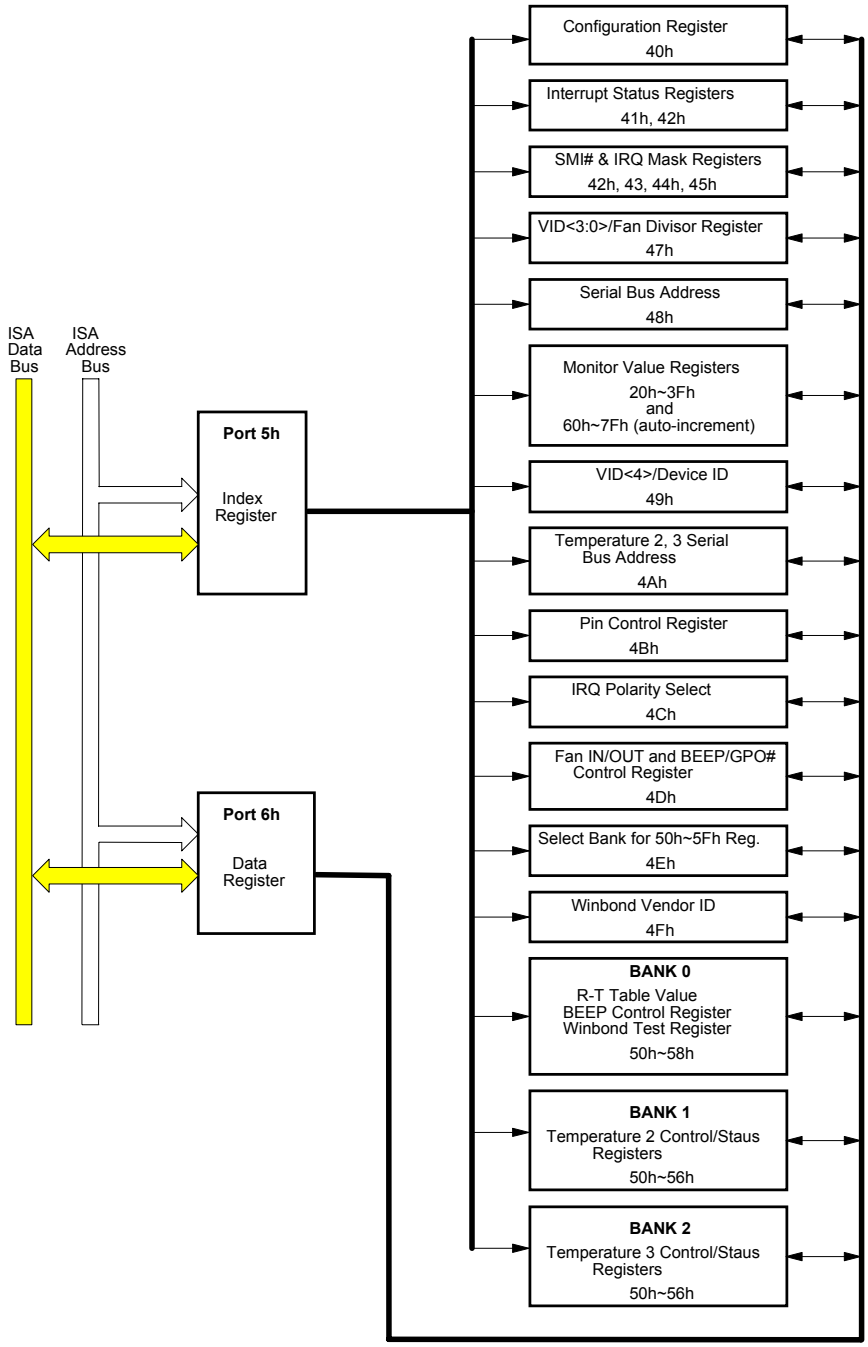
## 7. FUNCTIONAL DESCRIPTION

### 7.1 General Description

The W83781D/G provides 5 analog positive inputs, 2 analog negative input, 3 fan speed monitors or fan ON/OFF control, 3 thermistor voltage inputs, case open detection and beep function output when the monitor value exceed the set limit value. When start the monitor function on the chip, the watch dog machine monitor every function and store the value to registers. If the monitor value exceeds the limit value, the interrupt status will be set to 1.

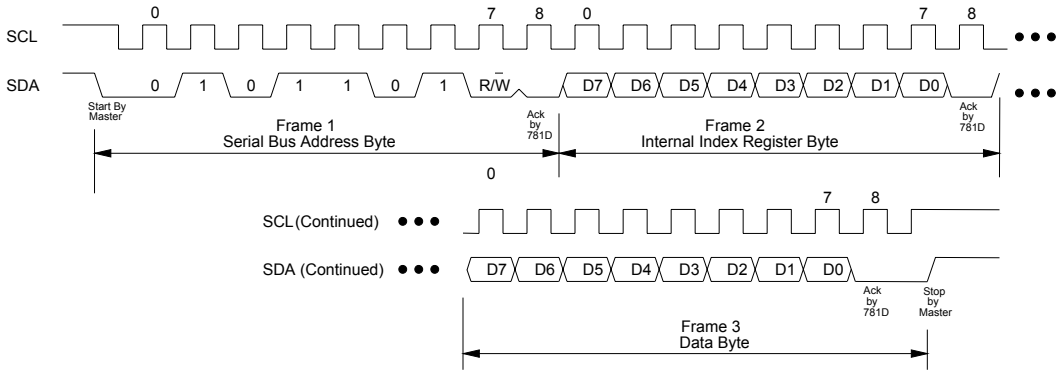
The W83781D/G provides two interface for microprocessor to read/write internal registers. The first interface use ISA Bus to access which the ports of low byte (bit2~bit0) are defined in the port 5h and 6h. The high byte of these ports is decoded by Chip Select (CS#), the general decoded address is set to port 295h and port 296h. These two ports are described as following:
Port 295h: W83781D/G Index register port.
Port 296h: Data port.

The register structure is showed as the diagram next page.
The second interface use Serial Bus. In the W83781D/G has three serial bus address. That is, the first address defined at CR48 can read/write all registers excluding Bank 1 and Bank 2 temperature 2/3 registers, the second address defined at CR4A.bit2-0 only read/write temperature sensor 2 registers, and the third address defined at CR4A.bit6-4 only can access (read/write) temperature sensor 3 registers.



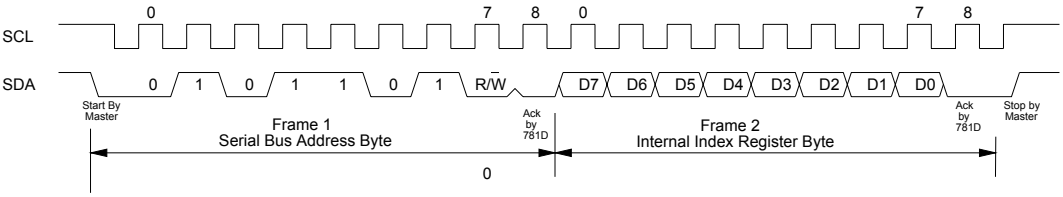
### 7.1.1 The first serial bus access timing is shown as follows:

(a) Serial bus write to internal address register followed by the data byte



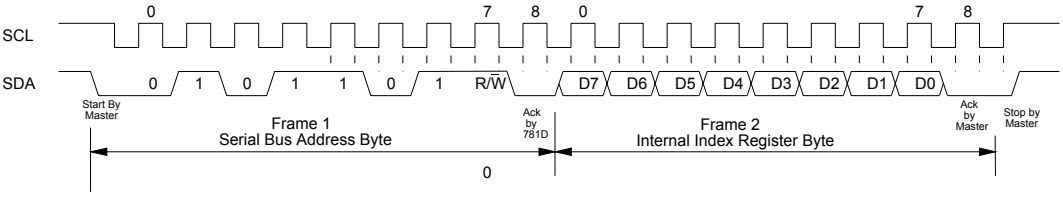

Serial Bus Write to Internal Address Register followed by the Data Byte

(b) Serial bus **write** to internal address register only




Serial Bus Write to Internal Address Register Only

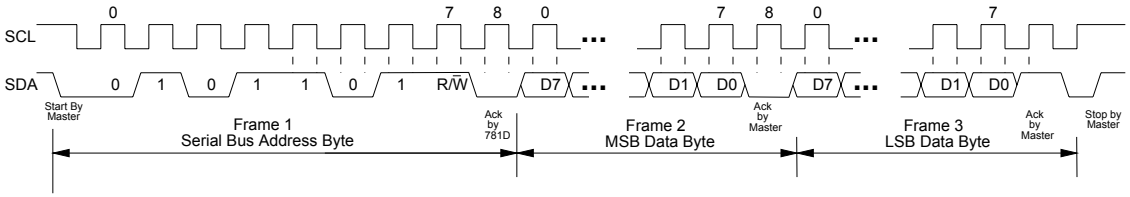
(c) Serial bus **read** from a register with the internal address register prefer to desired location




Serial Bus Write to Internal Address Register Only

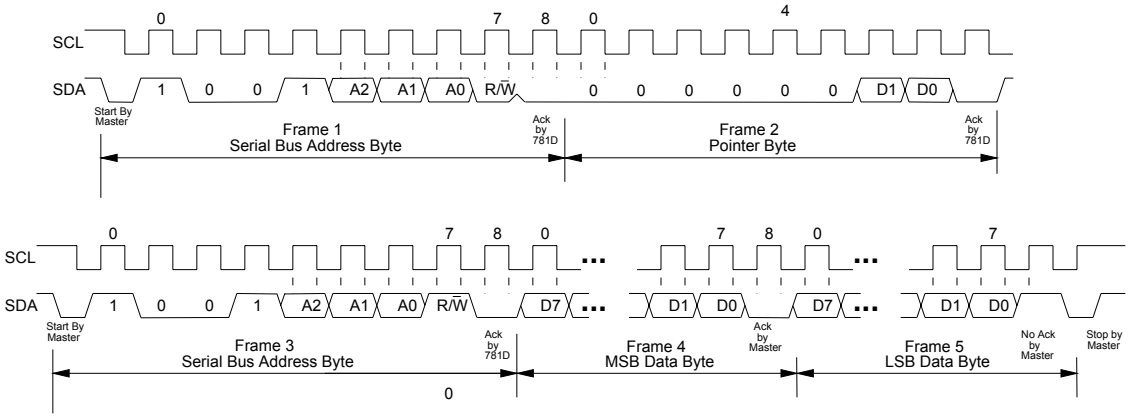
### 7.1.2 The serial bus timing of the temperature 2 and 3 is shown as follows:

(a) Typical **2-byte read** from preset pointer location (Temp, $T_{OS}$, $T_{HYST}$)



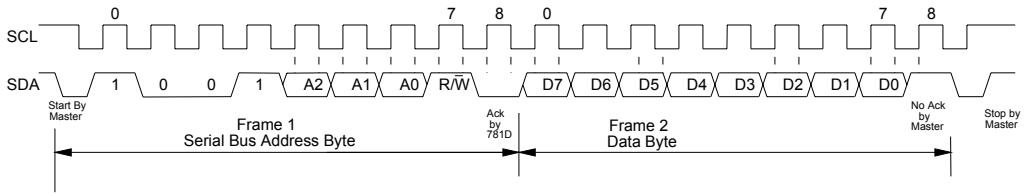

Typical 2-Byte Read From Preset Pointer Location

(b) Typical pointer set followed by immediate **read** for **2-byte register** (Temp, $T_{OS}$, $T_{HYST}$)



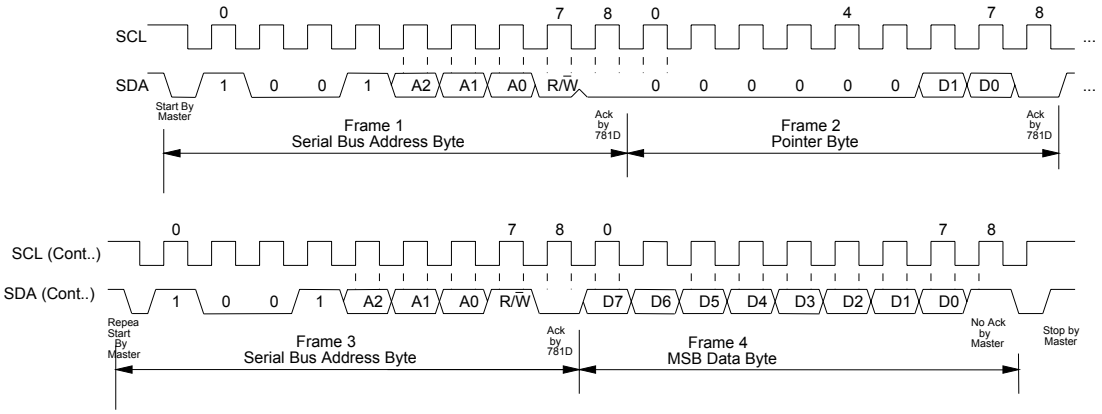

Typical Pointer Set Followed by Immediate Read for 2-Byte Register

(c) Typical **read 1-byte** from configuration register with preset pointer



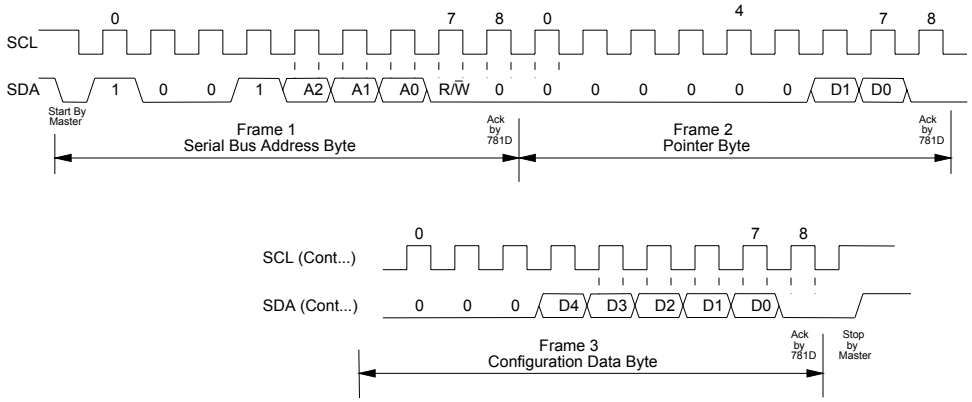

Typical 1-Byte Read From Configuration With Reset Pointer

(d) Typical pointer set followed by immediate **read** from **configuration register**



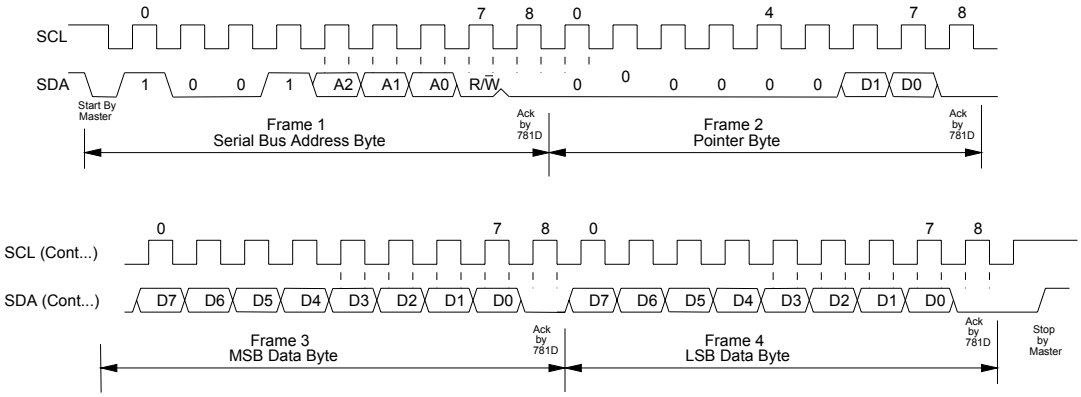

Typical Pointor Set Followed by Immediate Read from Temp 2/3 Configuration Register

(e) Temperature 2/3 configuration register **Write**




Configuration Register Write

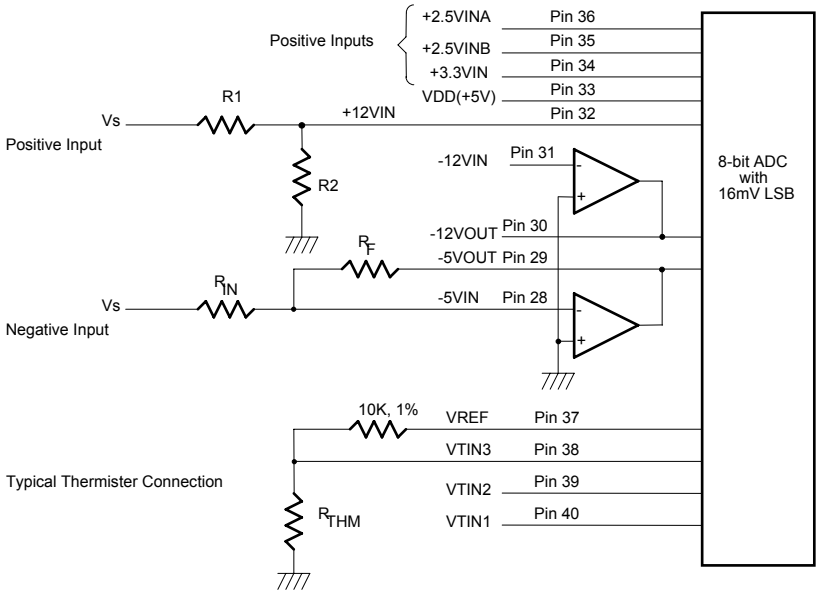
(f) Temperature 2/3 $T_{OS}$ and $T_{HYST}$ **write**




Configuration Register Write

## 7.2 Analog Inputs

The maximum input voltage of the analog pin is 4.096 because the 8-bit ADC has a 16mv LSB. Really, the application of the PC monitoring would most often be connected to power suppliers. The CPU V-core voltage and 3.3V can directly connected to these analog inputs. The +5V and +12V inputs should be reduced a factor with external resistors so as to obtain the input range. As followed figure is shown.




The input voltage can be expressed as following equation.

$$V_{IN} = V_s \times \frac{R_2}{R_1 + R_2}$$

The value of $R_1$ and $R_2$ can be selected to 28K Ohms and 10K Ohms, respectively, when the input voltage is 12V. The Pin 33 is connected to +5V power supply to provide analog power, and this voltage is connected to internal resistors to monitor the +5V voltage.
The negative voltage should be connected an op amps to invert and reduce the -5V and -12V voltage. The input voltage can be calculated by following equation.

$$V_S = -V_{IN} \times (\frac{R_F}{R_{IN}})$$

The Winbond recommended value is $R_{IN}$=90.9K Ohms and $R_F$=60.4K Ohms for -5V voltage input, $R_{IN}$=210K Ohms and $R_F$=60.4K Ohms for -12V voltage input.
The temperature sensors are connected by a 10K Ohms, then connect to VREF (Pin 37). The sensors should choose 10K Ohms at 25°C and β-value is 3435 for default R-T table. If the β-value is not 3435, the R-T table should be re-program to generate a correct temperature.

## 7.3 FAN Inputs and FAN Control

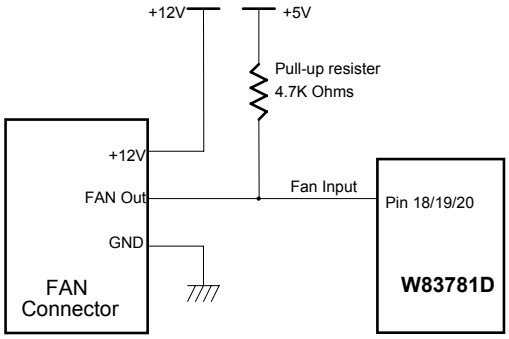
Inputs are provides for signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage can not be over +5.5V. If the input signals from the tachometer outputs are over the VCC, the external trimming circuit should be added to reduce the voltage to obtain the input specification. The normal circuit and trimming circuits are shown as following.

Determine the fan counter according to:

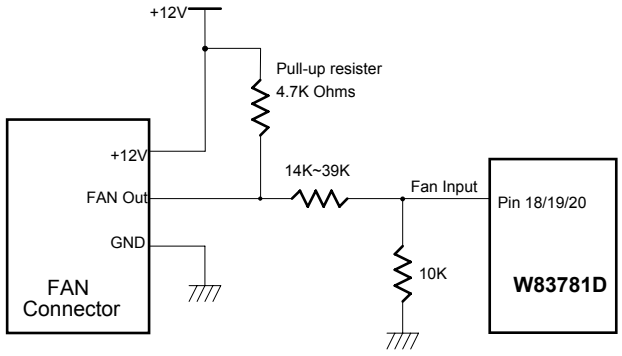
$$\text{Count} = \frac{1.35 \times 10^6}{\text{RPM} \times \text{Divisor}}$$

The default divisor is 2 and defined at CR47.bit7~4 and CR4B.bit7~6. The followed table is an example for the relation of divisor, PRM, and count.

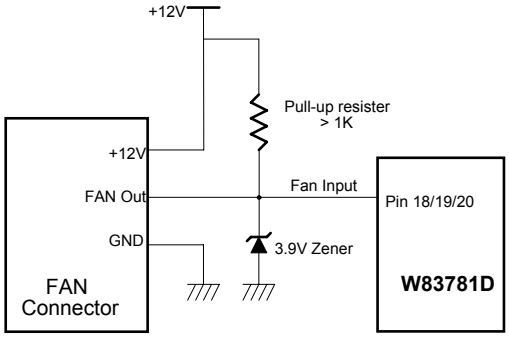
| DIVISOR | NOMINAL PRM | TIME PER REVOLUTION | COUNTS | 70% RPM | TIME FOR 70% |
|---|---|---|---|---|---|
| 1 | 8800 | 6.82 ms | *153* | 6160 | 9.74 ms |
| **2** | 4400 | 13.64 ms | *153* | 3080 | 19.48 ms |
| 4 | 2200 | 27.27 ms | *153* | 1540 | 38.96 ms |
| 8 | 1100 | 54.54 ms | *153* | 770 | 77.92 ms |



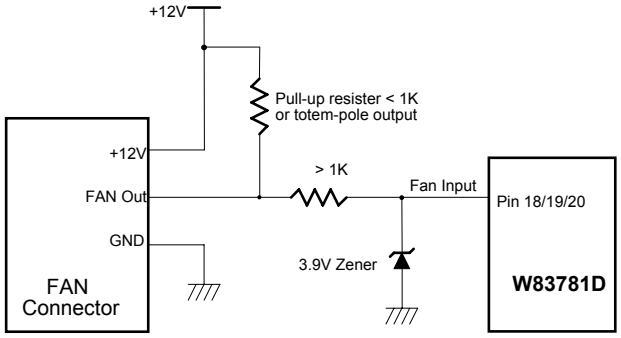

Fan with Tach Pull-Up to +5V




Fan with Tach Pull-Up to +12V, or Totem-Pole Output and Register Attenuator




Fan with Tach Pull-Up to +12V and Zener Clamp



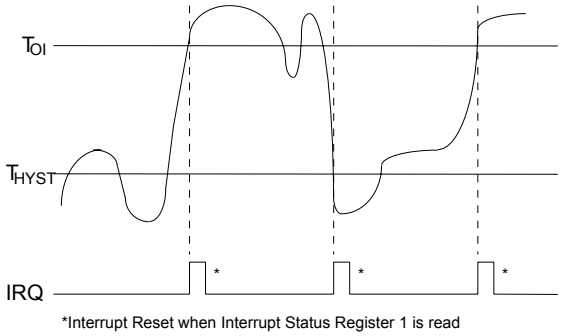

Fan with Tach Pull-Up to +12V, or Totem-Pole Putput and Zener Clamp

## 7.4 Temperature Measurement Machine

The temperature data format is 8-bit two -complement for sensor 1 and 9-bit two -complement for sensor 2/3. The table are expressed the temperature data as following.

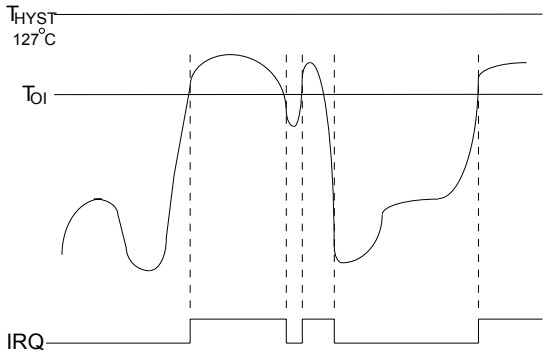
| Temperature | 8-Bit Digital Output | | 9-Bit Digital Output | |
|---|---|---|---|---|
| | 8-Bit Binary | 8-Bit Hex | 9-Bit Binary | 9-Bit Hex |
| +125°C | 0111,1101 | 7Dh | 0,1111,1010 | 0FAh |
| +25°C | 0001,1001 | 19h | 0,0011,0010 | 032h |
| +1°C | 0000,0001 | 01h | 0,0000,0010 | 002h |
| +0.5°C | - | - | 0,0000,0001 | 001h |
| +0°C | 0000,0000 | 00h | 0,0000,0000 | 000h |
| -0.5°C | - | - | 1,1111,1111 | 1FFh |
| -1°C | 1111,1111 | FFh | 1,1111,1110 | 1FFh |
| -25°C | 1110,0111 | E7h | 1,1100,1110 | 1CEh |
| -55°C | 1100,1001 | C9h | 1,1001,0010 | 192h |

The W83781D/G temperature interrupt has two mode: (1) The first is Interrupt Mode--exceeding $T_{OI}$ causes an interrupt until reset by reading Interrupt Status Register 1 (CR41). Once an interrupt event has occurred over $T_{OI}$, the interrupt will occur again by the temperature going below $T_{HYST}$. (2) Comparator Mode--setting the $T_{HYST}$ limit to 127°C will cause the comparator mode. When temperature exceeds $T_{OI}$, the interrupt will be generate Interrupt. If the temperature goes below the $T_{OI}$, the interrupt will be reset. Two interrupt modes are shown as below.



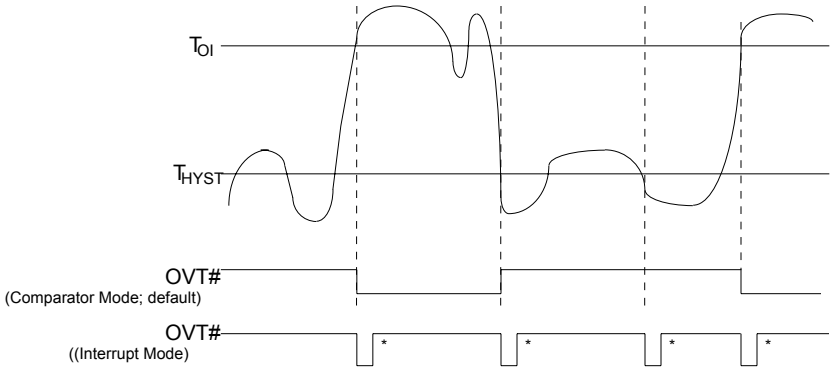

*Interrupt Reset when Interrupt Status Register 1 is read

(1) Interrupt Mode




(2) Comparator Mode

The temperature sensor 2 or 3 Over-Temperature (OVT) response is same as temperature sensor 1 IRQ signal.



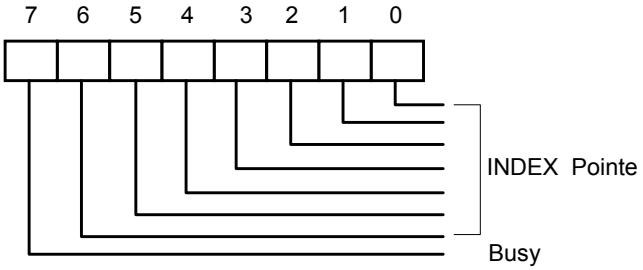

*Interrupt Reset when Temperature 2/3 is read

Over-Temperature Response Diagram

# 8. CONTROL AND STATUS REGISTERS

## 8.1 Address Register (Port x5h)

The main register is the INDEX Register located at Port x5h. The bit designations are as follows:




Bit7: Read Only

The logical 1 indicates the device is busy because of a Serial Bus transaction or another ISA bus transaction. With checking this bit, multiple ISA drivers can use W83781D/G without interfering with each other or a Serial Bus driver.

It is the user's responsibility not to have a Serial Bus and ISA bus operations at the same time.

This bit is:

**Set:** with a write to Port x5h or when a Serial Bus transaction is in progress.

**Reset:** with a write or read from Port x6h if it is set by a write to Port x5h, or when the Serial Bus transaction is finished.

Bit 6-0: Read/Write

**INDEX of Control and Status Registers. See the tables below for detail.**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Busy | Index Pointer (Power On default 00h) | | | | | | |
| (Power On default 0) | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

**Index Pointer (A6-A0)**

| Registers | Bank | A6-A0 in Hex | Power On Value of Registers: <7:0>in Binary | Notes |
|---|---|---|---|---|
| Configuration Register | 0 | 40h | 00001000 | |
| Interrupt Status Register 1 | 0 | 41h | 00000000 | Auto-increment to the address of Interrupt Status Register 2 after a read or write to Port x6h. |
| Interrupt Status Register 2 | 0 | 42h | 00000000 | |

Index Pointer (A6-A0), continued

| Registers | Bank | A6-A0 in Hex | Power On Value of Registers: <7:0>in Binary | Notes |
|---|---|---|---|---|
| SMI# Mask Register 1 | 0 | 43h | 00000000 | Auto-increment to the address of SMI# Mask Register 2 after a read or write to Port x6h. |
| SMI# Mask Register 2 | 0 | 44h | 00000000 | |
| IRQ Mask Register 1 | 0 | 45h | 00000000 | Auto-increment to the address of IRQ Mask Register 2 after a read or write to Port x6h |
| IRQ Mask Register 2 | 0 | 46h | 00000000 | |
| VID/Fan Divisor Register | 0 | 47h | <7:4> = 0101;<br><3:0> = VID3-VID0 | |
| Serial Bus Address Register | 0 | 48h | <6:0> = 0101101;<br><7> = 0 | |
| Voltage ID | 0 | 49h | <7:6> is Reserved<br><5:4> is 01 binary<br><0> is mapped to VID <4> | |
| Temperature 2 and Temperature 3 Serial Bus Address Register | 0 | 4Ah | <7:0> = 0000,0001 binary | |
| Pin Control Register | 0 | 4Bh | <7:0> 44h | |
| RQ/OVT# Property Select | 0 | 4Ch | <7:0> ---0,0001 | |
| FAN IN/OUT and BEEP/GPO# Control Register | 0 | 4Dh | <7:0> 0001,0101 | |
| Register 50h ~ 5Fh Bank Select | 0 | 4Eh | <6:3> = Reserved, <7> = 1, <2:0> = 0 | |
| Winbond Vendor ID | 0 | 4Fh | <15:0> = 5CA3h | |
| Resistor-Temperature Table Register | 0 | 50-51h | | |
| FAN Input Clock Pre-Divisor Register 2 | 0 | 55h | <7:0> -000,0001 | |
| BEEP Control Register 1 | 0 | 56h | <7:0> 0000,0000 | |
| BEEP Control Register 2 | 0 | 57h | <7:0> 1000-0000 | |

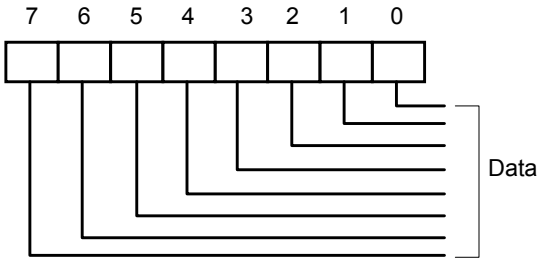
Index Pointer (A6-A0), continued

| Registers | Bank | A6-A0 in Hex | Power On Value of Registers: <7:0>in Binary | Notes |
|---|---|---|---|---|
| Chip ID | 0 | 58h | <7:0> 0001-0000 | |
| Temperature Sensor 2 Temperature Register | 1 | 50-51h | | |
| Temperature Sensor 2 Configuration Register | 1 | 52h | <7:0> = 0x00 | |
| Temperature Sensor 2 Hysteresis (High Byte) Register | 1 | 53h | <7:0> = 0x4B | |
| Temperature Sensor 2 Hysteresis (Low Byte) Register | 1 | 54h | <7:0> = 0x0 | |
| Temperature Sensor 2 Over-temperature(High Byte) Register | 1 | 55h | <7:0> = 0x50 | |
| Temperature Sensor 2 Over-temperature (Low Byte) Register | 1 | 56h | <7:0> = 0x0 | |
| Temperature Sensor 3 Temperature Register | 2 | 50-51h | | |
| Temperature Sensor 3 Configuration Register | 2 | 52h | <7:0> = 0x00 | |
| Temperature Sensor 3 Hysteresis (High Byte) Register | 2 | 53h | <7:0> = 0x4B | |
| Temperature Sensor 3 Hysteresis (Low Byte) Register | 2 | 54h | <7:0> = 0x0 | |
| Temperature Sensor 3 Over-temperature (High Byte)Register | 2 | 55h | <7:0> = 0x50 | |
| Temperature Sensor 2 Over-temperature (Low Byte) Register | 2 | 56h | <7:0> = 0x0 | |
| Value RAM | 0 | 20-3Fh | | |
| Value RAM | 0 | 60-7Fh | | Auto-increment to the next location after a read or write to Port x6h and stop at 7Fh. |

**Note:** Index Pointer (A6-A0) and Value RAM only can be read at the accurate bank.

## 8.2 Data Register (Port x6h)

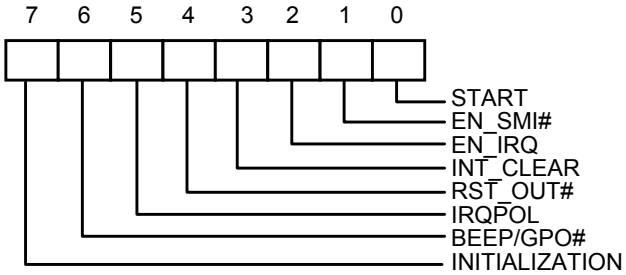
Data Port: Port x6h
Power on Default Value 00h
Attribute: Read/write
Size: 8 bits




Bit 7-0: Data to be read from or to be written to RAM and Register.

## 8.3 Configuration Register – Index 40h (*Bank 0*)

Register Location: 40h
Power on Default Value 00000001 binary
Attribute: Read/write
Size: 8 bits




Bit 7: The logical 1 restores power on default value to all registers except the Serial Bus Address register. This bit clears itself since the power on default is zero.

Bit 6: The logical 1 in this bit drives a zero on GPO# pin.

Bit 5: IRQ polarity select. When set to 0, IRQ active high. Set to 1, IRQ active low. Default 0.

Bit 4: The logical 1 outputs at least a 20 ms active low reset signal at RST_OUT# if <7> = 1 in SMI# Mask Register 2. This bit is cleared once the pulse has gone inactive.

Bit 3: The logical 1 disables the SMI# and IRQ outputs without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.

Bit 2: The logical 1 enables the IRQ Interrupt output.

Bit 1: The logical 1 enables the SMI# Interrupt output.

Bit 0: **1** enables startup of monitoring operations

**0** puts the part in standby mode.

**Note:** The outputs of Interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred unlike "INT_CLEAR" bit.

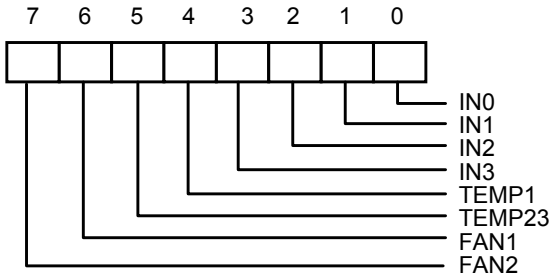
## 8.4 Interrupt Status Register 1 – Index 41h (*Bank 0*)

Register Location: 41h

Power on Default Value 00h

Attribute: Read Only

Size: 8 bits




Bit 7: The logical 1 indicates the fan count limit has been exceeded.

Bit 6: The logical 1 indicates the fan count limit has been exceeded.

Bit 5: The logical 1 indicates a High or Low limit has been exceeded from temperature sensor 2 or sensor 3. The high and low limits value are defined in index registers: 53h-56h of the Bank 1.

Bit 4: The logical 1 indicates a High or Low limit has been exceeded from temperature sensor 1.

Bit 3-0: The logical 1 indicates a High or Low limit has been exceeded.

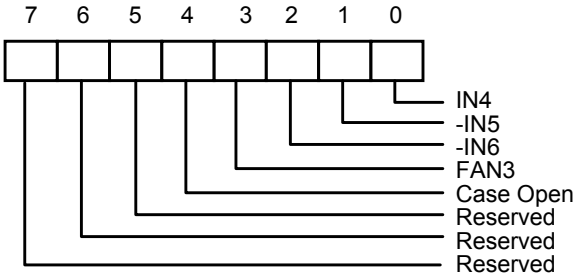
## 8.5 Interrupt Status Register 2 – Index 42h (*Bank 0*)

Register Location: 42h

Power on Default Value 00h

Attribute: Read Only

Size: 8 bits




Bit 7-5: Reserved.This bit should be set to 0.

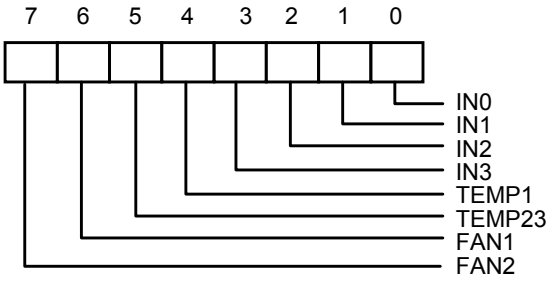
Bit 4: The logical 1 indicates Case Open has gone high.

Bit 3: The logical 1 indicates the fan count limit has been exceeded.

Bit 2-0: The logical 1 indicates a High or Low limit has been exceeded.

## 8.6 SMI# Mask Register 1 – Index 43h (*Bank 0*)

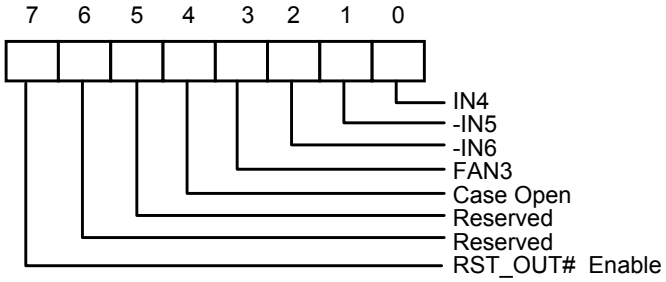
Register Location: 43h
Power on Default Value 00h
Attribute: Read/Write
Size: 8 bits




Bit 7-0: The logical 1 disables the corresponding interrupt status bit for SMI# interrupt.

## 8.7 SMI# Mask Register 2 – Index 44h (*Bank 0*)

Register Location: 44h
Power on Default Value 00h
Attribute: Read/Write
Size: 8 bits



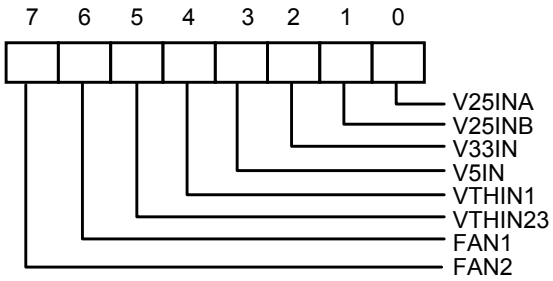

Bit 7: <7> = 1 in SMI# ask Register 2 enables the RST_OUT# in the Configuration Register. 13.8 IRQ Mask Register 1—Index 45h

Bit 6-5: Reserved. This bit should be set to 0.

Bit 4-0: The logical 1 disables the corresponding interrupt status bit for SMI# interrupt.

## 8.8 IRQ Mask Register 2 – Index 45h (*Bank 0*)

Register Location: 45h
Power on Default Value 00h
Attribute: Read/Write
Size: 8 bits




Bit 7-0: The logical 1 disables the corresponding interrupt status bit for IRQ interrupt.

## 8.9 IRQ Mask Register 2 – Index 46h (*Bank 0*)

Register Location: 46h
Power on Default Value <7:0> = 01000000 binary
Attribute: Read/Write
Size: 8 bits