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W83782D/W83782G

WINBOND
H/W MONITORING IC

winbond

Table of Contents-

1. GENERAL DESCRIPTION

W83782D/G is an evolving version of W83781D/G -- Winbond's most popular hardware status monitoring IC. The W83782D/G can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system to work stable and properly. W83782D/G provides both ISA and I^{2}C™ serial bus interface.

An 8-bit analog-to-digital converter (ADC) was built inside W83782D/G. The W83782D/G can simultaneously monitor 9 analog voltage inputs, 2 fan tachometer inputs, 3 remote temperature, one case-open detection signal. The remote temperature sensing can be performed by thermistors, or 2N3904 NPN-type transistors, or directly from Intel™ Deschutes CPU thermal diode output. Also the W83782D/G provides 4 PWM (pulse width modulation) outputs for the fan speed control; beep tone output for warning; SMI#, OVT#, GPO# signals for system protection events.

Through the application software or BIOS, the users can read all the monitored parameters of system from time to time. And a pop-up warning can be also activated when the monitored item was out of the proper/preset range. The application software could be Winbond's Hardware Doctor™, or Intel™ LDCM (LanDesk Client Management), or other management application software. Also the users can set up the upper and lower limits (alarm thresholds) of these monitored parameters and to activate one programmable and maskable interrupts. An optional beep tone could be used as warning signal when the monitored parameters are out of the preset range.

Additionally, 5 VID inputs are provided to read the VID of CPU (i.e. Pentium™ II) if applicable. This is to provide the Vcore voltage correction automatically. Also W83782D/G uniquely provides an optional feature: early stage (before BIOS was loaded) beep warning. This is to detect if the fatal elements present --- Vcore or +3.3V voltage fail, and the system can not be boomed up. Also there are 3 specific pins to provide selectable address setting for application of multiple devices (up to 8 devices) wired through I^{2}C™ interface.

2. FEATURES

Monitoring Items

- 3 thermal inputs from remote thermistors or 2N3904 NPN-type transistors or Pentium™ II (Deschutes) thermal diode output
- 9 voltage inputs
  - Typical for Vcore, +3.3V, +12V, -12V, +5V, -5V, +5V Vsb, Vbat, and one reserved
- 3 fan speed monitoring inputs
- Case open detection input
- WATCHDOG comparison of all monitored values
- Programmable hysteresis and setting points (alarm thresholds) for all monitored items

Actions Enabling

- Beep tone warning
- 4 PWM (pulse width modulation) outputs for fan speed control (3 are MUX optional)
  - Total up to 3 sets of fan speed monitoring and controlling
- Issue SMI#, OVT#, GPO# signals to activate system protection
- Warning signal pop-up in application software

General

- ISA and I²C™ serial bus interface
- 5 VID input pins for CUP Vcore identification (for Pentium™ II)
- Initial power fault beep (for +3.3V, Vcore)
- Master reset input to W83782D/G
- Independent power plane of digital Vcc and analog Vcc (inputs to IC)
- 3 pins (IA0, IA1, IA2) to provide selectable address setting for application of multiple devices (up to 8 devices) wired through I²C™ interface
- Intel™ LDCM (DMI driver 2.0) support
- Acer™ ADM (DMI driver 2.0) support
- Winbond hardware monitoring application software (Hardware Doctor™) support, for both Windows 95/98 and Windows NT 4.0/5.0
- Input clock rate optional for 24, 48, 14.318 MHz
- 5V Vcc operation

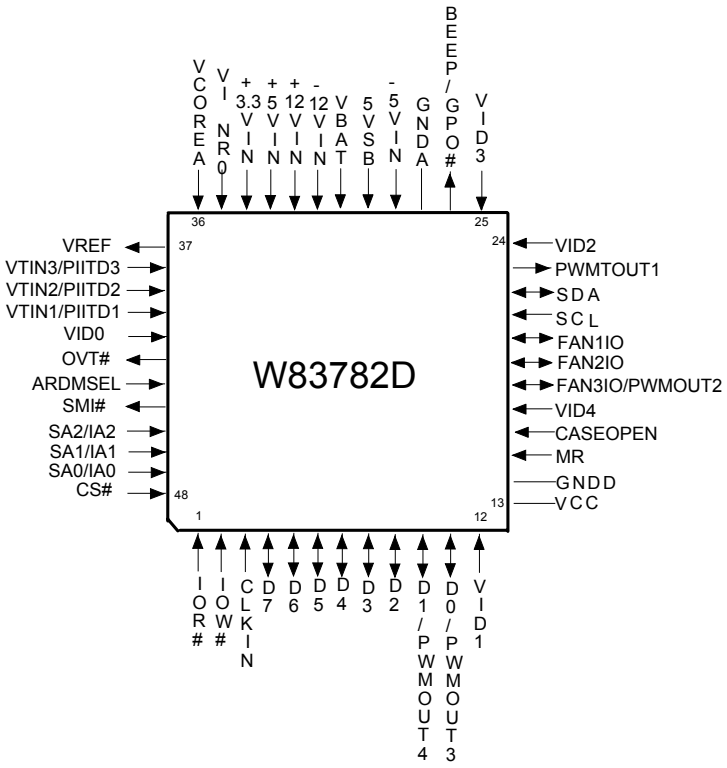
Package

- 48-pin LQFP

3. KEY SPECIFICATIONS

- Voltage monitoring accuracy ±1% (Max.)
- Monitoring Temperature Range and Accuracy
  - – 40°C to +120°C ± 3°C (Max.)
- Supply Voltage 5V
- Operating Supply Current 5 mA typ.
- ADC Resolution 8 Bits

4. PIN CONFIGURATION



5. PIN DESCRIPTION

I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink capability
I/O_{12ts} - TTL level and schmitt trigger
OUT_{12} - Output pin with 12 mA source-sink capability
AOUT - Output pin(Analog)
OD_{12} - Open-drain output pin with 12 mA sink capability
IN_t - TTL level input pin
IN_{ts} - TTL level input pin and schmitt trigger
AIN - Input pin(Analog)

PIN NAME	PIN NO.	TYPE	DESCRIPTION
IOR#	1	IN_{ts}	An active low standard ISA bus I/O Read Control.
IOW#	2	IN_{ts}	An active low standard ISA bus I/O Write Control.
CLKIN	3	IN_{t}	System clock input. Can select 48MHz or 24MHz or 14.318MHz. The default is 24MHz.
D7~D2	4-9	I/O_{12t}	Bi-directional ISA bus Data lines. D0 corresponds to the low order bit, with D7 the high order bit. These pins are activated if pin ADRMSEL=0.
D1 / PWMOUT4	10	I/O_{12t} OUT_{12}	Bi-directional ISA bus Data lines. This pin is activated if pin ADRMSEL=0. / Fan speed control PWM output. This pin is activated if pin ADRMSEL=1.
D0 / PWMOUT3	11	I/O_{12t} OUT_{12}	Bi-directional ISA bus Data lines. This pin is activated if pin ADRMSEL=0. / Fan speed control PWM output. This pin is activated if pin ADRMSEL=1.
VID1	12	IN_{t}	Voltage Supply readouts from P6. This value is read in the VID/Fan Divisor Register.
V_{CC} (+5V)	13	POWER	+5V V_{CC} power. Bypass with the parallel combination of 10μF (electrolytic or tantalum) and 0.1μF (ceramic) bypass capacitors.
GNDD	14	DGROUND	Internally connected to all digital circuitry.
MR	15	IN_{ts}	Master reset input.
CASEOPEN#	16	IN_{t}	CASE OPEN detection. An active low input from an external device when case is opened. This signal can be latched if pin VBAT is connect to battery, even W83782D/G is power off.
VID4	17	IN_{t}	Voltage Supply readouts from P6. This value is read in the bit <0> of Device ID Register.
FAN3IO/ PWMOUT2	18	I/O_{12t}	0V to +5V amplitude fan tachometer input. / Fan speed control PWM output.
FAN2IO-FAN1IO	19-20	I/O_{12t}	0V to +5V amplitude fan tachometer input / Fan on-off control output. These multi-functional pins can be programmable input or output.
SCL	21	IN_{ts}	Serial Bus Clock.
SDA	22	OD_{12}	Serial Bus bi-directional Data.
PWMOUT1	23	OUT_{12}	Fan speed control PWM output.

Pin Description, continued

PIN NAME	PIN NO.	TYPE	DESCRIPTION
VID2	24	IN_t	Voltage Supply readouts from P6. This value is read in the VID/Fan Divisor Register.
VID3	25	IN_t	Voltage Supply readouts from P6. This value is read in the VID/Fan Divisor Register.
BEEP/GPO#	26	OD_{12}	Beep (Default) / General purpose output This multi-functional pin is programmable.
GNDA	27	AGROUND	Internally connected to all analog circuitry. The ground reference for all analog inputs.
-5VIN	28	AIN	0V to 4.096V FSR Analog Inputs.
5VSB	29	AIN	0V to 4.096V FSR Analog Inputs.
VBAT	30	AIN	0V to 4.096V FSR Analog Inputs. (This pin should be connected to 3V BATTERY.)
-12VIN	31	AIN	0V to 4.096V FSR Analog Inputs.
+12VIN	32	AIN	0V to 4.096V FSR Analog Inputs.
+5VIN	33	AIN	This pin is Analog Vcc and connects internal monitor channel IN3 with fixed scale.
+3.3VIN	34	AIN	0V to 4.096V FSR Analog Inputs.
VINR0	35	AIN	0V to 4.096V FSR Analog Inputs.
VCOREA	36	AIN	0V to 4.096V FSR Analog Inputs.
VREF	37	AOUT	Reference Voltage.
VTIN3 / PIITD3	38	AIN	Thermistor 3 terminal input.(Default) / Pentium™ II diode 3 input. This multi-functional pin is programmable.
VTIN2 / PIITD2	39	AIN	Thermistor 2 terminal input. (Default)/ PentiumTM II diode 2 input. This multi-functional pin is programmable.
VTIN1 / PIITD1	40	AIN	Thermistor 1 terminal input. (Default)/ PentiumTM II diode 1 input. This multi-functional pin is programmable.
VID0	41	IN_t	Voltage Supply readouts from P6. This value is read in the VID/Fan Divisor Register.
OVT#	42	OD_{12}	Over temperature Shutdown Output.

Pin Description, continued

PIN NAME	PIN NO.	TYPE	DESCRIPTION
ADRMSEL	43	IN_t	Pin 45--47 mode selection. 0 = The 3 lowest order bits of ISA Address Bus.(Default, internal pull-down 47K ohm) 1 = 7 bit I^2C^{TM} address setting pin.(bit2 - bit0)
SMI#	44	OD_{12}	System Management Interrupt (open drain). This output is enabled when Bit 1 in the Configuration Register is set to 1. The default state is disabled.
SA2-SA0 IA2, IA1, IA0	45-47	IN_t IN_t	The three lowest order bits of the 16-bit ISA Address Bus. A0 corresponds to the lowest order bit. (Default, when ARDMSEL =0 or left open) The hardware setting pin of 7 bit I^2C^{TM} serial address bit2, bit1 and bit0 at CR[48h]. (When ARDMSEL =1)
CS#	48	IN_t	Chip Select input from an external decoder which decodes high order address bits on the ISA Address Bus. This is an active low input.

6. FUNCTIONAL DESCRIPTION

6.1 General Description

The W83782D/G provides 7 analog positive inputs, 3 fan speed monitors, at most 4 sets for fan PWM (Pulse Width Modulation) control, 3 thermal inputs from remote thermistors or 2N3904 transistors or Pentium™ II (Deschutes) thermal diode outputs, case open detection and beep function output when the monitor value exceed the set limit value including voltage, temperature, or fan counter. When starting the monitor unction on the chip, the watch dog machine monitors every function and stores the value to registers. If the monitor value exceeds the limit value, the interrupt status will be set to 1.

6.2 Access Interface

The W83782D/G provides two interfaces for microprocessor to read/write internal registers.

6.2.1 ISA interface

The first interface uses ISA Bus to access which the ports of low byte (bit2~bit0) are defined in the port 5h and 6h. The high byte (from ISA address bus bit15~bit3) of these ports is decoded by Chip Select (CS#), the general decoded address is set to port 295h and port 296h. These two ports are described as following:

Port 295h: W83782D/G Index register port.

Port 296h: Data port.

The register structure is showed as the Figure 1.

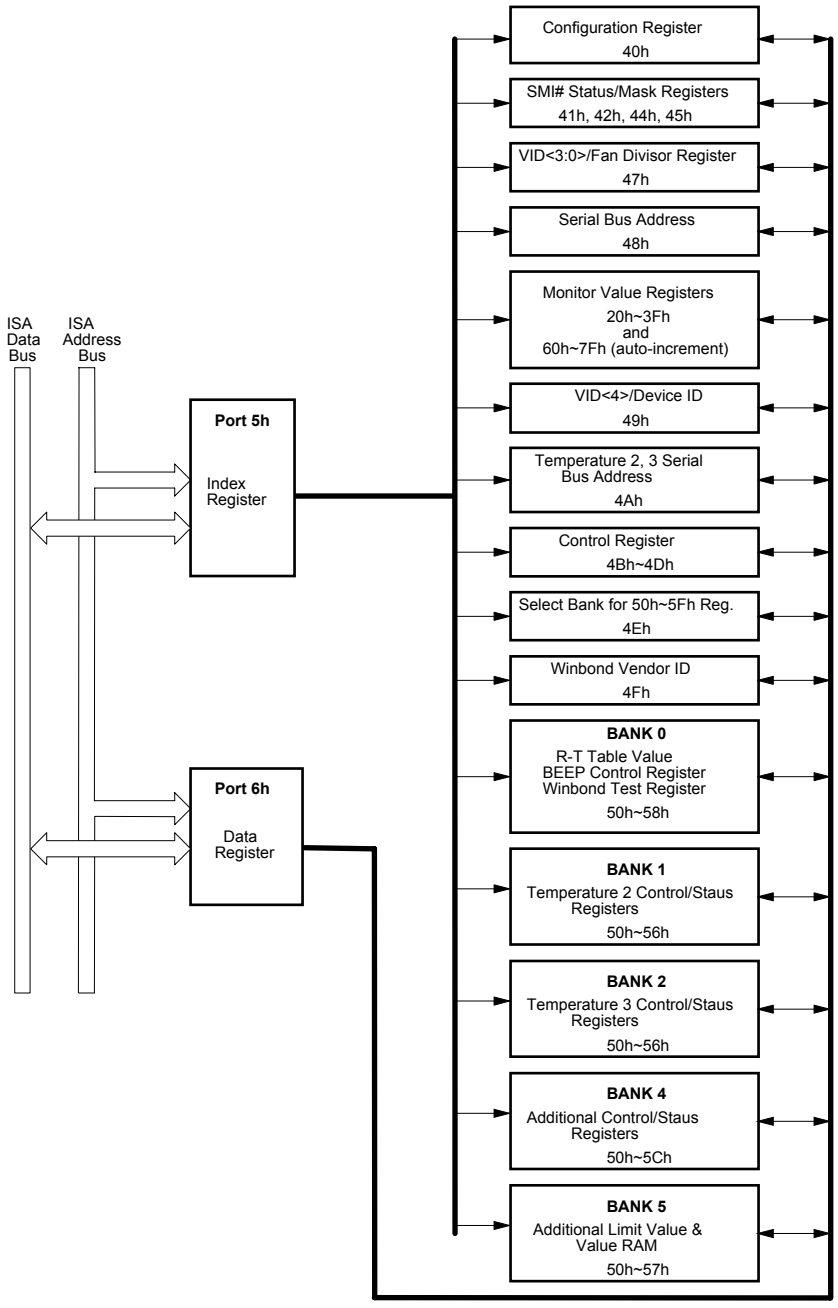


Figure 1. ISA interface access diagram

6.2.2 I²C interface

The second interface uses I²C Serial Bus. In the W83782D/G has three serial bus addresses. That is, the first address defined at CR [48h] can read/write all registers excluding Bank 1 and Bank 2 temperature sensor 2/3 registers. The second address defined at CR [4Ah] bit2-0 only read/write temperature sensor 2 registers, and the third address defined at CR [4Ah] bit6-4 only can access (read/write) temperature sensor 3 registers.

The first serial bus address of W83782D/G has 3 hardware setting bits set by pin47-45 when pin 43 is set to high. The address is 00101[pin45] [pin46] [pin47]. If pin45=1, pin46=1, pin47=0, for example, the content of CR [48h] is 0101110. If CR [4Ah] bit 2-0 is XXX, the temperature sensor 2 serial address is 1001XXXG, in which G is the read/write bit. If CR [4Ah] bit 6-4 is YYY, the temperature sensor 3 serial address is 1001YYYG, in which G is the read/write bit.

6.2.3 The first serial bus access timing is shown as follows:

(a) Serial bus write to internal address register followed by the data byte

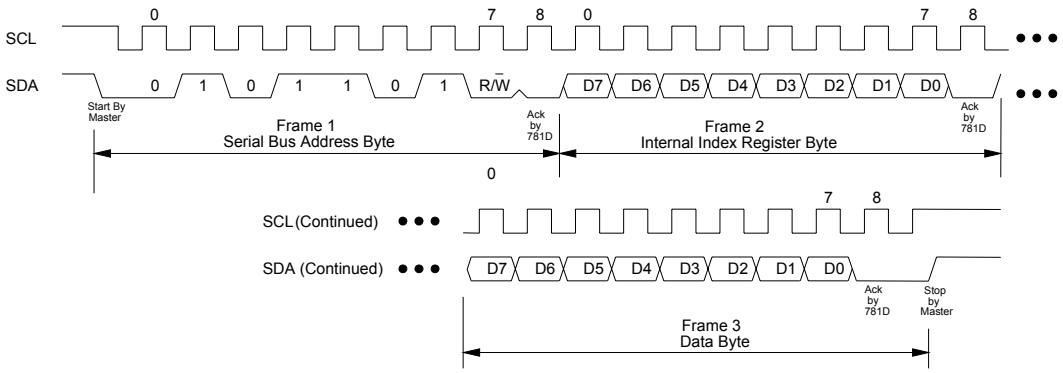


Figure 2. Serial Bus Write to Internal Address Register followed by the Data Byte

(b) Serial bus write to internal address register only

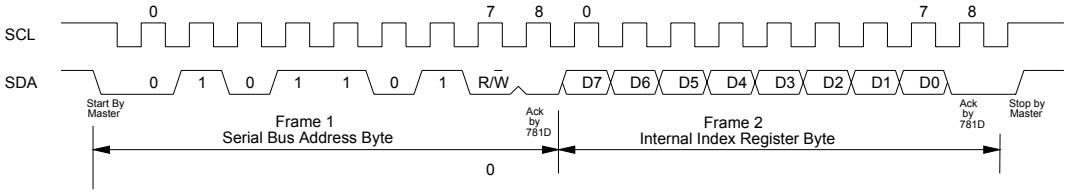


Figure 3. Serial Bus Write to Internal Address Register Only

(c) Serial bus read from a register with the internal address register prefer to desired location

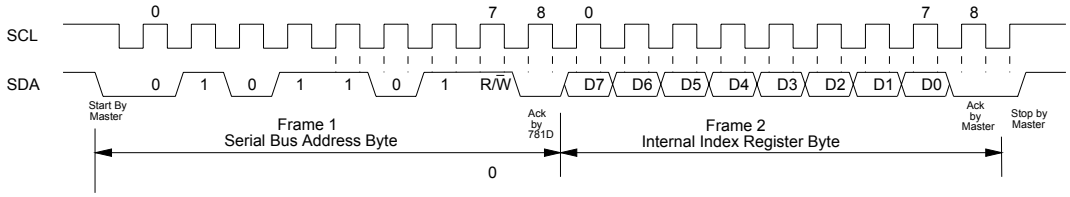


Figure 4. Serial Bus Write to Internal Address Register Only

6.2.4 The serial bus timing of the temperature 2 and 3 is shown as follow:

(a) Typical 2-byte read from preset pointer location (Temp, T_{OS}, T_{HYST})

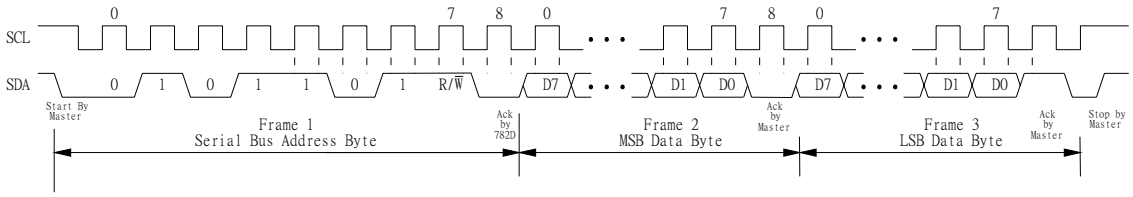


Figure 5. Typical 2-Byte Read From Preset Pointer Location

(b) Typical pointer set followed by immediate read for 2-byte register (Temp, T_{OS}, T_{HYST})

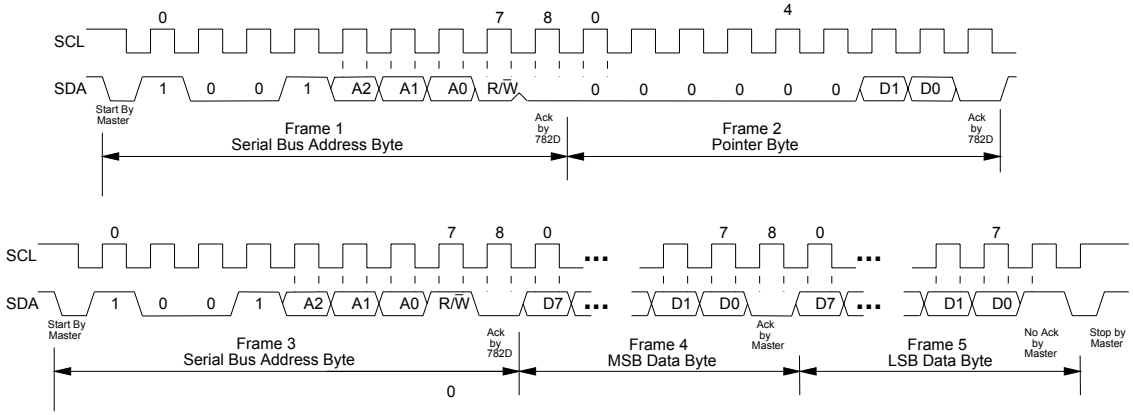


Figure 6. Typical Pointer Set Followed by Immediate Read for 2-Byte Register

(c) Typical read 1-byte from configuration register with preset pointer

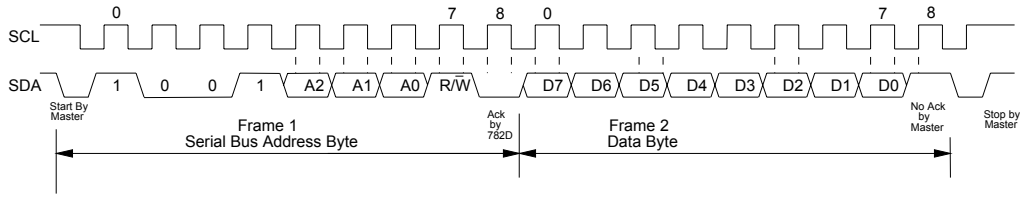


Figure 7. Typical 1-Byte Read From Configuration With Preset Pointer

(d) Typical pointer set followed by immediate read from configuration register

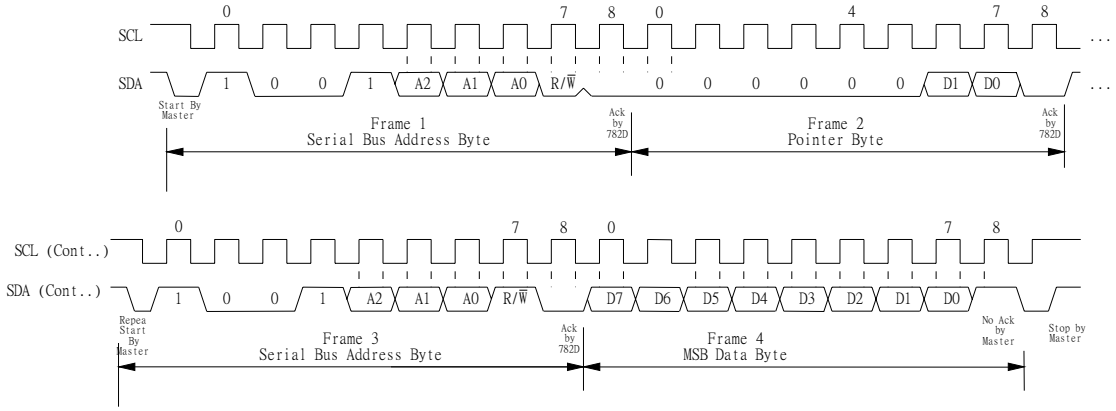


Figure 8. Typical Pointor Set Followed by Immediate Read from Temp 2/3 Configuration Register

(e) Temperature 2/3 configuration register Write

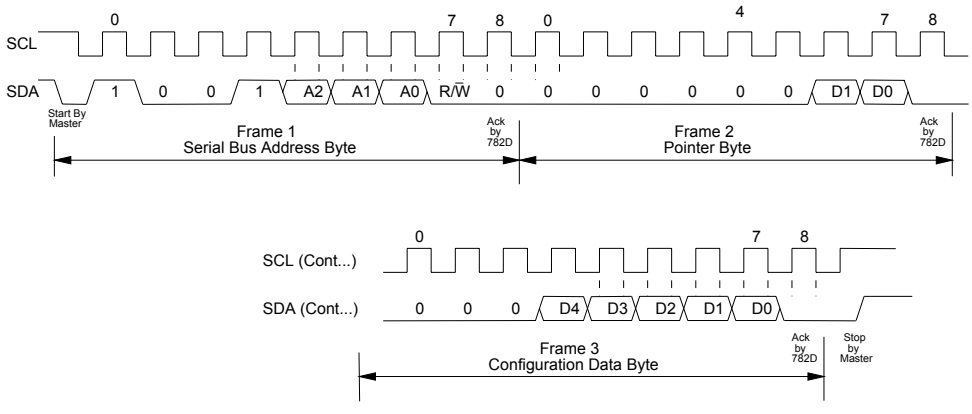


Figure 9. Configuration Register Write

(f) Temperature 2/3 T_{OS} and T_{HYST} write

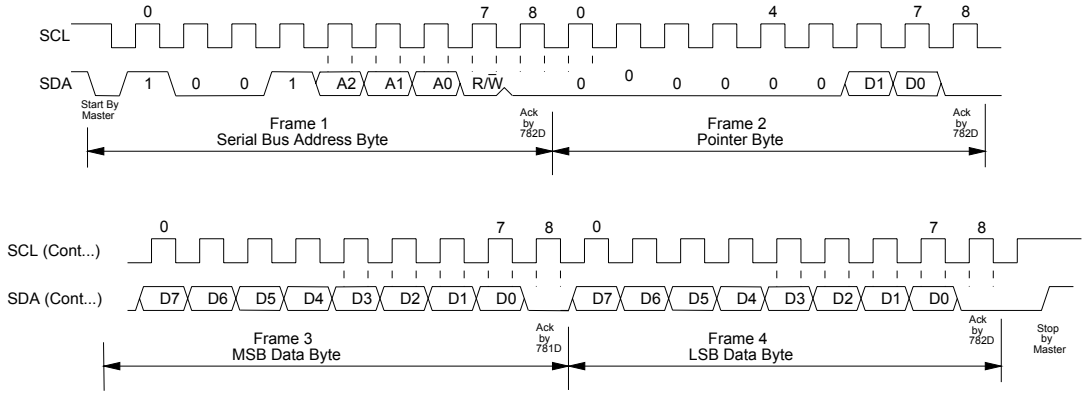


Figure 10. Configuration Register Write

6.3 Analog Inputs

The maximum input voltage of the analog pin is 4.096V because the 8-bit ADC has a 16mv LSB. Really, the application of the PC monitoring would most often be connected to power suppliers. The CPU V-core voltage, +3.3V and battery voltage can directly connect to these analog inputs. The 5VSB and +12V inputs should be reduced a factor with external resistors so as to obtain the input range. As Figure 11 shows.

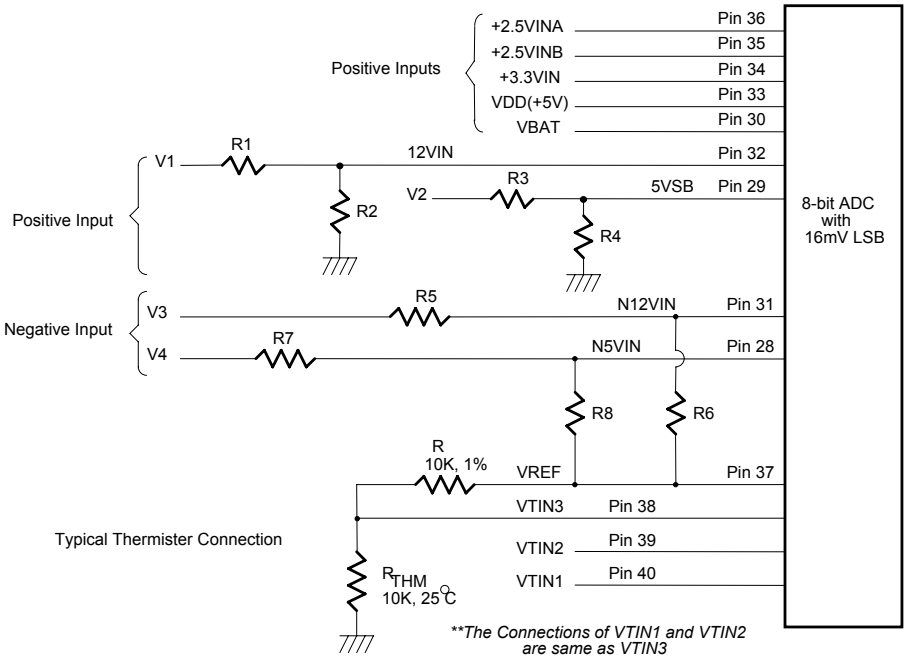


Figure 11.

6.3.1 Monitor over 4.096V voltage:

The input voltage +12VIN can be expressed as following equation.

$$12VIN = V_1 \times \frac{R_2}{R_1 + R_2}$$

The value of R1 and R2 can be selected to 28K Ohms and 10K Ohms, respectively, when the input voltage V1 is 12V. The node voltage of +12VIN can be subject to less than 4.096V for the maximum input range of the 8-bit ADC. Similarly, the node voltage of 5VSB (measure standby power VSB for ATX power supply) also can be evaluated by using two series resistors R3 and R4 which real value can be 5.1K ohms and 7.5K ohms so as to obtain the 5VSB is limited to less than 4.096V. The Pin 33 is connected to the power supply VCC with +5V. There are two functions in this pin with 5V. The first function is to supply internal analog power in the W83782D/G and the second function is that this voltage with 5V is connected to internal serial resistors to monitor the +5V voltage. The values of two serial resistors are 34K ohms and 50K ohms so that input voltage to ADC is 2.98V which is less than 4.096V of ADC maximum input voltage. The express equation can represent as follows.

$$V_{in} = VCC \times \frac{50K\Omega}{50K\Omega + 34K\Omega} \cong 2.98V$$

where VCC is set to 5V.

6.3.2 Monitor negative voltage:

The negative voltage should be connected two series resistors and a positive voltage VREF (is equal to 3.6V). In the Figure 11, the voltage V3 and V4 are two negative voltages which are -12V and -5V, respectively. The voltage V3 is connected to two serial resistors then is connected to another terminal VREF which is positive voltage. So as that the voltage node N12VIN can be obtain a posedge voltage if the scales of the two serial resirtors are carefully selected. It is recommended from Winbond that the scale of two serial resistors are R5=232K ohms and R6=56K ohm. The input voltage of node -12VIN can be calculated by following equation.

$$N12VIN = (VREF + |V_5|) \times (\frac{232K\Omega}{232K\Omega + 56K\Omega}) + V_5$$

where VREF is equal 3.6V.

If the V_5 is equal to -12V then the voltage is equal to 0.567V and the converted hexdecimal data is set to 35h by the 8-bit ADC with 16mV-LSB.This monitored value should be converted to the real negative voltage and the express equation is shown as follows.

$$V_5 = \frac{N12VIN - VREF \times \beta}{1 - \beta}$$

Where β is 232K/(232K+56K). If the N2VIN is 0.567 then the V5 is approximately equal to -12V.

The other negative voltage input V6 (approximate -5V) also can be evaluated by the similar method and the serial resistors can be selected with R7=120K ohms and R8=56K ohms by the Winbond recommended. The expression equation of V6 With -5V voltage is shown as follows.

$$V_6 = \frac{N5VIN - VREF \times \gamma}{1 - \gamma}$$

Where the β is set to 120K/(120K+56K). If the monitored ADC value in the N5VIN channel is 0.8635, VREF=3.6V and the parameter β is 0.6818 then the negative voltage of V6 can be evalated to be -5V.

6.3.3 Monitor temperature from thermistor

The W83782D/G can connect three thermistors to measure three different envirment temperatures. The specification of thermistor should be considered to (1) β value is 3435K, (2) resistor value is 10K ohms at 25°C. In the Figure 11, the themistor is connected by a serial resistor with 10K Ohms, then connect to VREF (Pin 37).

6.3.4 Monitor temperature from Pentium II™ thermal diode or bipolar transistor 2N3904

The W83782D/G can alternate the thermistor to Pentium II™ (Deschutes) thermal diode interface or transistor 2N3904 and the circuit connection is shown as Figure 12. The pin of Pentium II™ D- is connected to power supply ground (GND) and the pin D+ is connected to pin PIITDx in the W83782D/G. The resistor R=30K ohms should be connected to VREF to supply the diode bias current and the bypass capacitor C=3300pF should be added to filter the high frequency noise. The transistor 2N3904 should be connected to a form with a diode, that is, the Base (B) and Collector (C) in the 2N3904 should be tied together to act as a thermal diode.

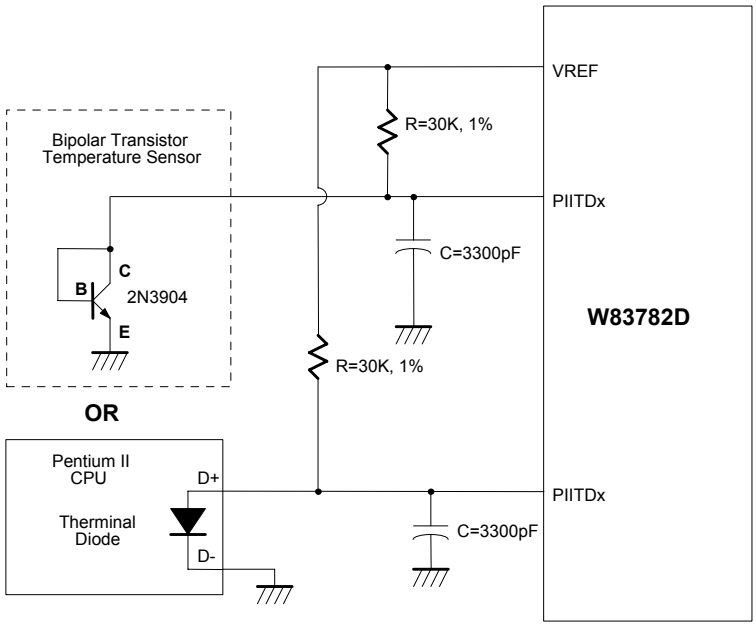


Figure 12.

6.4 FAN Speed Count and FAN Speed Control

6.4.1 Fan speed count

Inputs are provides for signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage can not be over +5.5V. If the input signals from the tachometer outputs are over the VCC, the external trimming circuit should be added to reduce the voltage to obtain the input specification. The normal circuit and trimming circuits are shown as Figure 13.

Determine the fan counter according to:

$$\text{Count} = \frac{1.35 \times 10^6}{\text{RPM} \times \text{Divisor}}$$

In other words, the fan speed counter has been read from register CR28 or CR29 or CR2A, the fan speed can be evaluated by the following equation.

$$RPM = \frac{1.35 \times 10^6}{Count \times Divisor}$$

The default divisor is 2 and defined at CR47.bit7~4, CR4B.bit7~6, and Bank0 CR5D.bit5~7 which are three bits for divisor. That provides very low speed fan counter such as power supply fan. The followed table is an example for the relation of divisor, PRM, and count.

DIVISOR	NOMINAL PRM	TIME PER REVOLUTION	COUNTS	70% RPM	TIME FOR 70%
1	8800	6.82 ms	153	6160	9.74 ms
2 (default)	4400	13.64 ms	153	3080	19.48 ms
4	2200	27.27 ms	153	1540	38.96 ms
8	1100	54.54 ms	153	770	77.92 ms
16	550	109.08 ms	153	385	155.84 ms
32	275	218.16 ms	153	192	311.68 ms
64	137	436.32 ms	153	96	623.36 ms
128	68	872.64 ms	153	48	1246.72 ms

Table 1

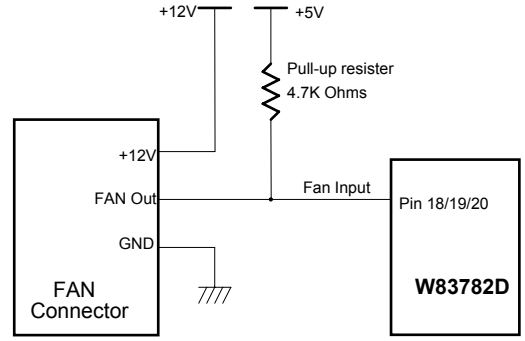


Figure 13-1. Fan with Tach Pull-Up to +5V

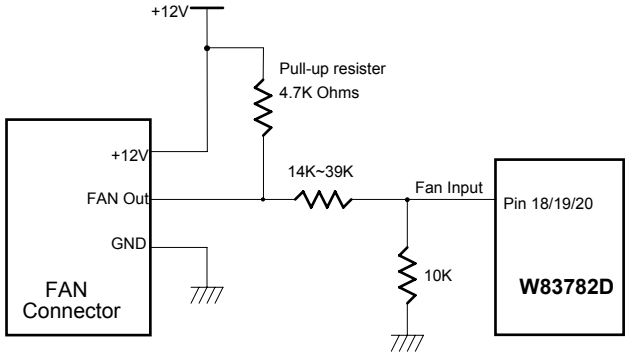


Figure 13-2. Fan with Tach Pull-Up to +12V, or Totem-Pole Output and Register Attenuator

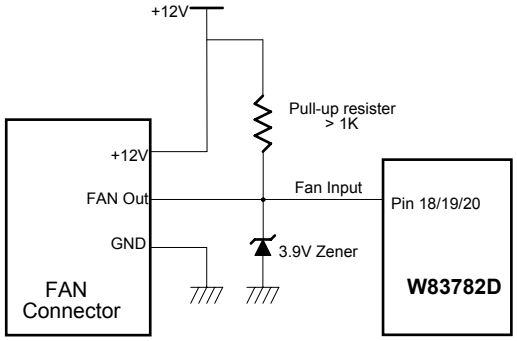


Figure 13-3. Fan with Tach Pull-Up to +12V and Zener Clamp

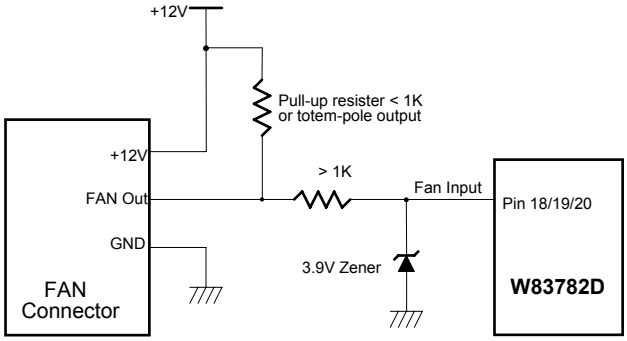


Figure 13-4. Fan with Tach Pull-Up to +12V, or Totem-Pole Putput and Zener Clamp

Fan speed control

The W83782D/G provides four sets for fan PWM speed control. The duty cycle of PWM can be programmed by an 8-bit registers which are defined in the Bank0 CR5A, CR5B, CR5E, and CR5F. The default duty cycle is set to 100%, that is, the default 8-bit registers is set to FFh. The expression of duty can be represented as follows.

$$\text{Duty} - \text{cycle}(\%) = \frac{\text{Programmed 8 - bit Register Value}}{255} \times 100\%$$

The PWM clock frequency also can be program and defined in the Bank0.CR5C and Bank4.CR5C. The application circuit is shown as follows.

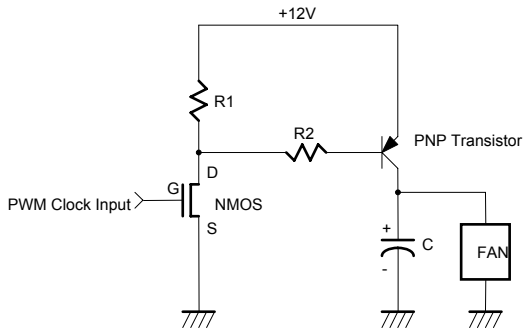


Figure 14.

6.5 Temperature Measurement Machine

The temperature data format is 8-bit two - complement for sensor 1 and 9-bit two - complement for sensor 2/3. The 8-bit temperature data can be obtained by reading the CR [27h]. The 9-bit temperature data can be obtained by reading the 8 MSBs from the Bank1/2 CR [50h] and the LSB from the Bank1/2 CR [51h] bit 7. The format of the temperature data is show in Table 1.

TEMPERATURE	8-BIT DIGITAL OUTPUT		9-BIT DIGITAL OUTPUT	
	8-Bit Binary	8-Bit Hex	9-Bit Binary	9-Bit Hex
+125°C	0111,1101	7Dh	0,1111,1010	0FAh
+25°C	0001,1001	19h	0,0011,0010	032h
+1°C	0000,0001	01h	0,0000,0010	002h
+0.5°C	-	-	0,0000,0001	001h
+0°C	0000,0000	00h	0,0000,0000	000h
-0.5°C	-	-	1,1111,1111	1FFh
-1°C	1111,1111	FFh	1,1111,1110	1FFh
-25°C	1110,0111	E7h	1,1100,1110	1CEh
-55°C	1100,1001	C9h	1,1001,0010	192h

Table 2

6.5.1 The W83782D/G temperature sensor 1 SMI# interrupt has two modes

(1) Comparator Interrupt Mode

Setting the T_{HYST} (Temperature Hysteresis) limit to 127°C will set temperature sensor 1 SMI# to the Comparator Interrupt Mode. Temperature exceeds T_O (Over Temperature) Limit causes an interrupt and this interrupt will be reset by reading all the Interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_O, the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding T_O and not reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below T_O. (Figure 16-1)

(2) Two-Times Interrupt Mode

Setting the T_{HYST} lower than T_O will set temperature sensor 1SMI# to the Two-Times Interrupt Mode. Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will not occur. (Figure 15-2)

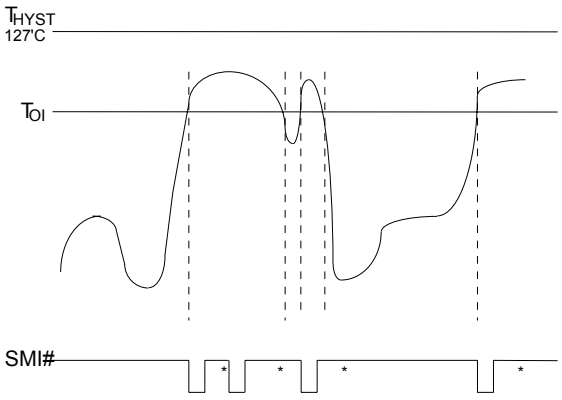


Figure 15-1. Comparator Interrupt Mode

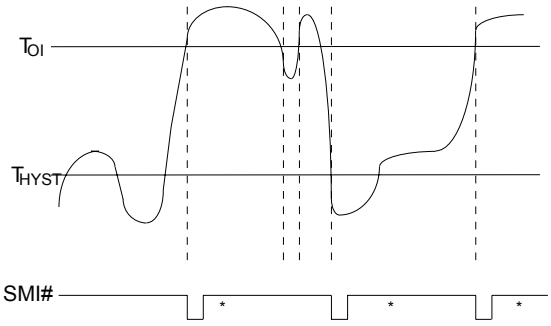


Figure 15-2. Two-Times Interrupt Mode

*Interrupt Reset when Interrupt Status Registers are read

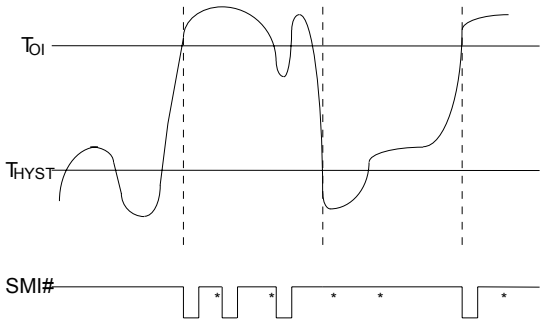
6.5.2 The W83782D/G temperature sensor 2 and sensor 3 SMI# interrupt has two modes and it is programmed at CR [4Ch] bit 6.

(1) Comparator Interrupt Mode

Temperature exceeding T_O causes an interrupt and this interrupt will be reset by reading all the Interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding T_O and not reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below T_{HYST}. (Figure 16-1)

(2) Two-Times Interrupt Mode

Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will not occur. (Figure 16-2)



*Interrupt Reset when Interrupt Status Registers are read

Figure 16-1. Comparator Interrupt Mode

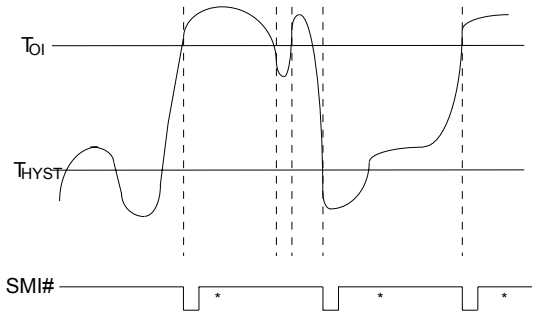


Figure 16-2. Two-Times Interrupt Mode

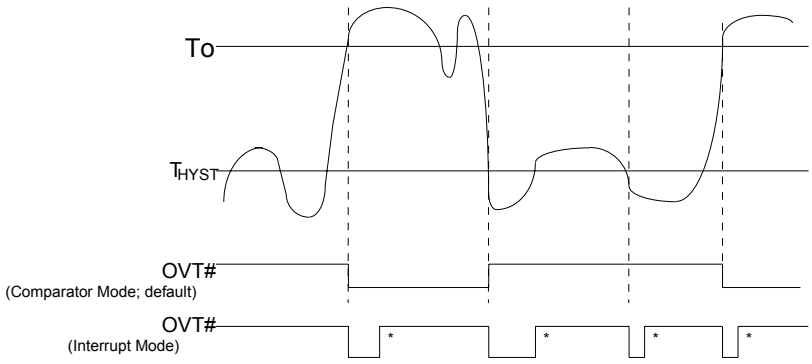
6.5.3 The W83782D/G temperature sensor 2 and 3 Over-Temperature (OVT#) has two modes, and they are programmed at Bank1 and Bank2 CR [52h] bit1. These two bits needs to be programmed the same value.

(1) Comparator Mode:

Temperature exceeding T_O causes the OVT# output activated until the temperature is less than T_{HYST}. (Figure 17)

(2) Interrupt Mode:

Temperature exceeding T_O causes the OVT# output activated indefinitely until reset by reading temperature sensor 2 or sensor 3 registers. Temperature exceeding T_O, then OVT# reset, and then temperature going below T_{HYST} will also cause the OVT# activated indefinitely until reset by reading temperature sensor2 or sensor 3 registers. Once the OVT# is activated by exceeding T_O, then reset, if the temperature remains above T_{HYST}, the OVT# will not be activated again. (Figure 17)



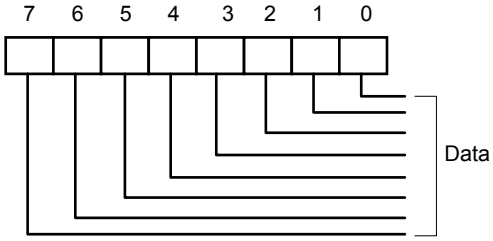
*Interrupt Reset when Temperature 2/3 is read

Figure 17. Over-Temperature Response Diagram

7. REGISTERS AND RAM

7.1 Address Register (Port x5h)

Data Port: Port x5h
Power on Default Value 00h
Attribute: Bit 6:0 Read/write, Bit 7: Read Only
Size: 8 bits



Bit7: Read Only

The logical 1 indicates the device is busy because of a Serial Bus transaction or another ISA bus transaction. With checking this bit, multiple ISA drivers can use W83782D/G without interfering with each other or a Serial Bus driver.

It is the user's responsibility not to have a Serial Bus and ISA bus operations at the same time.

This bit is:

Set: with a write to Port x5h or when a Serial Bus transaction is in progress.

Reset: with a write or read from Port x6h if it is set by a write to Port x5h, or when the Serial Bus transaction is finished.

Bit 6-0: Read/Write

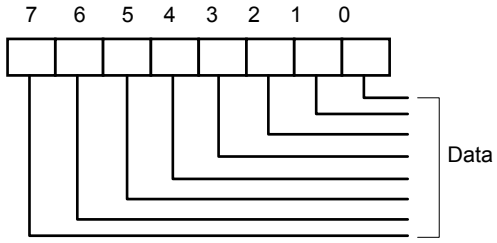
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Busy	Address Pointer (Power On default 00h)						
(Power On default 0)	A6	A5	A4	A3	A2	A1	A0

Address Pointer Index (A6-A0)

Registers and RAM	A6-A0 in Hex	Power On Value of Registers: <k7:0>in Binary	Notes
Configuration Register	40h	00001000	
Interrupt Status Register 1	41h	00000000	Auto-increment to the address of Interrupt Status Register 2 after a read or write to Port x6h.
Interrupt Status Register 2	42h	00000000	
SMI#Ý Mask Register 1	43h	00000000	Auto-increment to the address of SMIÝ Mask Register 2 after a read or write to Port x6h.
SMIÝ Mask Register 2	44h	00000000	
NMI Mask Register 1	45h	00000000	Auto-increment to the address of NMI Mask Register 2 after a read or write to Port x6h
NMI Mask Register 2	46h	01000000	
VID/Fan Divisor Register	47h	<7:4> = 0101; <3:0> = VID3-ID0	
Serial Bus Address Register	48h	<6:0> = 0101101; <7> = 0	
POST RAM	00-1Fh		Auto-increment to the next location after a read or write to Port x6h and stop at 1Fh.
Value RAM	20-3Fh		
Value RAM	60-7Fh		Auto-increment to the next location after a read or write to Port x6h and stop at 7Fh.

7.2 Data Register (Port x6h)

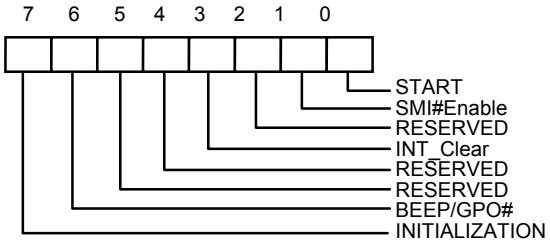
Data Port: Port x6h
Power on Default Value 00h
Attribute: Read/write
Size: 8 bits



Bit 7-0: Data to be read from or to be written to RAM and Register.

7.3 Configuration Register – Index 40h

Register Location: 40h
Power on Default Value 00000001 binary
Attribute: Read/write
Size: 8 bits



Bit 7: A one restores power on default value to all registers except the Serial Bus Address register. This bit clears itself since the power on default is zero.

Bit 6: The logical 1 in this bit drives a zero on BEEP/GPO# pin.

Bit 5: Reserved

Bit 4: Reserved

Bit 3: A one disables the SMI# output without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.

Bit 2: Reserved

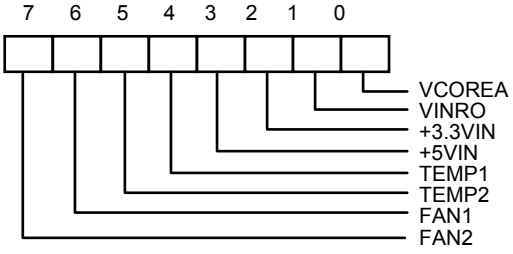
Bit 1: A one enables the SMI# Interrupt output.

Bit 0: A one enables startup of monitoring operations, a zero puts the part in standby mode.

Note: The outputs of Interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred unlike "INT_Clear" bit.

7.4 Interrupt Status Register 1 – Index 41h

Register Location: 41h
Power on Default Value 00h
Attribute: Read Only
Size: 8 bits



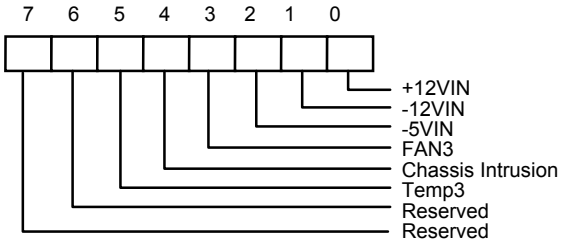
Bit 7: A one indicates the fan count limit of FAN2 has been exceeded.

Bit 6: A one indicates the fan count limit of FAN1 has been exceeded.

Bit 5: A one indicates a High limit of VTIN2 has been exceeded from temperature sensor 2.
Bit 4: A one indicates a High limit of VTIN1 has been exceeded from temperature sensor 1.
Bit 3: A one indicates a High or Low limit of +5VIN has been exceeded.
Bit 2: A one indicates a High or Low limit of +3.3VIN has been exceeded.
Bit 1: A one indicates a High or Low limit of VINR0 has been exceeded.
Bit 0: A one indicates a High or Low limit of VCOREA has been exceeded.

7.5 Interrupt Status Register 2 – Index 42h

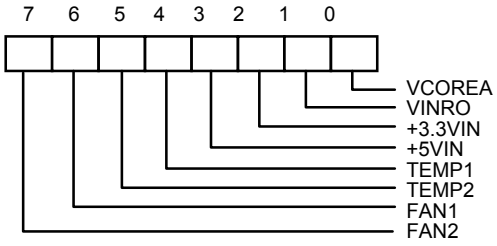
Register Location: 42h
Power on Default Value 00h
Attribute: Read Only
Size: 8 bits



Bit 7-6:Reserved.This bit should be set to 0.
Bit 5: A one indicates a High limit of VTIN3 has been exceeded from temperature sensor 3.
Bit 4: A one indicates Chassis Intrusion has gone high.
Bit 3: A one indicates the fan count limit of FAN3 has been exceeded.
Bit 2: A one indicates a High or Low limit of -5VIN has been exceeded.
Bit1: A one indicates a High or Low limit of -12VIN has been exceeded.
Bit0: A one indicates a High or Low limit of +12VIN has been exceeded.

7.6 SMI# Mask Register 1 – Index 43h

Register Location: 43h
Power on Default Value 00h
Attribute: Read/Write
Size: 8 bits



Bit 7-0: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.