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W83791D/W83791G
Winbond H/W
Monitoring IC

W83791D/W83791G
Data Sheet Revision History

	PAGES	DATES	VERSION	VERSION ON WEB	MAIN CONTENTS
1	n.a.			n.a.	All version before 0.50 are for internal use.
2	n.a.	01/Jan	0.5	n.a.	First publication.
3	P.7 P.34	01/Jan	0.51	n.a.	(1) Revise SLOTOCC# pin description. (2) Add SMI# /IRQ for Voltage/Fan description.
4	P.43/44	01/Mar	0.6	n.a.	Register Index 1Ah~1Fh revised.
5	P. 40 P. 42 P. 60/61 P. 58/59 P. 66 P. 66 P. 66 P. 87	01/May	0.7	n.a.	This update is for **C version** IC. 1) Add EVNTRAP1-5 polarity (Index Ah) 2) Add VID protection control bit (Index15h bit5) 3) Add FAN1-3/PWMOUT1-3 as GPIn data register. (Index 95h/97h) 4) SMARTFAN™ step up/down time registers exchanged. 5) Add a bit (Index A6 bit7) to know either speech or GPIO function did you use. 6) Pin44 (SMI#/LEDOUT) is a multi-function, it is programmable. 7) EVENTRAP can as GPIO by programming Index A6h bit0-4 . 8) Updated V0.17 schematics adding LEDOUT circuit for SMI# (Pin 44)
6	All pages	01/Aug	0.71	n.a.	Repaginate datasheet
7	n.a.	02/Apr	1.0	1.0	Change all version include version on web to 1.0
8	n.a.	06/Apr	1.1	1.1	Add lead-free package version

winbond

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1. GENERAL DESCRIPTION

W83791D/G is an evolving version of the W83782D/G --- Winbond's most popular hardware status monitoring IC. Besides the conventional functions of W83782D/G, W83791D/G uniquely provides several innovative features such as speech function, ASF sensor compliant, SMBus 2.0 ARP command compatible, VID table selection trapping, and 5VID output control. Conventionally, W83791D/G can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system to work stably and efficiently. As for data access, W83791D/G provides slave SMBus 2.0 interface which can reply PEC (Packet Error Code) when as ASF sensor.

An 8-bit analog-to-digital converter (ADC) was built inside W83791D/G. W83791D/G can simultaneously monitor 10 analog voltage inputs (including power VDD/5VSB monitoring), 5 fan tachometer inputs, 3 remote temperatures, and one case open detection signal. The sense of remote temperature can be performed by thermistors, 2N3904 NPN-type transistors, or directly from Intel™ CPU with thermal diode output. W83791D/G provides 3 PWM (pulse width modulation) outputs for two modes of smart fan control-**"** Thermal Cruise™ **"** mode and **"**Speed Cruise**"** mode. Under **"** Thermal Cruise™ **"** mode, temperatures of CPU and the system can be maintained within specific programmable ranges under the hardware control. **"**Speed Cruise**"**, namely, is to keep the fan operate in the specific programmable r.p.m. As for warning mechanism, W83791D/G provides speech voice warning, beep tone warning, and SMI#, OVT#, IRQ signals for system protection events.

Additionally, 5 VID inputs are provided to read the VID of CPU (i.e. Pentium™ II/III) if applicable. These VID inputs provide the information of Vcore voltage that CPU expects. Furthermore, W83791D/G provides programmable VID output control to alter the voltage CPU consumes. W83791D/G also uniquely provides an optional feature: early stage (before BIOS was loaded) beep / speech warning to detect if the fatal elements present --- Vcore or +3.3V voltage fail and thus the system can not be boomed up. If the VSB power on setting refers to Intel VRM 9.x, the VID table within W83791D/G will be according to the new one. W83791D/G also has 2 specific pins to provide selectable address setting for application of multiple devices (up to 4 devices) wired through I^2C™ interface.

W83791D/G speech function is enabled by building in a programmable speech synthesizer with a 9-bit current DAC output as well as a connectable external flash memory for storing voice data. W83791D/G supports 1 CPU present or absent event trap, 5 external event traps, 17 hardware monitor event traps (10 analog voltage, 3 fan tachometer, 3 remote temperature, 1 case open) and 128 internal programmable event traps, amounting to 151 different speech outputs. If more than two events happen simultaneously, the priority set is: SLOTOCC# > EVNTRP1 > EVNTRP2 > EVNTRP3 > EVNTRP4 > EVNTRP5 > 128 Programmable events (Bank0 index 09h) > 17 Hardware status events. Voice data stored in the external flash memory interface with Winbond W55FXX is flexible to change by Winbond application software and **on-line** programming flash data is provided also. Besides, an external resistor is added to provide ring oscillator.

When you do not use the speech function, W83791D/G provides a set of flexible I/O control functions to the system designer through a set of General Purpose I/O ports. These GPIO ports may serve as simple I/O or may be individually configured to provide a pre-defined alternate function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.

W83791D/G can uniquely serve as an ASF sensor to respond to ASF master's request for the implementation of network management in OS-absent state. Through W83791D/G compliance with ASF sensor spec, network server is able to monitor the environmental status of the client in OS-absent state by PET frame values returned from W83791D/G, such as temperatures, voltages, fan speed, and case open. Moreover, W83791D/G supports SMBus 2.0 ARP command to solve the problem of address conflicts by dynamically assigning a new unique address to W83791D/G after W83791D/G's UDID is sent.

Through the application software or BIOS, the users can read all the monitored parameters of the system from time to time. A pop-up warning can also be activated when the monitored item is out of the proper/preset range. The application software could be Winbond's Hardware Doctor™, Intel™ LDCM (LanDesk Client Management), or other management application software. Besides, the users can set up the upper and lower limits (alarm thresholds) of these monitored parameters and activate one programmable and maskable interrupts. An optional beep tone could be used as a warning signal when the monitored parameters are out of the preset range.

2. FEATURES

2.1 Monitoring Items

- 10 voltage inputs
  --- Typical for VCORE, +3.3V, +12V, -12V, +5V, -5V, +5VSB, VBAT, and two reserved
- 5 fan speed monitoring inputs
- 3 temperature inputs from remote thermistors, 2N3904 NPN-type transistors or Pentium™ II (Deschutes) thermal diode output
- Case open detection input
- WATCHDOG comparison of all monitored values
- Programmable hysteresis and setting points (alarm thresholds) for all monitored items

2.2 Address Resolution Protocol (ARP) and Alert-Standard Forum (ASF)

- Support System Management Bus (SMBus) version 2.0 specification
- Comply with hardware sensor slave ARP (Address Resolution Protocol)
- Response sensor type ARP command
- Response ASF command --- Get Event Data , Get Event Status
- Comply with ASF sensors (Monitoring fan speed, voltage, temperature, and case open)

2.3 Speech Items

- Programmable speech synthesizer with new high fidelity synthesis algorithm
- Build in 8-bit current D/A converter
- 1 CPU present or absent trigger input
- 5 External trigger inputs
- 128 Internal programmable trigger inputs
- 17 H/W Monitor event trigger inputs
- Programmable 0-255 seconds timeout trigger inputs for firmware or software
- Instruction cycle is <= 400 uS typically
- Section control provided in each voice section
- External resistor for ring oscillator

2.4 Actions Enabling

- Beep tone warning separated speech output
- 5 PWM (pulse width modulation) outputs for fan speed control (1~3 support Smart Fan control) and 5 Fan speed inputs for monitoring --- Total up to 5 sets of fan speed monitoring and controlling
- Issue SMI#, OVT#, IRQ signals to activate system protection
- Warning signal pop-up in application software

2.5 Enhance Monitoring VID function

- CPU Voltage ID reading
- VID output control
- Enhance beep warning by detecting Intel VRM 9.0 VID

2.6 General

- I^2C^{TM} serial bus interface
- 5 VID input pins for CPU VCORE identification (for Pentium™ II/III)
- Initial power fault beep (for +3.3V, VCORE)
- 2 pins (A0, A1) to provide selectable address setting for application of multiple devices (up to 4 devices) wired through I^2C^{TM} interface

Winbond hardware monitoring application software (Hardware Doctor™) support, for both Windows 95/98/2000 and Windows NT 4.0/5.0

- Internal clock Oscillator with 3M Hz
- 5V VSB operation

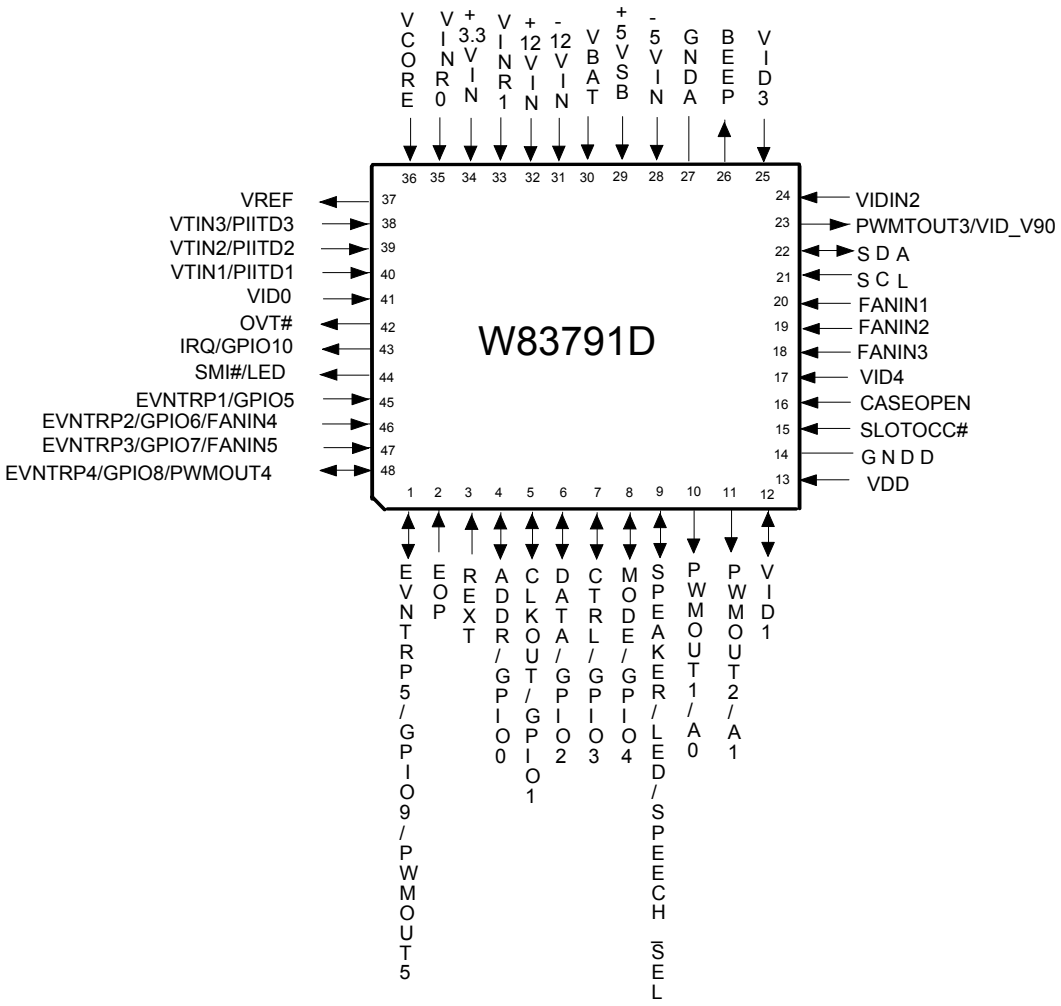
2.7 Package

- 48-pin LQFP

3. KEY SPECIFICATIONS

• Voltage monitoring accuracy	±1% (Max)
• Intel VRM 9.x Voltage monitoring accuracy	±0.5% (Max)
• Monitoring Temperature Range and Accuracy	
- 40°C to +120°C	± 3°C(Max)
• Supply Voltage	5V
• Operating Supply Current	5 mA typ.
• ADC Resolution	8 Bits

4. PIN CONFIGURATION



5. PIN DESCRIPTION

I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink capability
I/O_{12ts} - TTL level and schmitt trigger with 12 mA source-sink capability
I/O_{8ts} - TTL level and schmitt trigger with 8 mA source-sink capability
I/O_{6ts} - TTL level and schmitt trigger with 6 mA source-sink capability
I/OD_{12ts} - TTL level and schmitt trigger open drain output with 12 mA sink capability
OUT_{12} - Output pin with 12 mA source-sink capability
OD_{12} - Open-drain output pin with 12 mA sink capability
AOUT - Output pin (Analog)
IN_t - TTL level input pin
IN_{ts} - TTL level input pin and schmitt trigger
AIN - Input pin (Analog)

PIN NAME	PIN NO.	TYPE	DESCRIPTION
EVNTRP5 /	1	I/O_{12t}	Event trapping to selection speech output sound. Default is high edge trigger.
GPIO9/ PWMOUT5			General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active. The I/O control and status is defined in BANK0 Index 13h~14h. Otherwise, GPIO pin or PWMOUT Fan control can be selected by registers, but the PWMOUT can not support Smart Fan.
EOP	2	I	End of Process signal input from cascaded Flash.
GPIO11		I/OD_{12ts}	General purpose I/O function pin. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.
REXT	3	I	Resistor (Rosc) connect to VSB used to adjust ring oscillator frequency.
ADDR /	4	OUT_{12}	Speech address pulse output, connect to W55FXX. When this pin translates from logic high to logic low, it will latch the data pin 6 and shift it into a speech flash address counter.
GPIO0		I/OD_{12ts}	General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.
CLKOUT /	5	OUT_{12}	Speech clock output, for speech data read-out and write-in, connect to W55FXX. When this pin translates from logic high to logic low, the data pin 6 will be latched by this clock.
GPIO1		I/OD_{12ts}	General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.

PIN DESCRIPTION, continued

PIN NAME	PIN NO.	TYPE	DESCRIPTION
DATA /	6	I/O_{12t}	Serial data input/output, connect to W55FXX. The pin is latched by CLKOUT and ADDR acted as speech data and address respectively.
GPIO2		I/OD_{12ts}	General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.
CTRL /	7	OUT_{12}	Output clock numbers of this pin decide which mode is selected. Connect to W55FXX.
GPIO3		I/OD_{12ts}	General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.
MODE /	8	OUT_{12}	Output mode signal to W55FXX serial Flash.
GPIO4		I/OD_{12ts}	General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.
SPEAKER	9	OUT_{12}	Current type output driving an external speaker. The function is only working in VDD 5V OK.
LED		OUT_{12}	LED output control. This is a multi-function pin with SPEAKER. When the LED_SEL register (Bank0 Index 17h) is set to 1, LED output function will be active. Otherwise, set to 0 (default), this pin serves as SPEAKER output.
SPEECH_SEL		IN_{ts}	During VSB 5V power on, this pin is used to trap whether using speech function or GPIO function. Trapping low means using speech function (i.e. pin45-48, pin1, pin4-8 are as speech function). Trapping high means using GPIO function (i.e. pin45-48, pin1, pin4-8 are as GPIO function). The I/O control and status is defined in BANK0 Index 13h~16h.
PWMOUT1/	10	OUT_{12}	Fan speed control PWM output. When the power of VDD is 0v, this pin will drive logic 0. The power of this pin is supplied by VSB 5V.
A0		IN_{ts}	I^2C device address bit0 trapping during 5VSB power on.
PWMOUT2 /	11	OUT_{12}	Fan speed control PWM output. When the power of VDD is 0v, this pin will drive logic 0. The power of this pin is supplied by VSB 5V.
A1		IN_{ts}	I^2C device address bit1 trapping during 5VSB power on.
VID1	12	I/O_{12ts}	Voltage Supply readouts from CPU. After programming, this pin can be VID output to voltage regulator to generate Vcore for CPU.

PIN DESCRIPTION, continued

PIN NAME	PIN NO.	TYPE	DESCRIPTION
VDD (5V)	13	POWER	+5V VDD power. Bypass with the parallel combination of 10μF (electrolytic or tantalum) and 0.1μF (ceramic) bypass capacitors.
GNDD	14	DGROUND	Internally connected to all digital circuitry.
SLOTOCC#	15	IN_{ts}	CPU presence signal. 0 means CPU is present. 1 means CPU is absent.
CASEOPEN	16	I/O_{6ts}	CASE OPEN detection. An active high input from an external device when case is Intruded. This signal can be latched in external circuit which power is supplied by VBAT, even if W83791D/G is power off.
VID4	17	I/O_{12ts}	Voltage Supply readouts from CPU. After programming, this pin can be VID output to voltage regulator to generate Vcore for CPU.
FAN3IN-FAN1IN	18-20	IN_{ts}	0V to +5V amplitude fan tachometer input
SCL	21	IN_{ts}	Serial Bus Clock.
SDA	22	I/OD_{8ts}	Serial Bus bi-directional Data.
PWMOUT3 /	23	OUT_{12}	Fan speed control PWM output. When the power of VDD is 0v, this pin will drive logic 0. The power of this pin is supplied by VSB 5V.
VID_V90		IN_{ts}	VID table selection trapping during RSMRST (0: Intel VRM 8.2/8.3; 1: Intel VRM 9.0). When the trapping pin get a logic 1, the beep warning function is according to Intel VRM 9.0 VID.
VID2	24	I/O_{12ts}	Voltage Supply readouts from CPU. After programming, this pin can be VID output to voltage regulator to generate Vcore for CPU.
VID3	25	I/O_{12ts}	Voltage Supply readouts from CPU. After programming, this pin can be VID output to voltage regulator to generate Vcore for CPU.
BEEP	26	OD_{12}	Alarm beep output. Normal, this pin is low. When abnormal event happens, this pin will output alarm frequency.
GNDA	27	AGROUND	Internally connected to all analog circuitry. The ground reference for all analog inputs.
-5VIN	28	AIN	0V to 4.096V FSR Analog Inputs.
+5VSB	29	POWER	This pin is power for W83791D/G. Bypass with the parallel combination of 10μF (electrolytic or tantalum) and 0.1μF (ceramic) bypass capacitors.
VBAT	30	POWER	This pin is power for W83791D/G.

PIN DESCRIPTION, continued

PIN NAME	PIN NO.	TYPE	DESCRIPTION
-12VIN	31	AIN	0V to 4.096V FSR Analog Inputs.
+12VIN	32	AIN	0V to 4.096V FSR Analog Inputs.
VINR1	33	AIN	0V to 4.096V FSR Analog Inputs.
+3.3VIN	34	AIN	0V to 4.096V FSR Analog Inputs.
VINR0	35	AIN	0V to 4.096V FSR Analog Inputs.
VCORE	36	AIN	0V to 4.096V FSR Analog Inputs.
VREF	37	AOUT	Reference voltage.
VTIN3 / PIITD3	38	AIN	Thermistor 3 terminal input. (Default) Pentium™ II diode 3 input. This multi-functional pin is programmable.
VTIN2 / PIITD2	39	AIN	Thermistor 2 terminal input. (Default) Pentium™ II diode 2 input. This multi-functional pin is programmable.
VTIN1 / PIITD1	40	AIN	Thermistor 1 terminal input. (Default) Pentium™ II diode 1 input. This multi-functional pin is programmable.
VID0	41	I/O_{12ts}	Voltage Supply readouts from CPU. After programming, this pin can be VID output to voltage regulator to generate Vcore for CPU.
OVT#	42	OD_{12}	Over temperature Shutdown Output for temperature sensor 1-3.
IRQ / GPIO10	43	OUT_{12} I/OD_{12ts}	Interrupt request. General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.
SMI# / LED	44	OD_{12} OUT_{12}	System Management Interrupt (open drain). LED output control. This is a multi-function pin with SMI. When the register (Bank0 Index 17h bit7 and Index A6h bit 6) is set to 1, LED output function will be active. Otherwise, set to 0 (default), this pin serves as SMI#.
EVNTRP1/ GPIO5	45	I/O_{12ts}	Event trapping to selection speech output sound. Default is high edge trigger. General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this speech function will be active. The I/O control and status is defined in BANK0 Index 13h~14h. Otherwise, GPIO pin can be selected by registers.

PIN DESCRIPTION, continued

PIN NAME	PIN NO.	TYPE	DESCRIPTION
EVNTRP2-3/	46-47	I/O_{12ts}	Event trapping to selection speech output sound. Default is high edge trigger.
GPIO6-7/ FANIN4-5		I/O_{12ts}	General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this speech function will be active. The I/O control and status is defined in BANK0 Index 13h~14h. Otherwise, GPIO pin or FAN inputs can be selected by registers.
EVNTRP4/	48	I/O_{12ts}	Event trapping to selection speech output sound.
GPIO8/ PWMOUT4		I/O_{12ts}	General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active. The I/O control and status is defined in BANK0 Index 13h~14h. Otherwise, GPIO pin or PWMOUT Fan control can be selected by registers, but the PWMOUT can not support Smart Fan.

6. FUNCTION DESCRIPTION

6.1 General Description

The W83791D/G provides 10 analog positive inputs, 5 fan speed inputs , at most 5 sets for fan PWM (Pulse Width Modulation) control, 3 thermal inputs from remote thermistors, 2N3904 transistors or Pentium™ II/III (Deschutes) thermal diode outputs, case open detection and beep function output when the monitored values exceed preset ranges, including the voltage, temperature, and fan count. Moreover, W83791D/G uniquely provides several innovative and practical functions to make the whole system more efficient and compliant with future trend of network management, such as speech function, ASF sensor compliant, SMBus 2.0 ARP command compatible, VID table selection trapping, 5VID output control, and so forth. Once the monitoring function of W83791D/G is enabled, the watch dog machine will monitor every function and store the values to registers for comparison with preset ranges. If the monitoring value exceeds the limit value, the interrupt status will be set to 1 and W83791D/G will issue interrupt signals such as SMI# and IRQ if not masked..

6.2 Access Interface

The W83791D/G provides I^2C Serial Bus for microprocessor to read/write internal registers. In the W83791D/G, there are three serial bus addresses. Through the first address defined at CR [48h], all the registers can be read and written except CPUT1/CPUT2 temperature sensor registers. The read/write of the CPUT1/CPUT2 temperature sensor registers can be implemented through the second address (defined at CR [4Ah] bit2-0) and the third address (defined at CR [4Ah] bit6-4).

The first serial bus address of W83791D/G has 2 hardware setting bits set by pin10-11. The address is 001011[pin11], and [pin10]. Hence, the content of CR [48h] would be 00101110 if pin11=1 and pin10=0.

6.2.1 The first serial bus access timing

(a) Serial bus writes to internal address register followed by the data byte

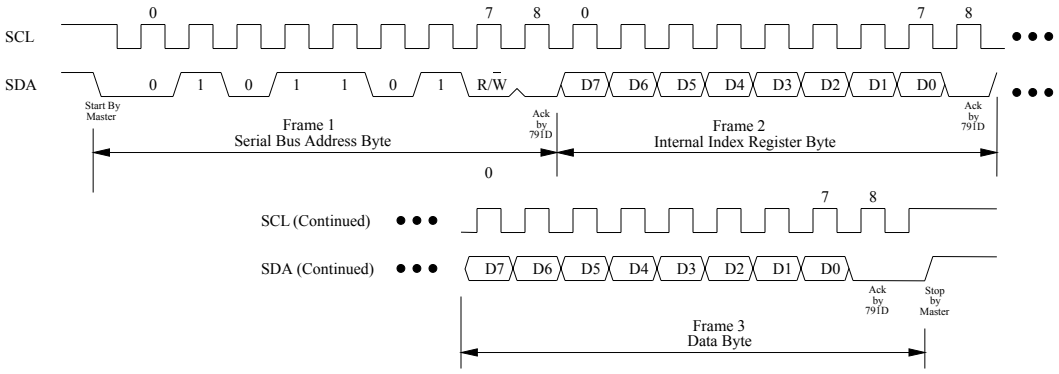


Figure 1. Serial Bus Write to Internal Address Register followed by the Data Byte

(b) Serial bus read from a register

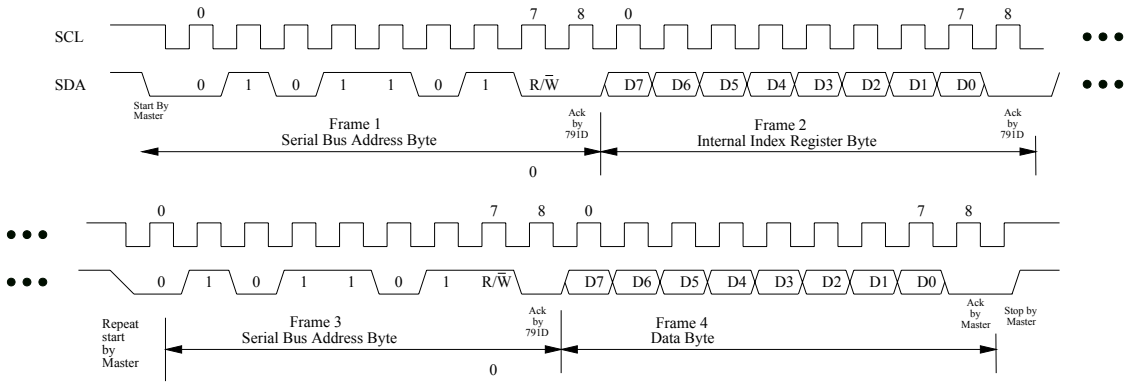


Figure 2. Serial Bus Read from Internal Address Register

6.3 Speech Function

6.3.1 General Description

The W83791D/G is a derivative of Winbond's *PowerSpeech*™ synthesizers. There are up to 5 hardware trigger inputs, 17 Hardware Monitor event and 128 programmable software event trigger inputs. If more than two events happen simultaneously, the priority set by the internal H/W is: SLOTOCC# > EVNTRAP1 > EVNTRAP2 > EVNTRAP3 > EVNTRAP4 > EVNTRAP5 > TRIGREG (Index 09h) 128 events > VIN0 > VIN1> others (VIN2 –VIN9, TEMP, FAN, case open). Software trigger is able to accommodate 128 event triggers, with timeout register (index 08h) enabled in advance for allowance of time on detecting devices. That is, once the system's power is on, BIOS can fill trigger event and speech voice will not be sent till the system fails owing to timeout. In addition, to prevent events from taking place simultaneously.

6.3.2 Event Trigger Queue

W83791D/G provides 8 byte FIFO queue to store event trigger, for example, the first 8 event can be served by speech and speech will clear FIFO queue after service. Coding of Speech program must assign correct CPU_MODE event vector to issue correct speech voices correspondent to speech trigger events. For example, CPU_MODE event vector =1 represents absence of CPU, then coding speech with CPU is absent voice. When W83791D/G detects no CPU exists, it will send vector = 1 to speech synthesizer and play this voice data. Following is the block diagram of the 8-Byte event trigger queue.

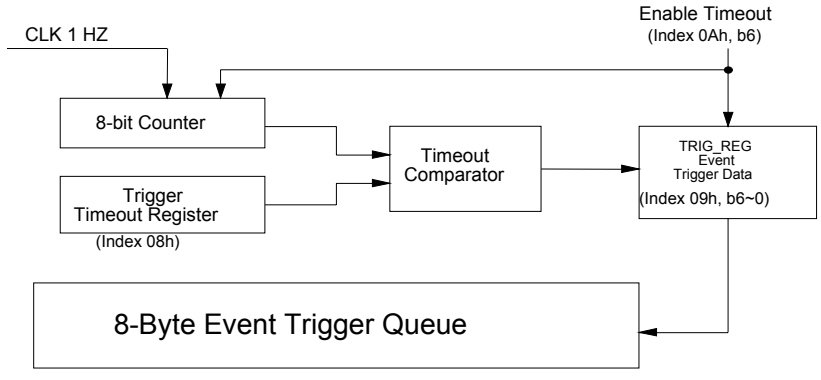


Figure 3. Event trigger Queue

As BIOS usually has POST (Power On Self Test) program, then it will test every item step by step if no failure takes place, however, if it detects a failure on a specific item, it will hang on there. Therefore, BIOS could write timeout value to register 08h and start timer setup speech trigger event (register 09h), then is BIOS test program started. Whenever the system is hang on specific item such as DRAM testing, W83791D would say “DRAM test fails” after the timeout previously set at CR [08h]. On the contrary, if DRAM test is ok, then BIOS could update the timeout value and proceed to the next test program.

Below is the speech CPU_MODE table of W83791D/G**:**

CPU_MODE ITEM	DEFINITION	VECTOR (H)
POI	Reserverd	0,32
SLOTOCC	CPU present or absent	1
EVNTRAP1(TG1)	Hardware trgger1	2
EVNTRAP2	Hardware trgger2	3
EVNTRAP3	Hardware trgger3	4
EVNTRAP4	Hardware trgger4	5
EVNTRAP5	Hardware trgger5	6
TRIGREG	I2C setting software trigger	80-FF
IN0	Vcore(VIN0) exceed limit	40
IN1	VINR0(VIN1) exceed limit	41
IN2	(+3.3VIN)VIN2 exceed limit	42
IN3	(5VDD)VIN3 exceed limit	43
IN4	(+12VIN)VIN4 exceed limit	44
IN5	(-12VIN)VIN5 exceed limit	45
IN6	(-5VIN)VIN6 exceed limit	46
IN7	VSB(VIN7) exceed limit	47
IN8	VBAT(VIN8) exceed limit	48
IN9	(VINR1)VIN9 exceed limit	49
TEMP1	VTIN1 exceed limit	4A
TEMP2	VTIN2 exceed limit	4B
TEMP3	VTIN3 exceed limit	4C
FAN1	FAN1 count over limit	4D
FAN2	FAN2 count over limit	4E
FAN3	FAN3 count over limit	4F
CHS_EV	Case open trigger	50

Table 1 CPU_MODE

6.3.3 Connection of EEPROM

As described previously the W83791D/G has connectable W55FXX to store voice data. To expand the storage capacity, users can select many W55FXX to connect with each other. The maximum capacity could be up to 16Mbit. Following is the connection chart of W55FX with W83791D/G.

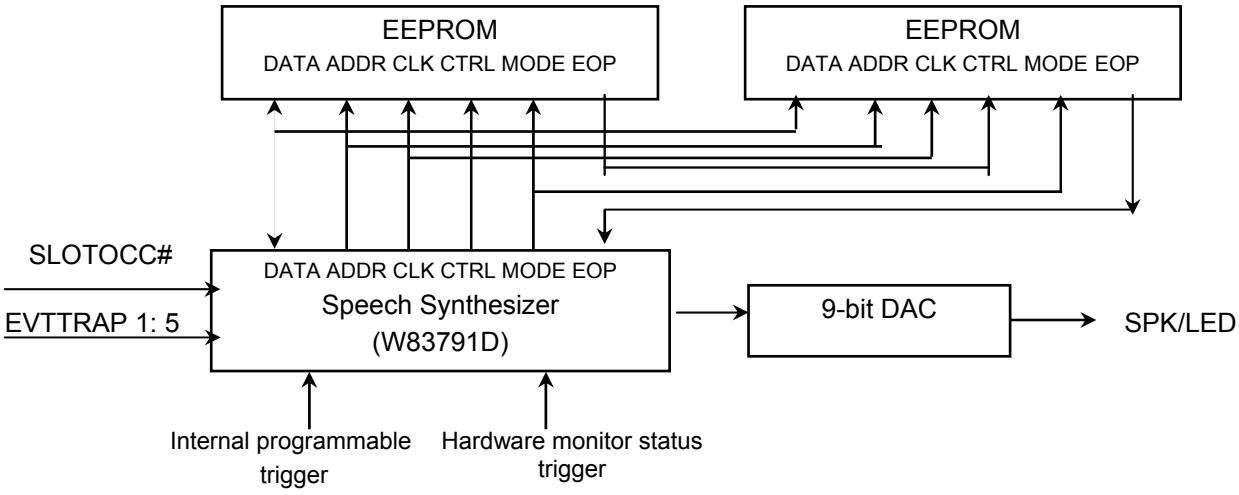


Figure 4 Speech Function Diagram

6.3.4 Speaker Output

Speech output pin is a 8 bit Current D/A converter, with which loading is needed. The resistor could range from 510~1K ohm and bipolar could be a low power NPN bipolar with β of 120 - 160. Usually, an 8050D transistor is appropriate. The spec of speaker is 8 Ω. Besides, SPK can also connect to AC97 codec chip Line_Out. C is decouple capacitor and is usually 200p- 0.01uF

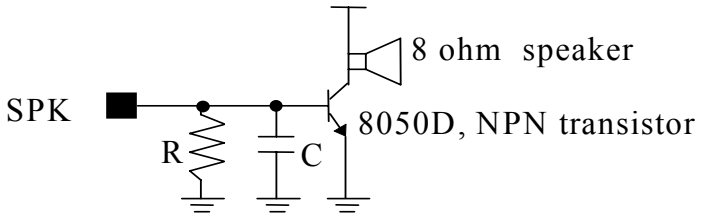


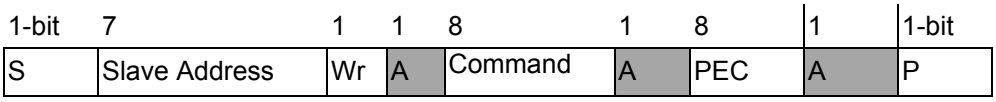
Figure. 5

6.4 Address Resolution Protocol (ARP) Introduction

As the W8791D/G is a slave device existing on the System Management Bus, it must have a unique address to prevent itself from conflicting with the other devices existing on the same bus. In order to solve the problem of address conflicts, SMBus version 2.0 introduces the concept of dynamically assigned address called Address Resolution Protocol (ARP). By such mechanism, each device existing on the SMBus will be given a unique slave address if it is a ARP-capable device. Thus, to meet the new spec, W83791D/G uniquely provides ARP compliant function to acquire a unique slave address.

The typical process of ARP contains several steps, including Prepare to ARP, Reset Device, Get UDID, Assign Address, and so on. Whenever the slave device accepts the command of ARP master, it must reply an Acknowledgement to the ARP master, thus the ARP master is able to carry on the next step. In order to provide a mechanism to isolate device for the purpose of address assignment, each device must implement a unique device identifier (UDID). The UDID is a 128-bit number comprised of several field, including Device Capabilities, Version Revision, Vendor ID, Device ID, Interface, Subsystem Vendor ID, Subsystem Device ID, and Vendor Specific ID. After the UDID of the device is sent to the ARP master, the ARP master will then assign a random address not in the Used Address Pool to the device

Generally speaking, there are eleven possible commands to read /write the data of SMBus device, and a slave device may use any or all of the eleven protocols to communicate. These protocols are Quick Command, Send Byte, Receive Byte, Write Byte, Write Word, Read Byte, Read word, Process Call, Block Write, and Block Write-Block Read Process Call. W83791D/G itself supports the Block Write-Block Read Process with PEC to communicate with ARP Master. Following is a description of the SMBus packet protocol diagrams element key. Not all protocol elements will be present in every command, that is, not all packets are required to include the Packet Error Code.



S	Start Condition
Sr	Repeated Start Condition
Rd	Read (bit value of 1)
Wr	Write (bit value of 0)
A	Acknowledge (this bit position may be '0' for an ACK or '1' for a NACK)
P	Stop Condition
PEC	Packet Error Code
	Master-to-Slave
	Slave-to-Master

Relative command list:

SLAVE ADDRESS	COMMAND	DESCRIPTION
C2h	01h	Prepare to ARP
C2h	02h	Reset device (general)
C2h	03h	Get UDID (general)
C2h	04h	Assign address
C2h	Slave_Addr | 1	Direct Get UDID
C2h	Slave_Addr | 0	Direct Reset
C2h	05h-1Fh	Reserved.

Following is an example of the Block Write-Block Read Process Call. The Block Write-Block Read Process Call is a two-part message. It begins with a salve address and a write condition. After the command code the host issues a write count M that describes how many more bytes will be written in the first part of the message. The second part of the message is a block of read data beginning with a repeated start condition followed by thee salve address and a Read Bit. The next read byte count N indicates how many more data will be read in the second part of the message. Note that the combined data payload must not exceed 32bytes. Besides, W83791D/G also provides packet error code (PEC) to insure the accuracy during data transmission.

1	7	1	1	8	1	8	1	8	1	
S	Slave Address	Wr	A	Command Code	A	Byte Count=M	A	Data Byte 1	A	…

8	1	…	8	1	
Data Byte 2	A	…	Data Byte M	A	…

1	7	1	1	8	1	8	1	1
Sr	Slave Address	Rd	A	Byte Count=N	A	Data Byte 1	A	…

8	1	…	8	1	8	1	1
Data Byte 2	A	…	Data Byte N	A	PEC	A	P

6.5 ASF (Alert Standard Format) Introduction

In order to implement network management in OS-absent, W83791D/G provides ASF Response Registers to meet ASF sensor spec. As a result, the network server is able to monitor several environmental status of the client in OS-absent by PET frame values returned from W83791D/G, including temperature, voltage, fan speed, and case open. In below is the ASF diagram:

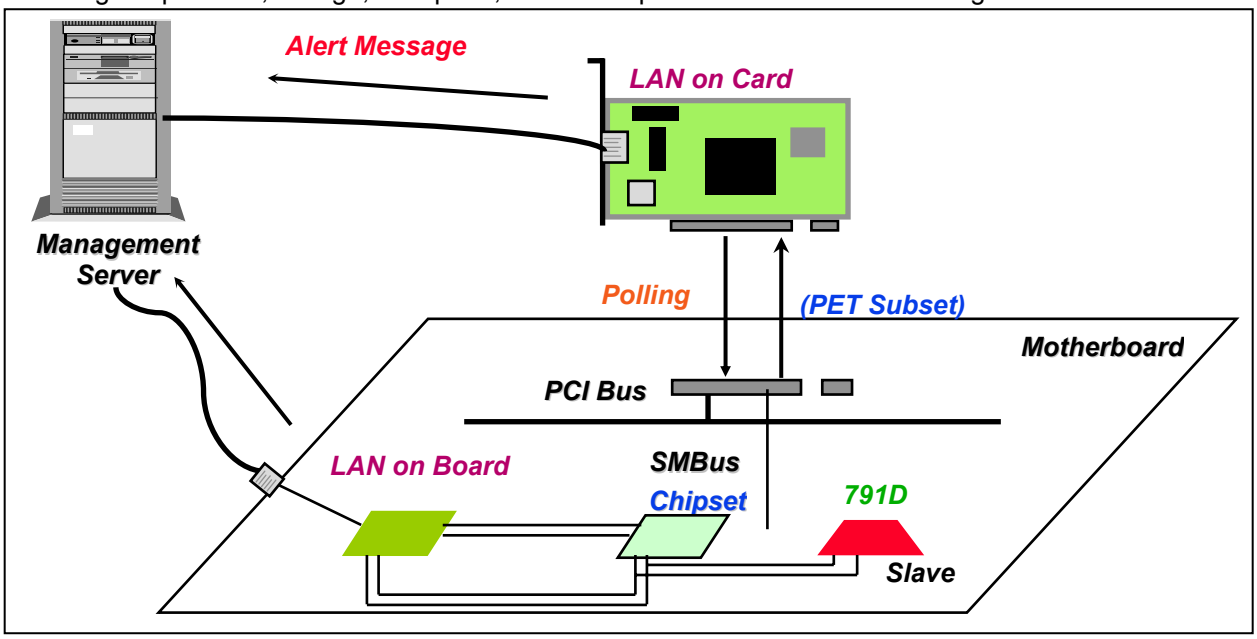


Figure 6. ASF Block Diagram

6.5.1 Platform Event Trap (PET)

PET is the ASF transmit protocol used to provide common fields for trap regardless of trap source. The variable bindings fields in a PET frame contain the system and sensor information for an event, such as event sensor type, event type, event offset, event source type, sensor device, sensor number, entity ID, entity instance, event status index, event status, and event severity. Each field has its definition and is described in the following table.

PET VARIABLE BINDING FIELD	DESCRIPTION
Event Sensor Type	The Event Sensor Type field indicates what types of events the sensor is monitoring. E.g. temperature, voltage, fan, etc.
Event Type	The Event Type indicates what type of transition/state change triggered the trap.
Event Offset	The Event Offset indicates which particular event occurred for a given Even Type.
Event source Type	The Event Source Type describes the originator of the event. It is ASF1.0 (68h) for all PET frames defined by this specification.

Platform Event Trap (PET), continued.

PET VARIABLE BINDING FIELD	DESCRIPTION
Sensor Device	The Sensor Device is the SMBus address of the sensor that caused the event for the PET frame.
Sensor Number	The Sensor Number is used to identify a given instance of a sensor relative to the Sensor Device.
Entity ID	The Entity ID indicates the platform entity the event is associated with. E.g. processor, system board, etc.
Entity Instance	The Entity Instance indicates which instance of the Entity the event is for. E.g. processor 1 or processor 2.
Event Status Index	The Event Status Index identifies a unique event monitored by the ASF-sensor. It is zero-based, sequential, continuous, and ranging form 0-37h.
Event Status	The Event Status indicates the event state of the ASF-sensor device associated with the message's Event Status Index.
Event Severity	The Event Severity gives the management station an indication of the severity of the event in the PET frame. Typical values are Monitor (0x01), Non Critical (0x08), or Critical Condition (0x10).

Following is the illustration of ASF SMBus command for Get Event Data.

1	7	1	1	8	1	8	1	
S	Slave Address	Wr	A	Command	A	Wr Byte Count	A	…
	ASF-sensor Address	0	0	Sensor Device 0000 0001	0	0000 0100	0	

8	1	8	1	8	1	8	1	
Wr Data 1	A	Wr Data 2	A	Wr Data 3	A	Wr Data 4	A	…
Sub Command Get Event Data 0001 0001	0	Version Number 0001 0000	0	Event Status Index 00ii iiii	0	Reserved 0000 0000	0	

1	7	1	1	8	1	
Sr	Slave Address	R	A	Rd Byte Count	A	…
	ASF-sensor Address	1	0	0000 1010 to 0000 1111	0	

1	8	1	8	1	8	1	
A	Rd Data 1	A	Rd Data 2	A	Rd Data 3	A	…
0	Status	0	Event Sensor Type	0	Event Type	0	

8	1	8	1	8	1	8	1	
Rd Data 4	A	Rd Data 5	A	Rd Data 6	A	Rd Data 7	A	…
Event Offset	0	Event Source Type	0	Event Severity	0	Sensor Device	0	

8	1	8	1	8	1	
Rd Data 8	A	Rd Data 9	A	Rd Data 10	A	…
Sensor Number	0	Entity	0	Entity Instance	0	

	8	1	1
…	PEC	A	P
From zero to five bytes of Event Data	[data dependent]	1	

6.6 Analog Inputs

The maximum input voltage of the analog pin is 4.096V because the 8-bit ADC has a 16mv LSB. Actually, the application of the PC monitoring would most often be connected to power supply. The CPU V-core voltage, +3.3V and battery voltage can directly connect to these analog inputs. The –5V, –12V and +12V inputs should be reduced a factor with external resistors to meet the input range. As Figure 7 shows.

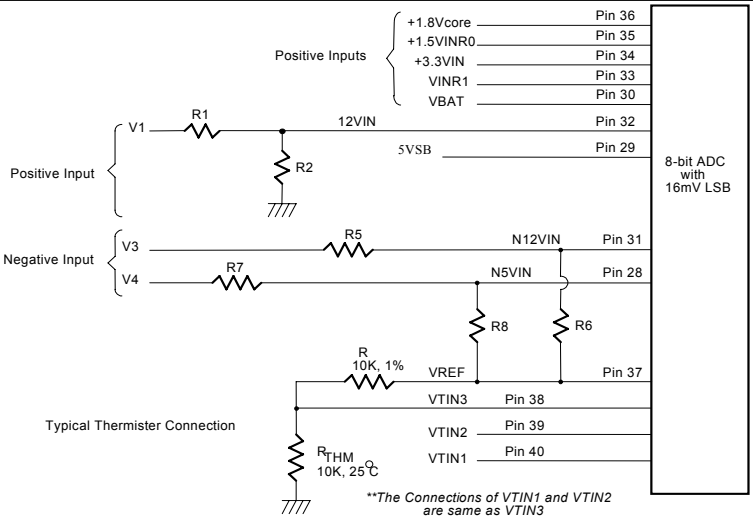


Figure 7.