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W83792AD/D
W83792AG/G

Winbond
H/W Monitoring IC
(CSB Version)

Date :2006 Apr. Revision: 0.9

W83792AD/D
Data Sheet Revision History

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
1		Aug-27-2003		N/A	Move Low Bit I/II to AEh and AFh
2		Aug-27-2003		N/A	Add Description of ASF Severity/Offset
3		Sep-12-2003	0.6	N/A	Update register
4	70-72	Sep-16-2003	0.6.1.	N/A	Update Application circuit
5	12-34	Nov-06-2003	0.7	N/A	Add the part of “Function Description”
6		Jan-05-2004	0.82	N/A	Combining with W83792D and W83792AD in one datasheet. Move Low Bit I/II to 3Eh and 3Fh
7		Dec-13-2004	0.83	N/A	Add description on Voltage translation.
8	11 20 39 45 48	Mar-01-2005	0.85	N/A	The Deletion of Vin4 4.096V(Voltage mode) Modify Monitor negative voltage Update voltage convert formula Modify Device Version ID 13h for C version. Modify Temperature Offset Attribute R/W
9	5-6 11 20 45 47 39 88 90-97	Nov-10-2005	0.86	N/A	Modify the W83792AD/D pin outputs define for BSA version. PIN25 and PIN26 pins are High active for Thermtrip. PIN35 is VCOREB/VIN4. Modify the PIN35 descriptions. VCOREB input detect range is 0~2.048V and Vin4 is 0~4.096V. Added the PIN37 VREF reference voltage is equal to 3.6V. Modify the monitor the negative voltage for VREF equals 3.6V. Modify Device Version ID 11h for B version CR [49h] and Pin control register. CR [4Bh] bit7 Modify Diode Selection Register CR[59h] power on value. Modify Low Bit I/II to AEh and AFh. The voltage Calculation with Low Bit I/II to AEh and AFh Modify top marking for the BSA version. Updated application circuits.

W83792AD/D Data Sheet Revision History, continued

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
10	5~6 10 10 40 35 83-90	Apr-26-2006	0.9	N/A	Modify the W83792AD/D pin outputs define for CSB version. PIN25 and PIN26 pins are low active for Thermtrip. PIN35 is VCOREB. Modify the PIN35 descriptions. VCOREB input detect range is 0~2.048V and Vin4 is deleted. Added the PIN37 VREF description. Reference voltage is equal to 2.048V. Modify Device Version ID 13h for C version. Modify Low Bit I/II to 3Eh and 3Fh. Updated application circuits. Add Pb-free package

winbond

Table of Contents-

1. GENERAL DESCRIPTION

W83792AD/AG and W8392D/G are two parts support single and dual CPU application, the former is for single CPU application which provides 1 set thermal trip and 1 set of VID controlling; the latter is for dual CPU application which provides dual CPU VID controlling and 2 sets of thermal trip. Other functions are all the same without difference except thermal trip and VID controlling numbers.

W83792D/G is an evolving version of the W83791D --- Winbond's most popular hardware status monitoring IC. Besides the conventional functions of W83791D, W83792D/G uniquely provides several innovative features such as support dual CPU VID controlling, VRM9.0 and VRD10.0 specifications supported, ASF 2.0 specification compliant, SMBus 2.0 ARP command compatible, 2 sets of Thermal trip, 12 VID control, 6 sets of Smart fan ™, VID table selection trapping. Conventionally, W83792D/G can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system, such as server, workstation…etc, working very stably and efficiently.

A 10-bit analog-to-digital converter (ADC) was built inside W83792D/G. W83792D/G can simultaneously monitor 9 analog voltage inputs (including power VDD/5VSB monitoring), 6 fan tachometer inputs, 3 remote temperatures, and Watch Dog Timer function. The sense of remote temperature can be performed by thermistors, or directly from Intel™ CPU with thermal diode output. W83792D/G provides 6 PWM (pulse width modulation)/DC fan output modes for smart fan control - " Thermal Cruise™ " mode and " Smart Fan™ II " mode. Under " Thermal Cruise™ " mode, temperatures of CPU and the system can be maintained within specific programmable ranges under the hardware control. As Smart Fan ™ II, which provides 4 sets of temperatures point each could control fan's duty cycle, depends on this construction, fan could be operated at the lowest possible speed so that the acoustic noise could be avoided. As for warning mechanism, W83792D/G provides SMI#, OVT#, IRQ signals for system protection events.

Additionally, 12 VID inputs are provided to read 2 sets of VID for CPU (i.e. Pentium™ III/4). These VID inputs provide the information of Vcore voltage that CPU expects. W83792D/G also has 2 specific pins to provide selectable address setting for application of multiple devices (up to 4 devices) wired through I^2C interface.

W83792D/G can uniquely serve as an ASF sensor to respond to ASF master's request for the implementation of network management in OS-absent status. Through W83792D/G's compliance with ASF2.0 sensor specification, network server is able to monitor the environmental status of each client in OS-absent state by PET (Platform Event Trip) frame values returned from W83792D/G, such as temperatures, voltages, fan speed, thermal trip, and case open. Moreover, W83792D/G supports SMBus 2.0 ARP command to solve the problem of address conflicts by dynamically assigning a new unique address for W83792D/G ASF Function after W83792D/G's UDID is sent.

Through the application software or BIOS, the users can read all the monitored parameters of the system from time to time. A pop-up warning can also be activated when the monitored item is out of the proper/preset range. The application software could be Winbond's Hardware Doctor™, Intel™ LDCM (LanDesk Client Management), or other management application software. Besides, the users can set up the upper and lower limits (alarm thresholds) of these monitored parameters and activate one programmable and maskable interrupts.

2. FEATURES

2.1 VCORE Monitoring Items

- Support dual CPU VID reading.
- VRM9.0 / VRD10.0 compliant to monitor dual CPU voltage.
- 2 sets of thermal trip latch mechanism to protect CPU from over temperature.

2.2 Monitoring Items

- Monitoring 9 voltage inputs.
- 6 DC / PWM Fan outputs for fan speed control and 6 Fan speed inputs for monitoring --- Total up to 6 sets of fan speed monitoring and controlling
- 3 temperature inputs from remote thermistor and PentiumTM II/III/4 (Deschutes) thermal diode output
- 6 sets Smart FanTM could control the most fitting speed automatically by temperature.
- Case open detection input
- 2 sets of CPU thermal management:2 Thermal Trip signals latch up and generate VRM_EN signal to PWM for removing CPU power.
- Programmable hysteresis and setting points (alarm thresholds) for all monitored items

2.3 Address Resolution Protocol (ARP) and Alert-Standard Format (ASF 2.0)

- Support System Management Bus (SMBus) version 2.0 specification
- Comply with hardware sensor slave ARP (Address Resolution Protocol)
- Response ASF 2.0 command --- Get Event Data, Get Event Status, Device Type Poll
- Comply with ASF 2.0 sensors (Power on/off remote control, Monitoring fan speed, voltage, temperature, thermal trip and case open)
- Support Remote Control subset: Remote Power-on/ Power-off/ Reset.

2.4 Actions Enabling

- Issue SMI#, OVT#, IRQ signals to activate system protection
- Warning signal pop-up in application.

2.5 General

- I2C serial bus interface
- Support 2 sets of 6bit VID monitoring for dual processors application
- Watch Dog Timer function with pin: RESET#, SYSRST_IN.
- 16 GPIOs
- 2 pins (A0, A1) to provide selectable address setting for application of multiple devices (up to 4 devices) wired through I2C interface

- Winbond hardware monitoring application software (Hardware DoctorTM) support, for both Windows 95/98/2000/XP and Windows NT 4.0/5.0/2000
- 5V VSB operation

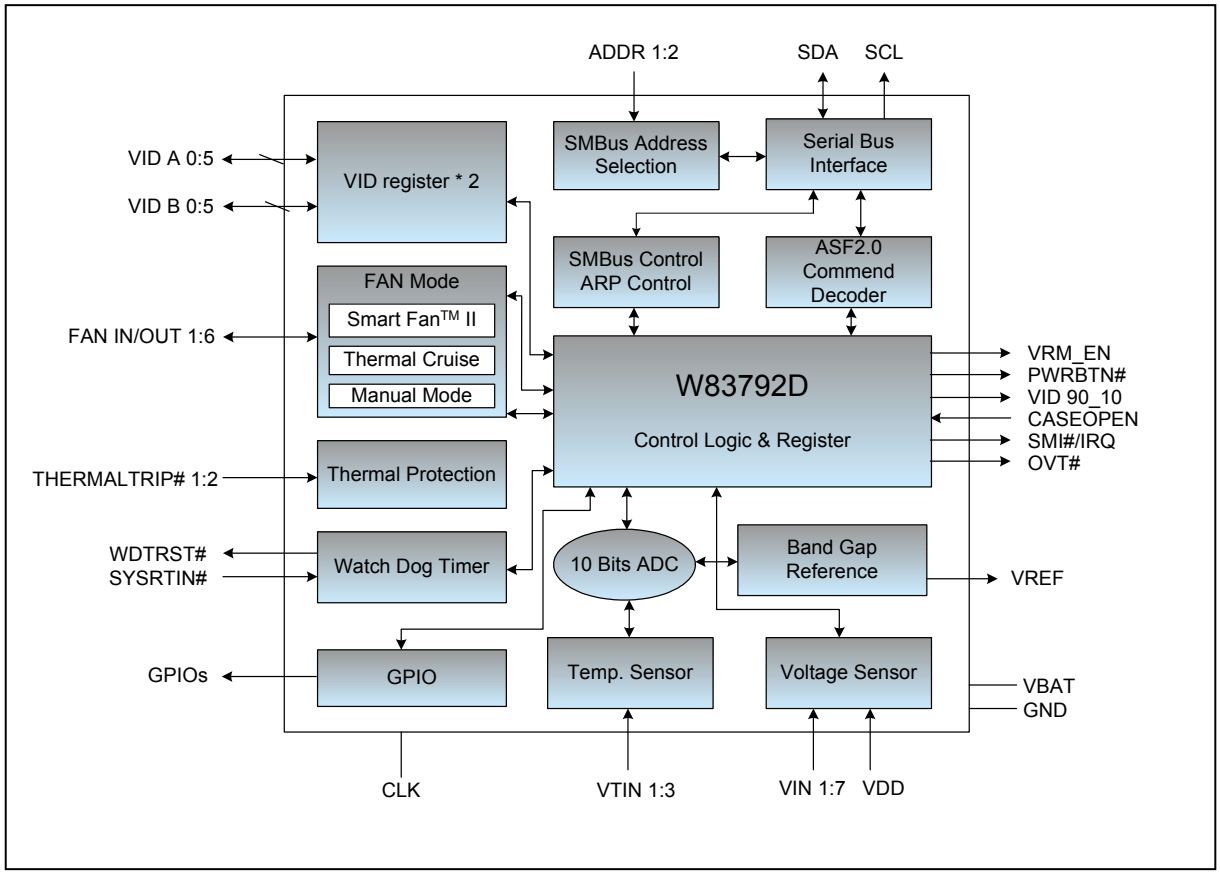
2.6 Package

- 48-pin LQFP

3. KEY SPECIFICAITON

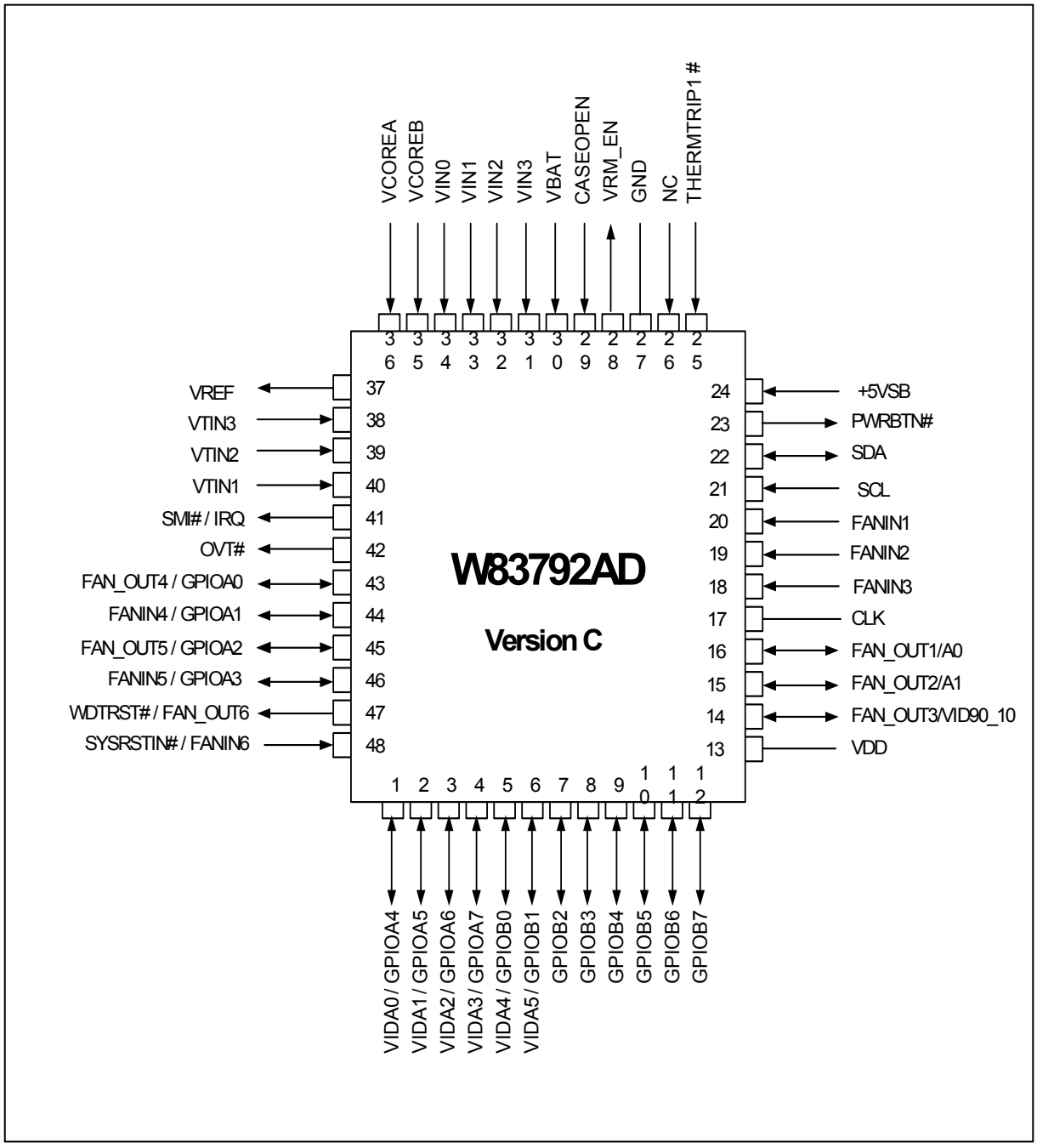
• Voltage monitoring accuracy	±1% (Max)
• Intel VRM 9.x/VRD10.0 Voltage monitoring accuracy	±1% (Max)
• Temperature Sensor Accuracy	
Remote Diode Sensor Accuracy	± 3°C(Max)
Resolution	0.5 ℃
• Supply Voltage	5V
• Operating Supply Current	5 mA typ.
• ADC Resolution	10 Bits

4. BLOCK DIAGRAM

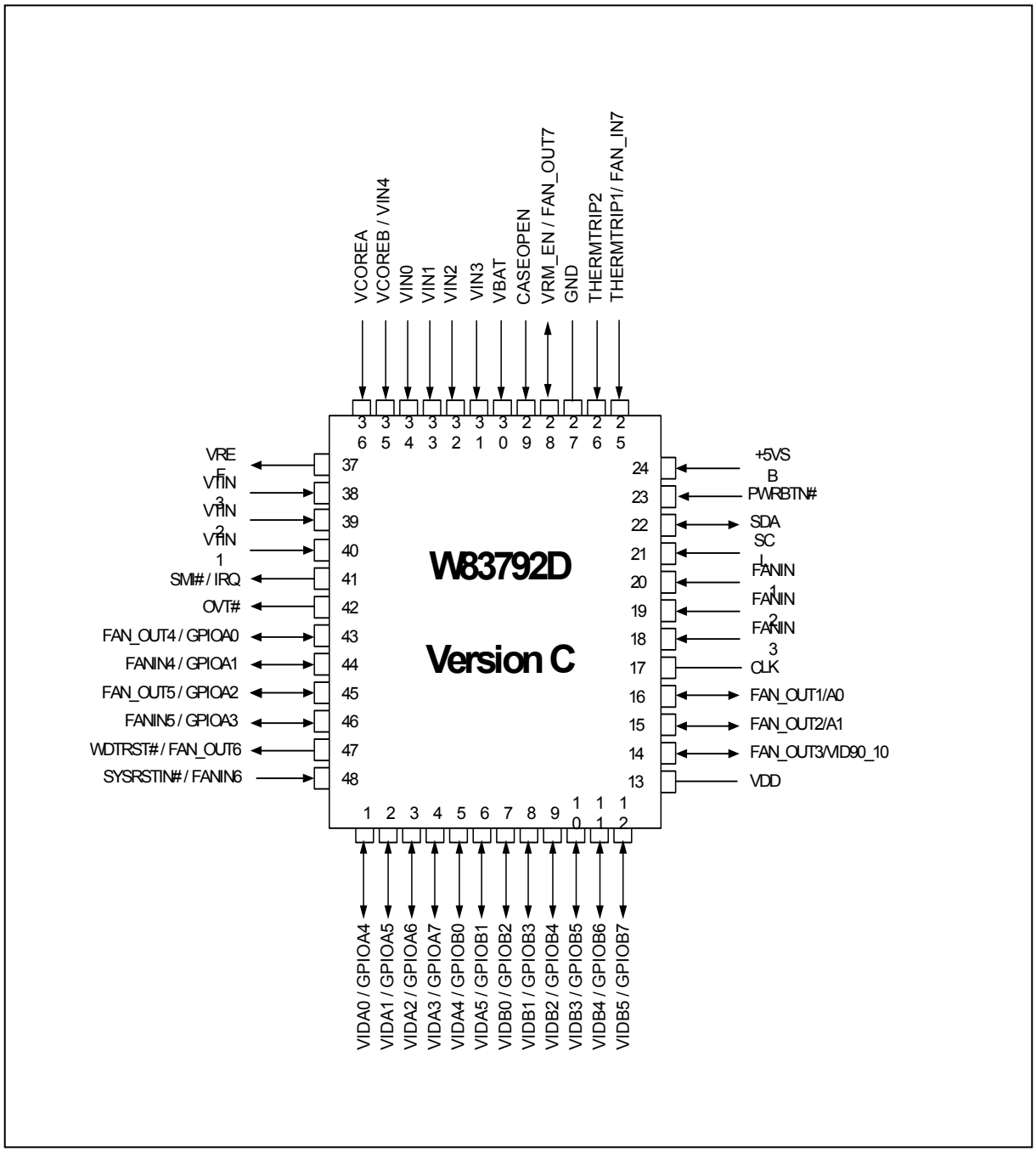


5. PIN CONFIGURATION

5.1 W83792AD/AG



5.2 W83792D/G


W83792D
Version C
VCOREA
VCOREB / VIN4
VIN0
VIN1
VIN2
VIN3
VBAT
CASEOPEN
VRM_EN / FAN_OUT7
GND
THERMTRIP2
THERMTRIP1/ FAN_IN7
VREF
VTIN3
VTIN2
VTIN1
SMI# / IRQ
OVT#
FAN_OUT4 / GPIOA0
FANIN4 / GPIOA1
FAN_OUT5 / GPIOA2
FANIN5 / GPIOA3
WDTRST# / FAN_OUT6
SYSRSTIN# / FANIN6
+5VSB
PWRBTN#
SDA
SCL
FANIN1
FANIN2
FANIN3
CLK
FAN_OUT1/A0
FAN_OUT2/A1
FAN_OUT3/VID90_10
VDD
VIDA0 / GPIOA4
VIDA1 / GPIOA5
VIDA2 / GPIOA6
VIDA3 / GPIOA7
VIDA4 / GPIOB0
VIDA5 / GPIOB1
VIDB0 / GPIOB2
VIDB1 / GPIOB3
VIDB2 / GPIOB4
VIDB3 / GPIOB5
VIDB4 / GPIOB6
VIDB5 / GPIOB7

6. PIN DESCRIPTION

6.1 Pin Type Description

I/O_{12t}	TTL level bi-directional pin with 12 mA source-sink capability
I/O_{12ts}	TTL level and schmitt trigger with 12 mA source-sink capability
I/O_{8ts}	TTL level and schmitt trigger with 8 mA source-sink capability
I/O_{6ts}	TTL level and schmitt trigger with 6 mA source-sink capability
I/OD_{12ts}	TTL level and schmitt trigger open drain output with 12 mA sink capability
OUT_{12}	Output pin with 12 mA source-sink capability
OD_{12}	Open-drain output pin with 12 mA sink capability
AOUT	Output pin (Analog)
IN_t	TTL level input pin
IN_{ts}	TTL level input pin and schmitt trigger
AIN	Input pin(Analog)

6.2 Pin Description List

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
VIDA0	1	5VSB	IN_{ts}	Voltage Supply readouts bit 0 from CPU A.
GPIOA4			I/OD_{12ts}	After programming, this pin can be VID output or GPIO.
VIDA1	2	5VSB	IN_{ts}	Voltage Supply readouts bit 1 from CPU A.
GPIOA5			I/OD_{12ts}	After programming, this pin can be VID output or GPIO.
VIDA2	3	5VSB	IN_{ts}	Voltage Supply readouts bit 2 from CPU A.
GPIOA6			I/OD_{12ts}	After programming, this pin can be VID output or GPIO.
VIDA3	4	5VSB	IN_{ts}	Voltage Supply readouts bit 3 from CPU A.
GPIOA7			I/OD_{12ts}	After programming, this pin can be VID output or GPIO.
VIDA4	5	5VSB	IN_{ts}	Voltage Supply readouts bit 4 from CPU A.
GPIOB0			I/OD_{12ts}	After programming, this pin can be VID output or GPIO.

Pin Description List, continued

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
VIDA5	6	5VSB	IN_{ts}	Voltage Supply readouts bit 5 from CPU A. Only used in VRD10.0.
GPIOB1			I/OD-12ts	After programming, this pin can be VID output or GPIO.
VIDB0	7	5VSB	IN_{ts}	Voltage Supply readouts bit 0 from CPU B.
GPIOB2			I/OD-12ts	After programming, this pin can be VID output or GPIO.
VIDB1	8	5VSB	IN_{ts}	Voltage Supply readouts bit 1 from CPU B.
GPIOB3			I/OD-12ts	After programming, this pin can be VID output or GPIO.
VIDB2	9	5VSB	IN_{ts}	Voltage Supply readouts bit 2 from CPU B.
GPIOB4			I/OD-12ts	After programming, this pin can be VID output or GPIO.
VIDB3	10	5VSB	IN_{ts}	Voltage Supply readouts bit 3 from CPU B.
GPIOB5			I/OD-12ts	After programming, this pin can be VID output or GPIO.
VIDB4	11	5VSB	IN_{ts}	Voltage Supply readouts bit 4 from CPU B.
GPIOB6			I/OD-12ts	After programming, this pin can be VID output or GPIO.
VIDB5	12	5VSB	IN_{ts}	Voltage Supply readouts bit 5 from CPU B. Only used in VRD10.0.
GPIOB7			I/OD-12ts	After programming, this pin can be VID output or GPIO.
VDD	13	-	POWER	+5V VDD power. Bypass with the parallel combination of 10μF (electrolytic or tantalum) and 0.1μF (ceramic) bypass capacitors.
FAN_OUT3	14	5VSB	OUT_{12}	Fan speed control PWM/DC output. When the power of VDD is 0v, this pin will drive logic 0. The power of this pin is supplied by VSB 5V.
VID9_10			IN_{ts}	At 5VSB power on, this pin is used to select Internal VRM 9 or 10 table. Detect 1, Select VRM9, Detect 0, selects VRM10.

Pin Description List, continued

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
FAN_OUT2	15	5VSB	OUT_{12}	Fan speed control PWM/DC output. When the power of VDD is 0v, this pin will drive logic 0. The power of this pin is supplied by VSB 5V.
A1			IN_{ts}	I^2C device address bit 1 trapping during 5VSB power on.
FAN_OUT1	16	5VSB	I/O_{12t}	Fan speed control PWM/DC output. When the power of VDD is 0v, this pin will drive logic 0. The power of this pin is supplied by VSB 5V.
A0			IN_{ts}	I^2C device address bit 0 trapping during 5VSB power on.
CLK	17	VDD	IN_{ts}	14.318MHz System clock while VCC5V powered up.
FANIN3	18	VDD	IN_{ts}	0V to +5V amplitude fan tachometer input
FANIN2	19	VDD	IN_{ts}	0V to +5V amplitude fan tachometer input
FANIN1	20	VDD	IN_{ts}	0V to +5V amplitude fan tachometer input
SCL	21	5VSB	IN_{ts}	Serial Bus Clock.
SDA	22	5VSB	I/OD_{12ts}	Serial Bus bi-directional data.
PWRBTN#	23	5VSB	OD_{12}	Power Button output for enable/disable power supply.
+5VSB	24	-	POWER	This pin is power for W83792D/G. Bypass with the parallel combination of 10μF (electrolytic or tantalum) and 0.1μF (ceramic) bypass capacitors.
THERMTRIP1# FANIN7	25	5VSB	IN_{ts}	Thermal Trip signal from CPU A. Low Active. 0~+5V FANIN 7 tachometer.
THERMTRIP2#	26	5VSB	IN_{ts}	Thermal Trip signal from CPU B. Low Active.

Pin Description List, continued

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
GND	27	-	POWER	System Ground.
VRM_EN FAN_OUT7	28	5VSB	OD_{12} OUT_{12}	Any assertion of thermal trip after VDD power good will disable Voltage Regulator Module. Fan speed control PWM output. By default it's high. The power of this pin is supplied by VSB 5V.
CASEOPEN	29	VBAT	IN_{ts}	CASE OPEN detection. An active high input from an external device when case is Intruded. This signal can be latched in external circuit which power is supplied by VBAT, even if W83792D is power off.
VBAT	30	-	POWER	VBAT supplies power for CASEOPEN, THERMALTRIP. Besides, it is also a voltage monitor channel.
VIN3- VIN0	31 - 34		AIN	0V to 4.096V Analog Voltage Monitor Inputs.
VCOREB	35		AIN	CPU B Core Voltage Input. Detect range is 0~2.048V.
VCOREA	36		AIN	CPU A Core Voltage Input. Detect range is 0~2.048V.
VREF	37		AOUT	Reference voltage and is equal to 2.048V
VTIN3	38		AIN	Thermistor 3 terminal input.(Default). Pentium™ 4 diode 3 input. This multi-functional pin is programmable.
VTIN2	39		AIN	Thermistor 2 terminal input. (Default). Pentium™ 4 diode 2 inputs. This multi-functional pin is programmable.
VTIN1	40		AIN	Thermistor 1 terminal input. (Default). Pentium™ 4 diode 1 inputs. This multi-functional pin is programmable.

Pin Description List, continued

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
IRQ /	41	VDD	OUT_{12}	Interrupt request.
SMI#			OD_{12}	System Management Interrupt (open drain).
OVT#	42	VDD	OD_{12}	Over temperature Shutdown Output for temperature sensor 1-3.
FAN_OUT4	43	5VSB	OUT_{12}	Fan speed control PWM/DC output. When the power of VDD is 0v, this pin will drive logic 0. The power of this pin is supplied by VSB 5V.
GPIOA0			I/O_{12ts}	After programming, this pin can be GPIO.
FANIN4	44	5VSB	IN_{ts}	0V to +5V amplitude fan tachometer input
GPIOA1			I/O_{12ts}	After programming, this pin can be GPIO.
FAN_OUT5	45	5VSB	OUT_{12}	Fan speed control PWM output. When the power of VDD is 0v, this pin will drive logic 0. The power of this pin is supplied by VSB 5V.
GPIOA2			I/O_{12ts}	After programming, this pin can be GPIO.
FANIN5	46	5VSB	IN_{ts}	0V to +5V amplitude fan tachometer input
GPIOA3			I/O_{12ts}	After programming, this pin can be GPIO.
FAN_OUT6	47	5VSB	OUT_{12}	Fan speed control PWM output. By default it's high. The power of this pin is supplied by VSB 5V.
RESET#			OD_{12}	Low active System RESET. If triggered, this pin will send out 100ms low pulse for system reset.
FANIN6	48	5VSB	IN_{ts}	0V to +5V amplitude fan tachometer input
SYSRSTIN#			IN_{ts}	System reset input, used to control WDT.

7. FUNCTION DECRIPPTION

7.1 General Description

The W83792D/G provides 9 analog voltage inputs, 7 fan speed inputs and output controls which support both of PWM (Pulse Width Modulation) control and DC (Direct Current) fan control, all of them are implemented with Smart FAN™ I and Smart FAN™ II. 3 sets of thermal inputs for remote thermistor or Pentium™ 4 thermal diode outputs, and case open detection also supported in W83792D/G. Further more, W83792D/G provides several innovative and practical functions to make the whole system manage more efficiently and compliant with future trend of network management, such as ASF2.0 sensor compliant, which could remote Power on/off control the system, report the status of thermal trip, fan, and temperature limitation. Also, it is SMBus 2.0 ARP command compatible. VID table could be selected by hardware trapping for VRM9.0 and VRD 10 specifications. 2 sets of 6 bits of VID input/output control for dual processors and 2 sets of thermal Trip input for disable VRM module, and for the more, once the monitoring function of W83792D/G is enabled, the watch dog will monitor every function and store the values to registers for comparison with preset ranges. If the monitoring value exceeds the limit value, the interrupt status will be set to 1 and W83792D/G will issue interrupt signals such as SMI# and IRQ if they are not masked off. W83792D/G also provides software and hardware Watch Dog Timer to avoid system hang on.

7.2 Access Interface

The W83792D/G provides I2C Serial Bus for microprocessor to read/write internal registers. In the W83792D/G, there are three serial bus addresses. Through the fi

The first serial bus address of W83792D/G has 2 hardware setting bits set by Pin15-16. *The address is 01011[pin15][pin16]X. Hence, the content of CR [48h] would be 00101110 if pin15=1 and pin16=0. The read/write of the CPUT1/CPUT2 temperature sensor registers can be implemented through the second address (defined at CR [4Ah] bit2-0 10011[IA1][IA0]X) and the third address (defined at CR[4Ah] bit6-4 10010[IA1][IA0]X).*rst address defined at CR[48h], all the registers can be read and written.

7.3 The first serial bus access timing

(a) Serial bus writes to internal address register followed by the data byte

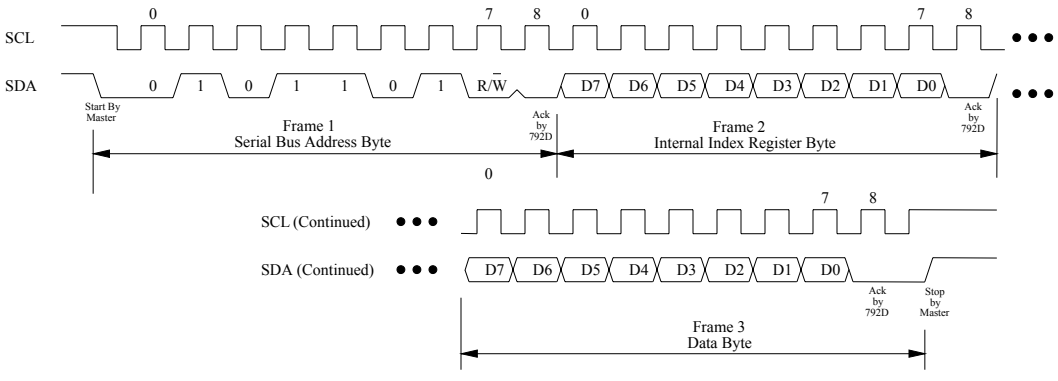


Figure 1. Serial Bus Write to Internal Address Register followed by the Data Byte

(b) Serial bus read from a register

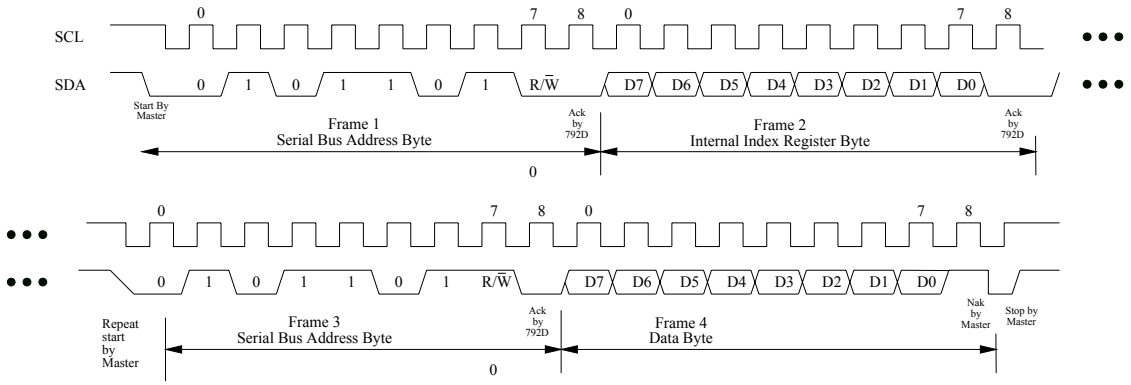


Figure 2. Serial Bus Read from Internal Address Register

7.4 Address Resolution Protocol (ARP) Introduction

As the W8792D/G is a slave device existing on the System Management Bus, it must have a unique address to prevent itself from conflicting with the other devices existing on the same bus. In order to solve the problem of address conflicts, SMBus version 2.0 introduces the concept of dynamically assigned address called Address Resolution Protocol (ARP). By such mechanism, each device existing on the SMBus will be given with an unique slave address if it is a ARP-capable device. Thus, to meet the new spec, W83792D/G uniquely provides ARP compliant function to acquire an unique slave address.

The typical process of ARP contains several steps, including *Prepare to ARP*, *Reset Device*, *Get UDID*, *Assign Address*, and so on. Whenever the slave device accepts the command of ARP master, it must reply an Acknowledgement to the ARP master, thus the ARP master is able to carry on the next step. In order to provide a mechanism to isolate device for the purpose of address assignment, each device must implement a *unique device identifier* (UDID). The UDID is a 128-bit number comprised of several field, including Device Capabilities, Version Revision, Vendor ID, Device ID, Interface, Subsystem Vendor ID, Subsystem Device ID, and Vendor Specific ID. After the UDID of the device is sent to the ARP master, the ARP master will then assign an address not in the Used Address Pool to the device.

Generally speaking, there are eleven possible commands to read /write the data of SMBus device, and a slave device may use any or all of the eleven protocols to communicate. These protocols are Quick Command, Send Byte, Receive Byte, Write Byte, Write Word, Read Byte, Read word, Process Call, Block Write, and Block Write-Block Read Process Call. W83792D/G itself supports the Block Write-Block Read Process with PEC to communicate with ARP Master. Following is a description of the SMBus packet protocol diagrams element key. Not all protocol elements will be present in every command, that is, not all packets are required to include the *Packet Error Code*.

1-bit	7	1	1	8	1	8	1	1-bit
S	Slave Address	Wr	A	Command	A	PEC	A	P

S		Start Condition
Sr		Repeated Start Condition
Rd		Read (bit value of 1)
Wr		Write (bit value of 0)
A		Acknowledge (this bit position may be '0' for an ACK or '1' for a NACK)
P		Stop Condition
PEC		Packet Error Code
		Master-to-Slave
		Slave-to-Master

Relative command list:

SLAVE ADDRESS	COMMAND	DESCRIPTION
C2h	01h	Prepare to ARP
C2h	02h	Reset device (general)
C2h	03h	Get UDID (general)
C2h	04h	Assign address
C2h	Slave_Addr | 1	Direct Get UDID
C2h	Slave_Addr | 0	Direct Reset
C2h	05h-1Fh	Reserved.

Following is an example of the Block Write-Block Read Process Call. The Block Write-Block Read Process Call is a two-part message. It begins with a salve address and a write condition. After the command code the host issues a write count M that describes how many more bytes will be written in the first part of the message. The second part of the message is a block of read data beginning with a repeat start condition followed by the salve address and a Read Bit. The next read byte count N indicates how many more data will be read in the second part of the message. Note that the combined data payload must not exceed 32bytes. Besides, W83792D/G also provides packet error code (PEC) to ensure the accuracy during data transmission.

1	7	1	1	8	1	8	1	8	1	
S	Slave Address	Wr	A	Command Code	A	Byte Count=M	A	Data Byte 1	A	…

8	1	…	8	1	
Data Byte 2	A	…	Data Byte M	A	…

1	7	1	1	8	1	8	1	1
Sr	Slave Address	Rd	A	Byte Count=N	A	Data Byte 1	A	…

8	1	…	8	1	8	1	1
Data Byte 2	A	…	Data Byte N	A	PEC	A	P

7.5 ASF (Alert Standard Format) Introduction

In order to implement network management in OS-absent, W83792D/G provides ASF Response Registers to meet ASF sensor spec. As a result, the network server is able to monitor several environmental status of the client in OS-absent by PET frame values returned from W83792D/G, including temperature, voltage, fan speed, and case open. In below is the ASF diagram:

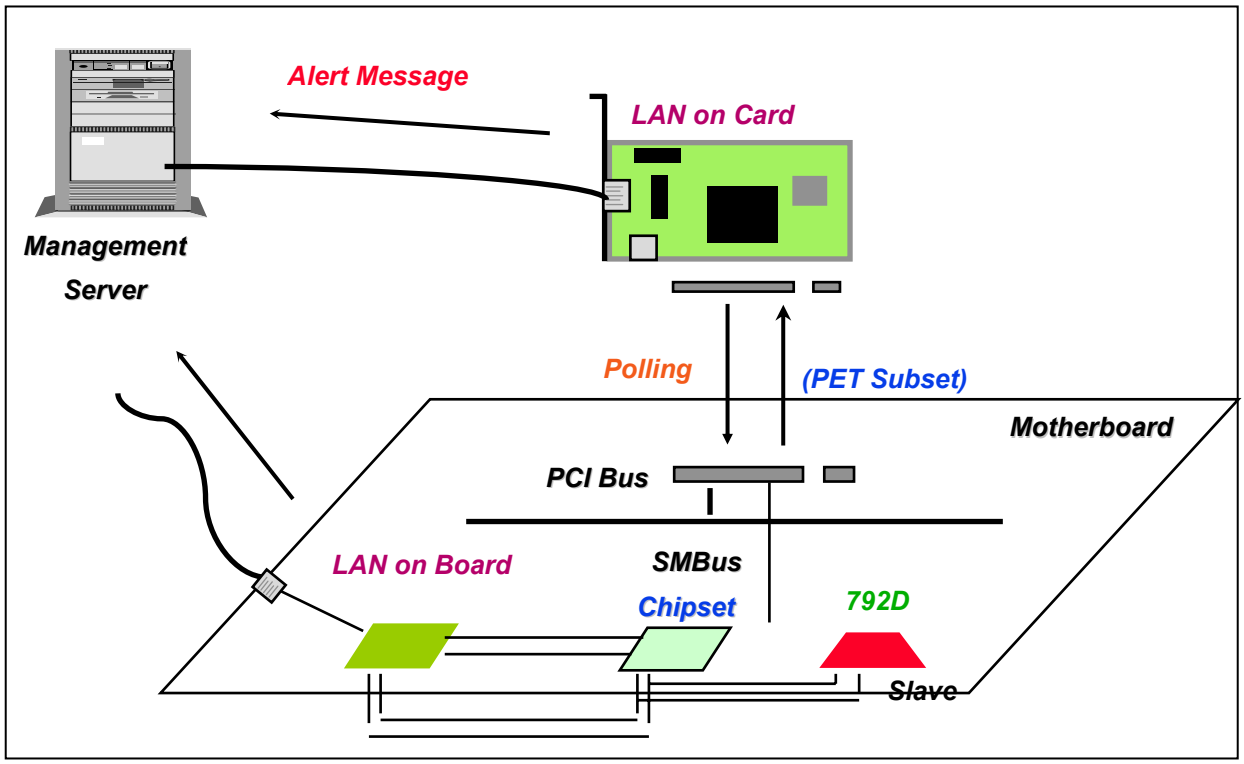


Figure 3. ASF Block Diagram

7.5.1 Platform Event Trap (PET)

PET is the ASF transmit protocol used to provide common fields for trap regardless of trap source. The variable bindings fields in a PET frame contain the system and sensor information for an event, such as event sensor type, event type, event offset, event source type, sensor device, sensor number, entity ID, entity instance, event status index, event status, and event severity. Each field has its definition and is described in the following table.

PET VARIABLE BINDING FIELD	DESCRIPTION
Event Sensor Type	The Event Sensor Type field indicates what types of events the sensor is monitoring. E.g. temperature, voltage, fan, etc.
Event Type	The Event Type indicates what type of transition/state change triggered the trap.
Event Offset	The Event Offset indicates which particular event occurred for a given Even Type.
Event source Type	The Event Source Type describes the originator of the event. It is ASF2.0(68h) for all PET frames defined by this specification.
Sensor Device	The Sensor Device is the SMBus address of the sensor that caused the event for the PET frame.
Sensor Number	The Sensor Number is used to identify a given instance of a sensor relative to the Sensor Device.
Entity ID	The Entity ID indicates the platform entity the event is associated with. E.g. processor, system board, etc.
Entity Instance	The Entity Instance indicates which instance of the Entity the event is for. E.g. processor 1 or processor 2.
Event Status Index	The Event Status Index identifies a unique event monitored by the ASF-sensor. It is zero-based, sequential, continuous, and ranging form 0-37h.
Event Status	The Event Status indicates the event state of the ASF-sensor device associated with the message's Event Status Index.
Event Severity	The Event Severity gives the management station an indication of the severity of the event in the PET frame. Typical values are Monitor (0x01), Non Critical (0x08), or Critical Condition (0x10).

Following is the illustration of ASF SMBus command for Get Event Data.

1	7	1	1	8	1	8	1	
S	Slave Address	Wr	A	Command	A	Wr Byte Count	A	…
	ASF-sensor Address	0	0	Sensor Device 0000 0001	0	0000 0100	0	

8	1	8	1	8	1	8	1	
Wr Data 1	A	Wr Data 2	A	Wr Data 3	A	Wr Data 4	A	…
Sub Command Get Event Data 0001 0001	0	Version Number 0001 0000	0	Event Status Index 00ii iiii	0	Reserved 0000 0000	0	

1	7	1	1	8	1	
Sr	Slave Address	R	A	Rd Byte Count	A	…
	ASF-sensor Address	1	0	0000 1010 to0000 1111	0	

1	8	1	8	1	8	1	
A	Rd Data 1	A	Rd Data 2	A	Rd Data 3	A	…
0	Status	0	Event Sensor Type	0	Event Type	0	

8	1	8	1	8	1	8	1	
Rd Data 4	A	Rd Data 5	A	Rd Data 6	A	Rd Data 7	A	…
Event Offset	0	Event Source Type	0	Event Severity	0	Sensor Device	0	

8	1	8	1	8	1	
Rd Data 8	A	Rd Data 9	A	Rd Data 10	A	…
Sensor Number	0	Entity	0	Entity Instance	0	

	8	1	1
…	PEC	A	P
From zero to five bytes of Event Data	[data dependent]	1	

7.6 Analog Inputs

The maximum input voltage of the analog pin is *4.096V* because the 10-bit ADC has a *4mv LSB.* Actually, the application of the PC monitoring would most often be connected to power supply. The CPU V-core voltage, +3.3V and battery voltage can *directly connect* to these analog inputs. The –5V, –12V and +12V inputs should be reduced a factor with external resistors to meet the input range. As Figure 4 shows.

*PS : VCORE channel resolution = 2mv VIN0-4 channel resolution = 4mv

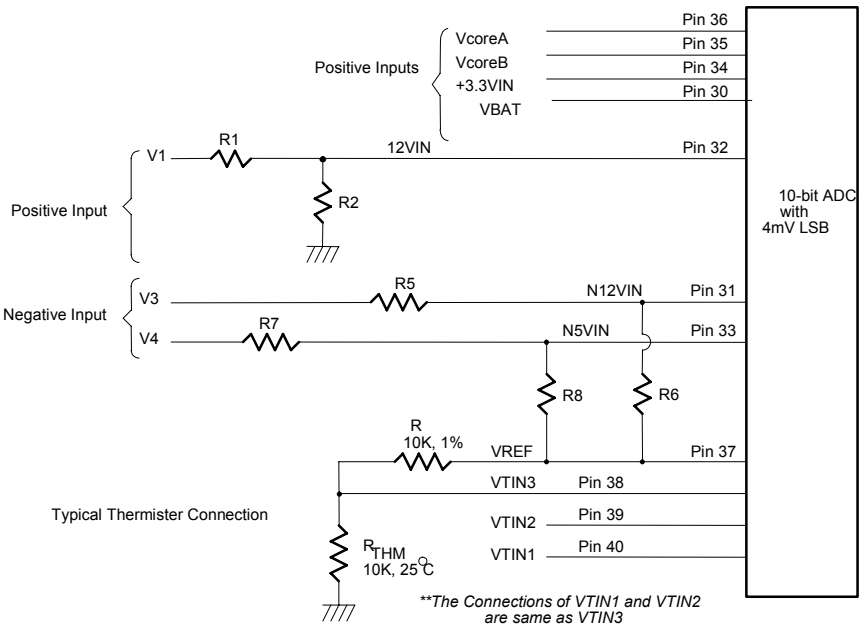


Figure 4.

7.6.1 Monitor over 4.096V voltage:

The input voltage +12VIN can be expressed as the following equation.

$$12VIN = V_1 \times \frac{R_2}{R_1 + R_2}$$

The value of R1 and R2 can be selected to 28K Ohms and 10K Ohms, respectively, when the input voltage V1 is 12V. The node voltage of +12VIN should be subject to under 4.096V for the maximum input range of the 8-bit ADC. The pin 13 and pin 29 are discretely connected to the power supply +5V and 5VSB . There are two functions in these pins with 5V. The first function is to supply internal analog power in the W83792D and the second one is that these voltages are all connected to internal serial resistors to monitor the +5V and 5VSB voltage.

7.6.2 Monitor negative voltage:

The negative voltage should be connected to two series resistors and a positive voltage VREF (equal to 2.048V). In the Figure 11, the voltage *V3 and V4* are two negative voltages and are -12V and -5V respectively. The voltage V3 is connected to two serial resistors as well as another positive terminal VREF. Therefore, the voltage node N12VIN would be a positive voltage if the scale of the two serial resistors are carefully selected. It is recommended from Winbond that the scale of the two serial resistors are R5=232K ohms and R6=10K ohm. The input voltage of node -12VIN can be calculated by the following equation.

$$N12VIN = (VREF + |V_5|) \times (\frac{232K\Omega}{232K\Omega + 10K\Omega}) + V_5$$

where VREF is equal to 2.048V.

If the V_5 is equal to -12V then the voltage is equal to 1.467V and the converted hexdecimal data is set to 60h by the 8-bit ADC with 8mV-LSB.This monitored value should be converted to the real negative voltage and the express equation is shown as follows.

$$V_5 = \frac{N12VIN - VREF \times \beta}{1 - \beta}$$

Where β is 232K/(232K+10K). If the N2VIN is 1.467 then the V5 is approximately equal to -12V.

The other negative voltage input V6 (approximate -5V) can also be evaluated by the similar method and the serial resistors can be R7=120K ohms and R8=10K ohms by the Winbond recommended. The expression equation of V6 With -5V voltage is shown as follows.

$$V_6 = \frac{N5VIN - VREF \times \gamma}{1 - \gamma}$$

Where the γ is set to 120K/(120K+10K). If the monitored ADC value in the N5VIN channel is 1.505, VREF=2.048V and the parameter γ is 0.923, then the negative voltage of V6 can be evaluated -5V.