Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

W83793G / W83793AG
Nuvoton H/W Monitor

DATE: DECEMBER 12, 2008

REVISION: 1.4

Table of Content-

1. GENERAL DESCRIPTION

The W83793G is an evolving version of the W83792D. Besides the conventional functions of the W83792D, the W83793G uniquely provides several innovative features. It is ASF 2.0 specification compliant, SMBus 2.0 ARP command compatible and has 8 sets of SMART FAN™. The W83793G can monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system, such as a server, or a workstation to work stably and efficiently.

A 10-bit analog-to-digital converter (ADC) is built inside the W83793G. The W83793G can simultaneously monitor 10 analog voltage inputs (including power 5VDD/5VSB/VBAT/Vtt monitoring), 12 fan tachometer inputs, 6 remote temperatures, 4 of which support Current Mode (dual current source) temperature measurement method, and the Watch Dog Timer function. The remote temperature can be sensed by thermistors, or directly from Intel® / AMD™ CPU with thermal diode output. The W83793G provides 8 PWM (pulse width modulation) / DC fan output modes for smart fan control – "Thermal Cruise™" mode and "SMART FAN™ II" mode. In "Thermal Cruise™" mode, temperatures of CPU and the system can be maintained within specific programmable ranges under the hardware control. The W83793G, as SMART FAN™ II, provides 8 temperature sets, each of which can control the fan's duty cycle. With this design, the fan can work at the lowest possible speed to avoid acoustic noise. As for the warning mechanism, the W83793G provides SMI#, OVT#, IRQ, and BEEP signals for system protection events. The W83793G also has 2 specific pins to provide selectable address settings for the applications of multiple devices (up to 4 devices) wired through the I^2C interface.

The W83793G can serve as an ASF sensor to respond to ASF master's request for the implementation of network management in OS-absent status. With the W83793G's compliance with ASF2.0 sensor specification, the network server is able to monitor the system status of each client in OS-absent state by PET (Platform Event Trap) frame values returned from the W83793G, such as temperatures, voltages, fan speed and case open. Moreover, the W83793G supports SMBus 2.0 ARP command to solve the address conflict problems by dynamically assigning a new address for ASF Function after UDID is sent.

Through the application software or BIOS, users can read all the monitored parameters of the system from time to time. A pop-up warning can also be activated when the monitored item is out of the proper/preset range. The application software could be Nuvoton's Hardware Doctor™ or other management application software. Besides, users can set the bounds (alarm thresholds) of these monitored parameters and activate corresponding maskable interrupts.

There is a feature reduced version of the W83793G available, W83793AG, which supports almost the same functions as those of W83793G, but removes 3 sets of thermal diode inputs (TD2 ~ TD4, Pin 31 ~ Pin 36), VcoreB input, and VIDB. The package of the W83793AG is the same as that of W83793G, which is 56-pin SSOP.

2. FEATURES

2.1 Monitoring Items

VOLTAGE

Monitoring 10 voltages (4 power pins – 5VSB, 5VDD, VBAT, Vtt, and 6 external pins – VcoreA, VcoreB, VSEN1~4). (W83793AG does not support Vcore B.)

TEMPERATURE

4 thermal diode (D+, D-) inputs, supporting Current Mode (dual current source) temperature measurement method. (W83793AG supports 1 thermal diode input only; TD2 ~ TD4 are removed in the W83793AG.)

2 thermistor inputs

Support Intel® PECI

FAN

8 DC/PWM fan outputs for fan speed control

8 fan speed inputs for monitoring (up to 12 by register setups)

SMART FAN™ -- controls the most fitting speed automatically by temperature.

CASEOPEN

CASEOPEN# detection input.

2.2 Address Resolution Protocol and Alert Standard Format

Support System Management Bus (SMBus) version 2.0 specification

Comply with hardware sensor slave ARP (Address Resolution Protocol)

Response ASF 2.0 command --- GetEventData, GetEventStatus, DeviceTypePoll

Comply with ASF 2.0 sensors (Monitoring fan speed, voltage, temperature, thermal trip and case open event/status)

Support Remote Control subset: Remote Power on/ Power off/ Reset.

2.3 Actions Enabling

Issue SMI#, OVT# signals to activate system protection

Issue BEEP signal to activate system speaker or buzzer

2.4 General

I^2C serial bus interface

Watch Dog Timer function with pin WDTRST# and SYSRST_IN.

2 pins (A0, A1) to provide selectable address settings for the application of multiple devices (up to 4 devices) wired together through the I^2C interface

5V operation

2.5 Package

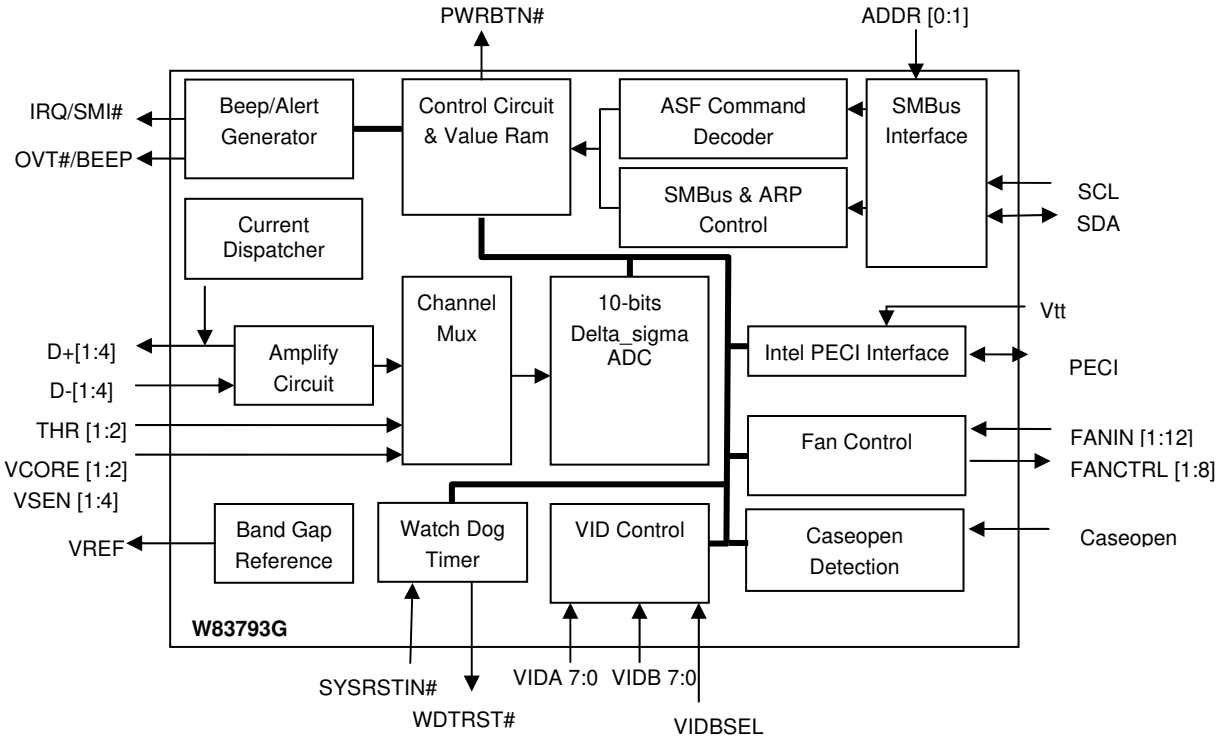
56 Pin SSOP 300mil. (For both W83793G and W83793AG)

3. KEY SPECIFICATIONS

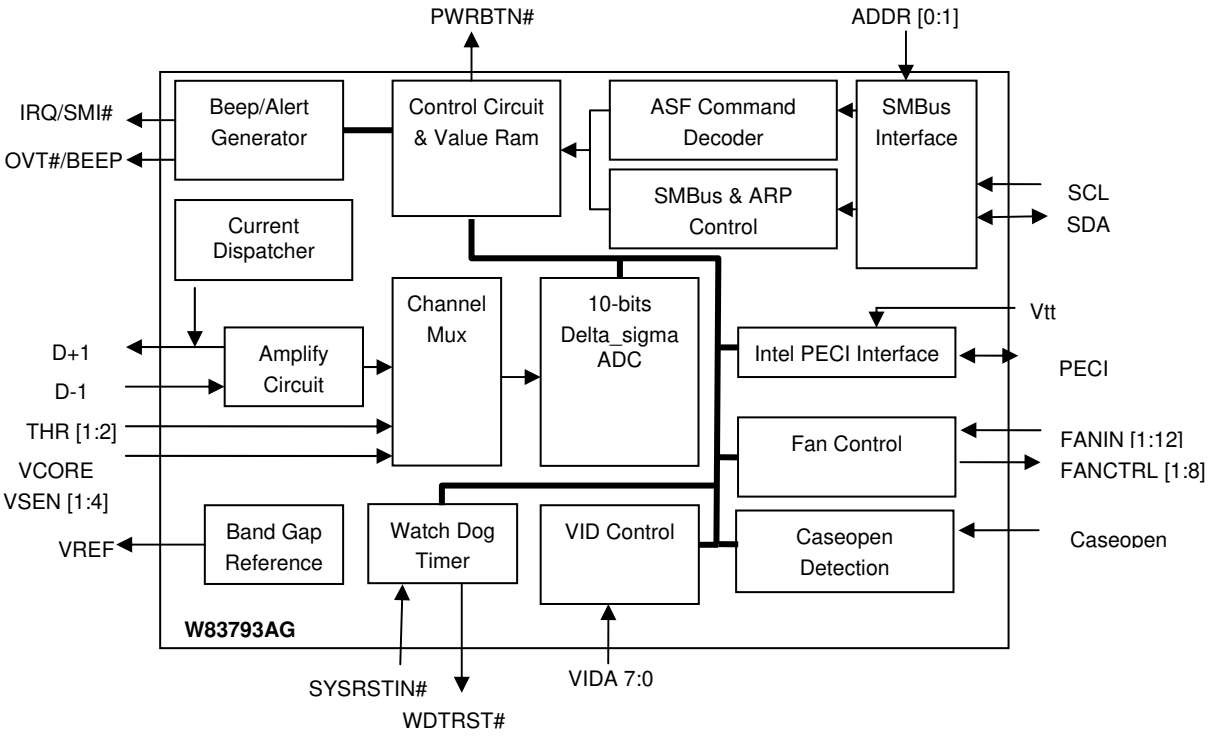
Voltage monitoring accuracy	±1%
● Temperature Sensor Accuracy	
Remote Diode Sensor Accuracy	± 1°C
Resolution	0.5 ℃
Supply Voltage (Pin 7, 5VSB)	5±0.25V
● Operating Supply Current	25 mA typ.
Current without 48MHz input at Pin 1	8 mA typ.
● ADC Resolution	10 Bits

4. BLOCK DIAGRAM

W83793G



W83793AG

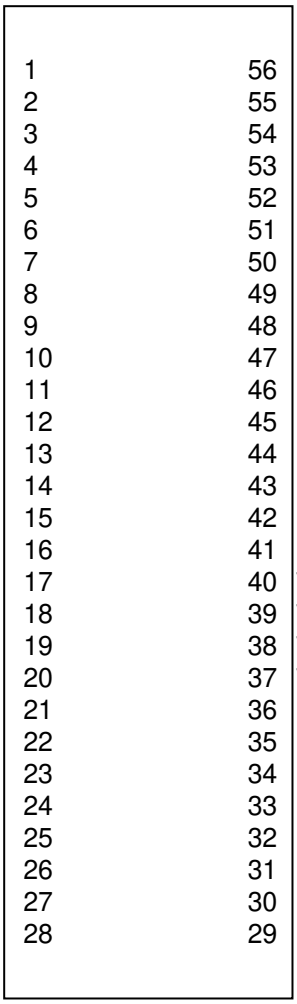

PWRBTN#
ADDR [0:1]
IRQ/SMI#
OVT#/BEEP
Beep/Alert Generator
Control Circuit & Value Ram
ASF Command Decoder
SMBus Interface
SMBus & ARP Control
SCL
SDA
Current Dispatcher
Channel Mux
10-bits Delta_sigma ADC
Vtt
D+1
D-1
Amplify Circuit
Intel PECI Interface
PECI
THR [1:2]
VCORE
VSEN [1:4]
Fan Control
FANIN [1:12]
FANCTRL [1:8]
VREF
Band Gap Reference
Watch Dog Timer
VID Control
Caseopen Detection
Caseopen
W83793AG
SYSRSTIN#
WDTRST#
VIDA 7:0

5. PIN CONFIGURATION

W83793G (56 SSOP)

CLK	1	56	VIDB7/FANCTL8
OVT#/BEEP	2	55	VIDB6/FANIN8
IRQ/SMI#	3	54	VIDB5/FANCTL7
SCL	4	53	VIDB4/FANIN7
SDA	5	52	VIDB3/FANCTL6
PWRBTN#	6	51	VIDB2/FANIN6
5VSB	7	50	VIDB1/FANCTL5
CASEOPEN#	8	49	VIDB0/FANCTL4
VBAT	9	48	FANIN5
VIDA4/FANIN8	10	47	FANIN4
VIDA5/FANCTL8	11	46	FANCTL3/VIDBSEL
VIDA6	12	45	FANIN3
VIDA7	13	44	FANCTL2/ADDR1
WDTRST#	14	43	FANIN2
SYSRSTIN#	15	42	FANCTL1/ADDR0
GND	16	41	FANIN1
PECI	17	40	VIDA3/FANIN12
VTT	18	39	VIDA2/FANIN11
VSEN1	19	38	VIDA1/FANIN10
VSEN2	20	37	VIDA0/FANIN9
VSEN4	21	36	4_D-
VSEN3	22	35	4_D+
VCOREA	23	34	3_D-
VCOREB	24	33	3_D+
5VDD	25	32	2_D-
VREF	26	31	2_D+
THR1	27	30	1_D-
THR2	28	29	1_D+

W83793AG (56 SSOP)



CLK	1	56	FANCTL8
OVT#/BEEP	2	55	FANIN8
IRQ/SMI#	3	54	FANCTL7
SCL	4	53	FANIN7
SDA	5	52	FANCTL6
PWRBTN#	6	51	FANIN6
5VSB	7	50	FANCTL5
CASEOPEN#	8	49	FANCTL4
VBAT	9	48	FANIN5
VIDA4/FANIN8	10	47	FANIN4
VIDA5/FANCTL8	11	46	FANCTL3
VIDA6	12	45	FANIN3
VIDA7	13	44	FANCTL2/ADDR1
WDTRST#	14	43	FANIN2
SYSRSTIN#	15	42	FANCTL1/ADDR0
GND	16	41	FANIN1
PECI	17	40	VIDA3/FANIN12
VTT	18	39	VIDA2/FANIN11
VSEN1	19	38	VIDA1/FANIN10
VSEN2	20	37	VIDA0/FANIN9
VSEN4	21	36	NC
VSEN3	22	35	NC
VCOREA	23	34	NC
NC	24	33	NC
5VDD	25	32	NC
VREF	26	31	NC
THR1	27	30	1_D-
THR2	28	29	1_D+

6. PIN DESCRIPTION

6.1 Pin Type Description

SYMBOL	DESCRIPTION
t	TTL level
v1	Vil/Vih=0.4/0.6 level
v2	Vil/Vih=0.8/1.4 level
v3	Vtt level
s	Schmitt trigger
12	12mA sink/source capability
OUT	Output pin
OD	Open-drain output pin
AOUT	Output pin (Analog)
IN	Input pin (digital)
AIN	Input pin(Analog)

6.2 Pin Description List

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
CLK	1	5VSB	IN_{ts}	48MHz System clock while 5VDD is powered up. PECI and the fan will use this clock to drive logics.
OVT#	2	5VSB	OD_{12}	Over temperature alert. Low active.
BEEP				BEEP output when any abnormal event occurs. If there is no abnormal event, this pin asserts low.
IRQ	3	5VSB	OUT_{12}	Interrupt request output when abnormal events occur.
SMI#			OD_{12}	System Management Interrupt (open drain).
SCL	4	5VSB	IN_{ts}	Serial Bus Clock.
SDA	5	5VSB	IN/OD_{12ts}	Serial Bus bi-directional data.

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
PWRBTN#	6	5VSB	OD_{12}	Power Button output signal to enable/ disable the power supply. This pin is related to ASF commands.
5VSB	7	-	POWER	This pin is the power source for the W83793G. Bypass with the parallel combination of 10μF (electrolytic or tantalum) and 0.1μF (ceramic) bypass capacitors.
CASEOPEN#	8	VBAT	IN_{ts}	CASE OPEN detection. An active low input from an external device when case is opened. This signal will be latched even when the case is closed.
VBAT	9		POWER	VBAT supplies power for CASEOPEN#. It is also a voltage monitor channel.
VIDA4	10	5VSB	IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 4 from CPU A. (Default)
FANIN8			IN_{ts}	0V to +5V amplitude fan tachometer input
VIDA5	11	5VSB	IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 5 from CPU A. (Default)
FANCTL8			OUT / OD_{12a}	FAN control output. The 8th fan control signal can be programmed to output through pin 56 or this pin. When this pin is programmed to be fan control signal, it only supports the PWM mode.
FANIN12			IN_{ts}	0V to +5V amplitude fan tachometer input
VIDA6	12	5VSB	IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 6 from CPU A.
VIDA7	13	5VSB	IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 7 from CPU A. (Default)
WDTRST#	14	5VSB	OD_{12}	Low active system reset. If triggered, this pin will send out 100ms low pulse for system reset.
SYSRSTIN#	15	5VSB	IN_{ts}	System reset input, used to control WDT.
GND	16		POWER	System Ground.
PECI	17	5VSB	IN/O_{V3}	Intel® CPU PECI interface
VTT	18		POWER	Intel® CPU Vtt power

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
VSEN1	19		AIN	Voltage sensor input. The detection range is 0~4.096V
VSEN2	20		AIN	Voltage sensor input. The detection range is 0~4.096V
VSEN4	21	-	AIN	Voltage sensor input. The detection range is 0~2.048V.
VSEN3	22		AIN	Voltage sensor input. The detection range is 0~4.096V.
VCOREA	23		AIN	CPU A core voltage input. The detection range is 0~2.048V
VCOREB*	24		AIN	CPU B Core Voltage Input. The detection range is 0~2.048V.
5VDD	25	-	POWER	+5V VDD power. Bypass with the parallel combination of 10μF (electrolytic or tantalum) and 0.1μF (ceramic) bypass capacitors.
VREF	26		AOUT	Reference voltage output.
THR1	27		AIN	Thermistor 1 terminal input.
THR2	28		AIN	Thermistor 2 terminal input.
1_D+	29		AIN	Thermal diode 1 D+.
1_D-	30		AIN	Thermal diode 1 D-.
2_D+*	31		AIN	Thermal diode 2 D+.
2_D-*	32		AIN	Thermal diode 2 D-.
3_D+*	33		AIN	Thermal diode 3 D+.
3_D-*	34		AIN	Thermal diode 3 D-.
4_D+*	35		AIN	Thermal diode 4 D+.
4_D-*	36		AIN	Thermal diode 4 D-.
VIDA0	37	5VSB	IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 0 from CPU A. (Default)

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
FANIN9			IN_{ts}	0V to +5V amplitude fan tachometer input
VIDA1	38	5VSB	IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 1 from CPU A. (Default)
FANIN10			IN_{ts}	0V to +5V amplitude fan tachometer input
VIDA2	39	5VSB	IN_{v1s}	Voltage Supply readouts bit 2 from CPU A. (Default)
FANIN11			IN_{ts}	0V to +5V amplitude fan tachometer input
VIDA3	40	5VSB	IN_{v1s}	Voltage Supply readouts bit 3 from CPU A. (Default)
FANIN12			IN_{ts}	0V to +5V amplitude fan tachometer input
FANIN1	41	5VSB	IN_{ts}	0V to +5V amplitude fan tachometer input
FANCTL1	42	5VSB	OUT / OD_{12} / AOUT	Fan speed control PWM/DC output. When the power of 5VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 5VSB. As DC output, 64 steps output voltage scaled from 0 to 5VSB.
ADDR0			IN_{ts}	I^2C device address bit 0 trapping during 5VSB power on.
FANIN2	43	5VSB	IN_{ts}	0V to +5V amplitude fan tachometer input
FANCTL2	44	5VSB	OUT / OD_{12} / AOUT	Fan speed control PWM/DC output. When the power of 5VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 5VSB. As DC output, 64 steps output voltage scaled from 0 to 5VSB.
ADDR1			IN_{ts}	I^2C device address bit 1 trapping during 5VSB power on.
FANIN3	45	5VSB	IN_{ts}	0V to +5V amplitude fan tachometer input
FANCTL3	46	5VSB	OUT / OD_{12} / AOUT	Fan speed control PWM/DC output. When the power of 5VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 5VSB. As DC output, 64 steps output voltage scaled from 0 to 5VSB.

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
VIDBSEL**			IN_{ts}	The pin straps the fan mode and VID mode during 5VSB power on. When strapped to high, it will select VID mode. When strapped to low, it will select Fan mode for pin49~56.
FANIN4	47	5VSB	IN_{ts}	0V to +5V amplitude fan tachometer input
FANIN5	48	5VSB	IN_{ts}	0V to +5V amplitude fan tachometer input
FANCTL4	49	5VSB	OUT / OD_{12} / AOUT	Fan speed control PWM/DC output. When the power of 5VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 5VSB. As DC output, 64 steps output voltage scaled from 0 to 5VSB.
VIDB0*			IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 0 from CPU B.
FANCTL5	50	5VSB	OUT / OD_{12} / AOUT	Fan speed control PWM/DC output. When the power of 5VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 5VSB. As DC output, 64 steps output voltage scaled from 0 to 5VSB.
VIDB1*			IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 1 from CPU B.
FANIN9			INts	0V to +5V amplitude fan tachometer input
FANIN6	51	5VSB	INts	0V to +5V amplitude fan tachometer input
VIDB2*			IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 2 from CPU B.
FANCTL6	52	5VSB	OUT / OD_{12} / AOUT	Fan speed control PWM/DC output. When the power of 5VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 5VSB. As DC output, 64 steps output voltage scaled from 0 to 5VSB.
FANIN10			INts	0V to +5V amplitude fan tachometer input
VIDB3*			IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 3 from CPU B.
FANIN7	53	5VSB	INts	0V to +5V amplitude fan tachometer input

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
VIDB4*			IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 4 from CPU B.
FANCTL7	54	5VSB	OUT / OD_{12} / AOUT	Fan speed control PWM/DC output. When the power of 5VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 5VSB. As DC output, 64 steps output voltage scaled from 0 to 5VSB.
FANIN11			INts	0V to +5V amplitude fan tachometer input
VIDB5*			IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 5 from CPU B.
FANIN8	55	5VSB	IN_{ts}	0V to +5V amplitude fan tachometer input
VIDB6*			IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 6 from CPU B.
FANCTL8	56	5VSB	OUT / OD_{12} / AOUT	Fan speed control PWM/DC output. The 8^{th} fan control signal can be programmed to output through pin 11 or this pin. When the power of 5VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 5VSB. As DC output, 64 steps output voltage scaled from 0 to 5VSB.
VIDB7*			IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 7 from CPU B.

Pins with * are for the W83793G only, not for the W83793AG.

Pins with ** are for the W83793G only. Please always strap low to select FANIN or FANCTL for the W83793AG.

7. FUNCTIONAL DESCRIPTION

This section is blank now. Refer to Chap 8 for function description.

8. CONFIGURATION REGISTERS

8.1 ID, Bank Select Registers

Inside the W83793G resides three banks of registers. Customers must set the banks correctly to access correct registers. All the registers described here can be accessed in all banks.

8.1.1 ID, Bank Select Registers Map

Address 00_{HEX}, $0D_{HEX}$, $0E_{HEX}$, $0F_{HEX}$ in all three register banks are reserved as ID and Bank Select registers.

Mnemonic	Register Name	Type
BankSel.	Bank Select	RW
VendorID.	Nuvoton Vendor ID	RO
ChipID.	Nuvoton Chip ID	RO
DeviceID.	Nuvoton Device Version ID	RO

8.1.2 ID, Bank Select Register Details

8.1.2.1. Bank Select Register (Bank Select)

Three banks of registers are inside the W83793G. The register bank could be selected by programming the Bank Select register. All 00_{HEX} Addresses in these three banks are defined as Bank Select register.

Location: Bank 0, 1, 2 Address 00_{HEX}
Type: Read / Write
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

BANKSELECT

BIT	7	6	5	4	3	2	1	0
NAME	HBACS	Reserve				BANK Select		
RESET	1	0_{HEX}				0_{HEX}		

BIT	DESCRIPTION
7	**HBACS** (High Byte Access) 0: Return the low byte while reading Nuvoton Vendor ID. 1: Return the high byte while reading Nuvoton Vendor ID.
6-3	Reserved.
2-0	BANK Select. 000_{BIN}: Bank 0 is selected. 001_{BIN}: Bank 1 is selected. 010_{BIN}: Bank 2 is selected.

8.1.2.2. Nuvoton Vendor ID Register (Vender ID)

The Nuvoton Vendor ID contains two-byte data. By programming register **HBACS**, the customer can choose to access either the high or the low byte of Nuvoton Vendor ID.

Location: Bank 0, 1, 2 Address $0D_{HEX}$
Type: Read Only
Reset: No Reset

VENDORID (NUVOTON VENDOR ID)

BIT	7	6	5	4	3	2	1	0
NAME	VendorID							

FIXED	$5C_{HEX}$ / $A3_{HEX}$

BIT	DESCRIPTION
7-0	VendorID. Return $5C_{HEX}$ if **HBACS** = 1; return $A3_{HEX}$ if **HBACS** = 0.

8.1.2.3. Nuvoton Chip ID Register (ChipID)

Location: Bank 0, 1, 2 Address $0E_{HEX}$
Type: Read Only
Reset: No Reset

CHIPID (NUVOTON CHIP ID)

BIT	7	6	5	4	3	2	1	0
NAME	ChipID							
RESET	$7B_{HEX}$							

BIT	DESCRIPTION
7-0	ChipID. Chip ID of W83793G is $7B_{HEX}$

8.1.2.4. Nuvoton Version ID Register (Device ID)

Location: Bank 0, 1, 2 Address $0F_{HEX}$
Type: Read Only
Reset: No Reset

VERSION ID

BIT	7	6	5	4	3	2	1	0
NAME	DeviceID							
FIXED	11_{HEX} /12_{HEX}							

BIT	DESCRIPTION
7-0	Version ID. Device ID of the W83793G. 11_{HEX} for B Version, and 12_{HEX} for C Version.

8.2 Watch Dog Timer Registers

The W83793G is integrated with a Watch Dog Timer, which enables users to reset the system by Pin 14 while the system is in an abnormal state. Once Watch Dog Timer is enabled, the W83793G starts to count down, and the host should set the timer for further count down or clear/disable the timer to prevent the W83793G from issuing reset signals.

8.2.1 Watch Dog Timer Registers Map

Watch Dog Timer consists of four registers. WDTLock and ENABLE_WDT are used to activate Soft-WDT and Hard-WDT, respectively. WDT_STS and DownCounter can inform the host whether the system time is up or not.

Mnemonic	Register Name	Type
WDTLock.	Lock Watch Dog	WO
EnableWDT.	Watch Dog Enable	RO
WDT_STS.	Watch Dog Status	R/W
DownCounter.	Watch Dog Timer	R/W

Two kinds of watchdog timer functions are supported by the W83793G. One is so-called Soft Watch Dog Timer, and the other is Hard Watch Dog Timer.

Hard Watch Dog timer, if enabled, will start a 4-minute WDT after the system reset is completed. (A low-to-high transition on SYSRSTIN# pin). BIOS needs to write a 00_{HEX} into Watch Dog Timer Register (04_{HEX}) to disable the timer within 4 minutes. Otherwise, Pin 14 WDTRST# will assert to reset the system.

Soft Watch Dog Timer will start counting down whenever Timeout Time is set and Soft Watch Dog Timer is enabled. WDTRST# will be issued when the time runs out.

Soft Watch Dog Timer will be disabled automatically after receiving a SYSRSTIN_N low signal.

Bank0, CR40 [2]/**ENWDT** must be set to 1 if wish to program the four Watch Dog Timer Registers.