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WINBOND I/O

W83877TF/W83877TG

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1. GENERAL DESCRIPTION

W83877TF/TG is an enhanced version from Winbond's most popular I/O chip W83877F --- which integrates the disk drive adapter, serial port (UART), IrDA 1.0 SIR, parallel port, configurable Plug-and-Play registers for the whole chip --- plus additional powerful features: **ACPI** / legacy power management, **serial IRQ,** and **IRQ sharing**.

The disk drive adapter functions of W83877TF/TG include a floppy disk controller compatible with the industry standard 82077/765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, interrupt and DMA logic. The wide range of functions integrated into W83877TF/TG greatly reduces the number of components required for interfacing with floppy disk drives. W83877TF/TG supports four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data transfer rates of 250 Kb/S, 300 Kb/S, 500 Kb/S,1 Mb/S, and 2 Mb/S.

W83877TF/TG provides two high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. One of the UARTs support infrared (IR) IrDA1.0. Both UARTs provide legacy speed with baud rate up to 115.2K and provide advanced speed with baud rate up to **230k**, **460k**, and **921k bps** which support higher speed Modems.

W83877TF/TG supports one PC-compatible printer port (SPP), Bi-directional printer port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). Through the printer port interface pins, also available are: Extension FDD Mode and Extension 2FDD Mode allowing one or two external floppy disk drives to be connected. This function is especially valuable for notebook computer applications.

Winbond W83877TF/TG provides functions that comply with **ACPI** (Advanced Configuration and Power Interface), which includes support of legacy and ACPI power management through SMI or SCI function pins. One 24-bits power management timer is implemented with the carry notify interrupt. W83877TF/TG also has auto power management mode to reduce the power consumption.

The **serial IRQ** for PCI architecture is supported, ISA IRQs (IRQ1~IRQ15) can be cascaded into one IRQSER pin. W83877TF/TG also features ISA bus **IRQ sharing** and allows two or more devices to share the same IRQ pin.

W83877TF/TG is made to fully comply with **Microsoft™ PC97 Hardware Design Guide**. IRQs, DMAs, and I/O space resources are flexible to adjust to meet ISA PnP requirement. Moreover W83877TF/TG is made to meet the specification of PC97's requirement in the power management: **ACPI** and **DPM** (Device Power Management).

The configuration registers support mode selection, function enable/disable, and power down function selection. Furthermore, the configurable PnP registers are compatible with the Plug-and-Play feature demand of Windows 95™ , which makes system resource allocation more efficient than ever.

Another benefit of W83877TF/TG is that it is pin-to-pin compatible to W83877F, and all of the 100-pin Winbond I/O IC family. Thus makes the design of applications very convenient and flexible.

2. FEATURES

General:

- Plug & Play 1.0A Compliant
- Support 8 IRQs (ISA), or 15 IRQs (Serial IRQ), 3 DMA channels, and 480 re-locatable address
- Capable of ISA Bus **IRQ Sharing**
- Comply with **Microsoft PC 97** Hardware Design Guide
- Support **DPM** (Device Power Management), **ACPI**
- Report ACPI status interrupt by SCI signal from $\overline{\text{SCI}}$ pin, serial IRQ IRQSER pin, or IRQ A~H pins
- Single 24MHz/48MHZ clock input

FDC:

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- DMA enable logic
- Supports floppy disk drives and tape drives
- Detects all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD write enable signal (write data signalwas forced to be inactive)
- Supports up to four 3.5-inch or 5.25-inch floppy disk drives
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Supports vertical recording format
- **Support 3-mode FDD, and its Win95 driver**
- 16-byte data FIFOs

UART:

- Two high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs
- MIDI compatible
- Fully programmable serial-interface characteristics:
  - 5, 6, 7 or 8-bit characters
  - Even, odd or no parity bit generation/detection
  - 1, 1.5 or 2 stop bits generation
- Internal diagnostic capabilities:
  - Loop-back controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation

- Programmable baud generator allows division of 1.8461 MHz and 24 MHz by 1 to (2^{16}-1)
- Maximum baud rate is up to 921k bps for 14.768MHz and 1.5M bps for 24MHz

Infrared:

- Supports IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Supports SHARP ASK-IR protocol with maximum baud rate up to 57600 bps

Parallel Port:

- Compatible with IBM parallel port
- Supports PS/2 compatible bi-directional parallel port
- Supports Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- Supports Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- Extension FDD mode supports disk drive B; and Extension 2FDD mode supports disk drives A and B through parallel port
- Enhanced printer port back-drive current protection

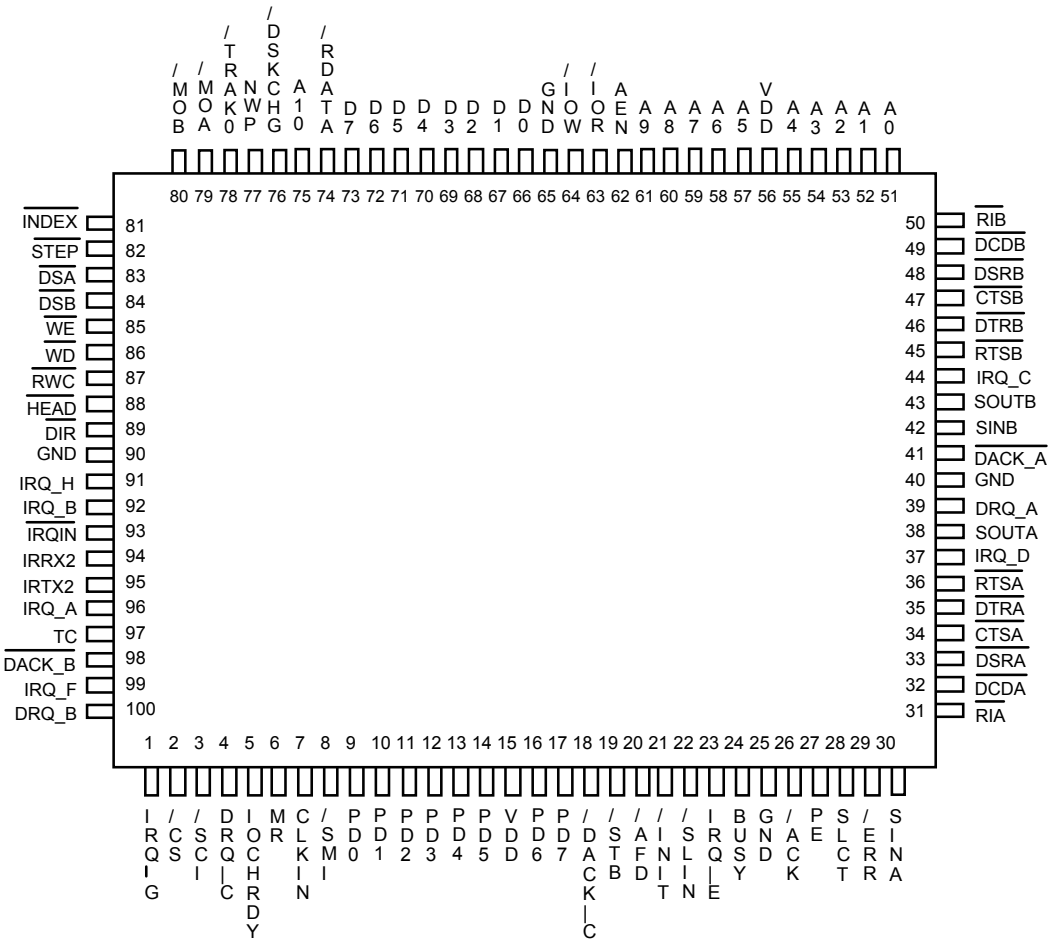
Others:

- Programmable configuration settings
- Immediate or automatic power-down mode for the power management
- All hardware power-on settings have internal pull-up or pull-down resistors as default value
- Dedicated Infrared Communication Pins

Package:

- 100-pin QFP (W83877TF/TG), and also 100-pin LQFP (W83877TD/TG)

3. PIN CONFIGURATION



4. PIN DESCRIPTION

(Note: Refer to section 12.2 DC CHARACTERISTICS for details.)

I/O8tc - TTL level output pin with 8 mA source-sink capability; CMOS level input voltage

I/O12t - TTL level bi-directional pin with 12 mA source-sink capability

I/O24t - TTL level bi-directional pin with 24 mA source-sink capability

OUT8t - TTL level output pin with 8 mA source-sink capability

OUT12t - TTL level output pin with 12 mA source-sink capability

OD12 - Open-drain output pin with 12 mA sink capability

OD24 - Open-drain output pin with 24 mA sink capability

INt - TTL level input pin

INts - TTL level Schmitt-triggered input pin

INc - CMOS level input pin

INcs - CMOS level Schmitt-triggered input pin

4.1 Host Interface

SYMBOL	PIN	I/O	FUNCTION
D0–D7	66-73	I/O_{24t}	System data bus bits 0-7.
A0–A9	51-55 57-61	IN_t	System address bus bits 0-9.
A10	75	IN_t	In ECP Mode, this pin is the A10 address input.
IOCHRDY	5	OD_{24}	In EPP Mode, this pin is the IO Channel Ready output to extend the host read/write cycle.
MR	6	IN_{ts}	Master Reset. Active high. MR is low during normal operations.
$\overline{CS}$	2	IN_t	Active low chip select signal.
AEN	62	IN_t	System address bus enable.
$\overline{IOR}$	63	IN_{ts}	CPU I/O read signal.
$\overline{IOW}$	64	IN_{ts}	CPU I/O write signal.
DRQ_B	100	OUT_{12t}	DMA request signal B.
$\overline{DACK\_B}$	98	IN_{ts}	DMA Acknowledge signal B.
DRQ_C	4	OUT12t	DMA request signal C.
$\overline{DACK\_C}$	18	INts	DMA Acknowledge signal C.
TC	97	INts	Terminal Count. When active, this pin indicates termination of a DMA transfer.
IRQIN	93	INt	Interrupt request input for IRQ routing ; For example , the IRQ12 can be routed into this port when PS/2 mouse is not installed.

Host Interface, continued

SYMBOL	PIN	I/O	FUNCTION
IRQ_A	96	OUT_{12t}	Interrupt request signal A, when CR16 Bit 5 (G1IQSEL) = 0.
GIO1		I/O_{12t}	General Purpose I/O port 1, when CR16 Bit 5 (G1IQSEL) = 1.
IRQ_B	92	OUT_{12t}	Interrupt request signal B, when CR16 Bit 4 (G0IQSEL) = 0.
GIO0		I/O_{12t}	General Purpose I/O port 0, when CR16 Bit 4 (G0IQSEL) = 1.
IRQ_C	44	OUT_{12t}	Interrupt request signal C.
IRQ_D	37	OUT_{12t}	Interrupt request signal D.
IRQ_E	23	OUT_{12t}	Interrupt request signal E.
IRQ_F	99	OUT_{12t}	Interrupt request signal F.
IRQ_G	1	OUT_{12t}	Interrupt request signal G.
PCICLK		IN_t	PCI clock input, when the serial IRQ function is selected.
IRQ_H	91	OUT_{12t}	Interrupt request signal H.
SERIRQ		I/O_{12t}	Serial interrupt input/output, when the Serial IRQ mode is selected by setting IRQMODS bit in CR31 register.
$\overline{SCI}$	3	OD_{12}	For the ACPI power management, $\overline{SCI}$ is active low 200ns for the power management events, which generate an SCI interrupt in the ACPI mode.
CLKIN	7	IN_t	24MHz/48MHZ clock input. CLKINSEL bit in CR2C register should be correctly reset/set according to the input frequency.
$\overline{SMI}$	8	OD_{12}	For the legacy power management, the $\overline{SMI}$ is active low 200ns for the power management events, which generate an SMI interrupt in the legacy power management mode. This SMI output is enabled by setting the SMI_EN bit in CR3A register.
$\overline{DACK\_A}$	41	IN_{ts}	DMA acknowledge signal A.
DRQ_A	39	OUT_{12t}	DMA request signal A.

4.2 Serial Port Interface

SYMBOL	PIN	I/O	FUNCTION
SINA SINB/IRRX1	30 42	IN_t	Serial Input. It is used to receive serial data from the communication link.
$\overline{RIA}$ $\overline{RIB}$	31 50	IN_t	Ring Indicator. An active low indicates that a ring signal is being received by the modem or data set.
$\overline{DCDA}$ $\overline{DCDB}$	32 49	IN_t	Data Carrier Detect. An active low indicates the modem or data set has detected a data carrier.
$\overline{DSRA}$ $\overline{DSRB}$	33 48	IN_t	Data Set Ready. An active low indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
$\overline{CTSA}$	34	IN_t	Clear To Send. It is the modem control input.
$\overline{CTSB}$	47		The function of these pins can be tested by reading Bit 4 of the handshake status register.
$\overline{DTRA}$	35	I/O_{8tc}	UART A Data Terminal Ready. An active low informs the modem or data set that the controller is ready to communicate.
PHEFRAS			During power-on reset, this pin is pulled down internally and is defined as PHEFRAS, which provides the power-on value for CR16 bit 0 (HEFRAS). While it is at Low, it selects the EFER (Extended Functions Enable Register) to be 250H. While it is at High, it selects the EFER to be 3F0H. A 4.7 kΩ is recommended when intends to pull up at power-on reset.
$\overline{RTSA}$	36	I/O_{8tc}	UART A Request To Send. An active low informs the modem or data set that the controller is ready to send data.
PPNPCVS			During power-on reset, this pin is pulled up internally and is defined as PPNPCVS, which provides the power-on value for CR16 bit 2 (PNPCVS). While it is at Low, all PnP-related registers (CR20 to CR29) are all set to be 0s. While it is at High, all PnP-related registers (CR20 to CR 29) are set to default values. A 4.7 kΩ is recommended when intends to pull down at power-on reset.
SOUTA	38	I/O_{8tc}	UART A Serial Output. It is used to transmit serial data out to the communication link.
PENFDC			During power-on reset, this pin is pulled up internally and used to enable or disable the FDC. While it is at Low, FDC PnP-related register (CR20) is set to be 0, i.e. FDC is disabled. While it is at High, CR20 is set to the default value, i.e. FDC is enabled. A 4.7 kΩ is recommended when intends to pull down at power-on reset.

Serial Port Interface, continued

SYMBOL	PIN	I/O	FUNCTION
SOUTB IRTX1 PIRQMDS	43	I/O_{8tc}	UART B Serial Output. It is used to transmit serial data out to the communication link. During power-on reset, this pin is pulled down internally and is defined as PIRQMDS to select the IRQ mode. While it is at Low, IRQ pins can be set to Normal mode or IRQ sharing mode which decided by CR18. If it is at High, the Serial IRQ mode is selected. A 4.7 kΩ is recommended when intending to pull up at power-on reset.
$\overline{RTSB}$	45	I/O_{8tc}	UART B Request To Send. An active low informs the modem or data set that the controller is ready to send data.
PGOIQSEL			During power-on reset, this pin is pulled down internally and is defined as PGOIQSEL, which provides the power-on value for CR16 bit 4 and bit 5 (G0IQSEL & G1IQSEL). While it is at Low, pins 92 and 96 function as IRQ pins IRQ_B,IRQ_A respectively. While it is at high, pins 92 and 96 function as General Purpose I/O pins GIO0,GIO1 respectively. A 4.7 kΩ is recommended when intends to pull up at power-on reset.
$\overline{DTRB}$	46	I/O_{8tc}	UART B Data Terminal Ready. An active low informs the modem or data set that the controller is ready to communicate.
IRTX2	95	OUT_{12t}	Functions as a InfraRed data transmission line.
IRRX2	94	IN_t	Functions as a InfraRed data receiving line.

4.3 Multi-Mode Parallel Port

The following pins have six functions, which are controlled by bits PRTMOD0, PRTMOD1, and PRTMOD2 of CR0 and CR9 (refer to section 11.0, Extended Functions).

SYMBOL	PIN	I/O	FUNCTION
BUSY	24	IN_t	PRINTER MODE: BUSY An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{MOB2}$ This pin is for Extension FDD B; the function of this pin is the same as that of the $\overline{MOB}$ pin.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{MOB2}$ This pin is for Extension FDD A and B; the function of this pin is the same as that of the $\overline{MOB}$ pin.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
$\overline{ACK}$	26	IN_t	PRINTER MODE: $\overline{ACK}$ An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{DSB2}$ This pin is for the Extension FDD B; its functions are the same as those of the $\overline{DSB}$ pin.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{DSB2}$ This pin is for Extension FDD A and B; the function of this pin is the same as that of the $\overline{DSB}$ pin.
PE	27	IN_t	PRINTER MODE: PE An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{WD2}$ This pin is for Extension FDD B; its function is the same as that of the $\overline{WD}$ pin.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{WD2}$ This pin is for Extension FDD A and B; this function of this pin is the same as that of the $\overline{WD}$ pin.
SLCT	28	IN_t	PRINTER MODE: SLCT An active high input on this pin indicates that the printer is selected. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: WE2 This pin is for Extension FDD B; its functions are the same as those of the $\overline{WE}$ pin.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{WE2}$ This pin is for Extension FDD A and B; this function of this pin is the same as that of the $\overline{WE}$ pin.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
$\overline{ERR}$	29	IN_t	PRINTER MODE: $\overline{ERR}$ An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{HEAD2}$ This pin is for Extension FDD B; its function is the same as that of the $\overline{HEAD}$ pin.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{HEAD2}$ This pin is for Extension FDD A and B; its function is the same as that of the $\overline{HEAD}$ pin.
$\overline{SLIN}$	22	OD_{12}	PRINTER MODE: $\overline{SLIN}$ Output line for detection of printer selection. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{STEP2}$ This pin is for Extension FDD B; its function is the same as that of the $\overline{STEP}$ pin.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{STEP2}$ This pin is for Extension FDD A and B; its function is the same as that of the $\overline{STEP}$ pin .
$\overline{INIT}$	21	OD_{12}	PRINTER MODE: $\overline{INIT}$ Output line for the printer initialization. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{DIR2}$ This pin is for Extension FDD B; its function is the same as that of the $\overline{DIR}$ pin.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{DIR2}$ This pin is for Extension FDD A and B; its function is the same as that of the $\overline{DIR}$ pin.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
$\overline{AFD}$	20	OD12	PRINTER MODE: $\overline{AFD}$ An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{RWC2}$ This pin is for Extension FDD B; its function is the same as that of the $\overline{RWC}$ pin.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{RWC2}$ This pin is for Extension FDD A and B; its function is the same as that of the $\overline{RWC}$ pin.
$\overline{STB}$	19	OD_{12}	PRINTER MODE: $\overline{STB}$ An active low output is used to latch the parallel data into the printer. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		- -	EXTENSION FDD MODE: NC pin EXTENSION 2FDD MODE: NC pin
PD0	9	I/O_{24t}	PRINTER MODE: PD0 Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: $\overline{INDEX2}$ This pin is for Extension FDD B; the function of this pin is the same as that of the $\overline{INDEX}$ pin. This pin is pulled high internally.
		IN_t	EXTENSION 2FDD MODE: $\overline{INDEX2}$ This pin is for Extension FDD A and B; this function of this pin is the same as $\overline{INDEX}$ pin. This pin is pulled high internally.
PD1	10	I/O24t	PRINTER MODE: PD1 Parallel port data bus bit 1. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		INt	EXTENSION FDD MODE: $\overline{TRAK02}$ This pin is for Extension FDD B; the function of this pin is the same as that of the $\overline{TRAK0}$ pin. This pin is pulled high internally.
		INt	EXTENSION. 2FDD MODE: $\overline{TRAK02}$ This pin is for Extension FDD A and B; this function of this pin is the same as $\overline{TRAK0}$ pin. This pin is pulled high internally.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
PD2	11	I/O24t	PRINTER MODE: PD2 Parallel port data bus bit 2. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: $\overline{WP2}$ This pin is for Extension FDD B; the function of this pin is the same as that of the $\overline{WP}$ pin. This pin is pulled high internally.
		IN_t	EXTENSION. 2FDD MODE: $\overline{WP2}$ This pin is for Extension FDD A and B; this function of this pin is the same as that of the $\overline{WP}$ pin. This pin is pulled high internally.
PD3	12	I/O_{24t}	PRINTER MODE: PD3 Parallel port data bus bit 3. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: $\overline{RDATA2}$ Motor on B for Extension FDD B; the function of this pin is the same as that of the $\overline{RDATA}$ pin. This pin is pulled high internally.
		IN_t	EXTENSION 2FDD MODE: $\overline{RDATA2}$ This pin is for Extension FDD A and B; this function of this pin is the same as that of the $\overline{RDATA}$ pin. This pin is pulled high internally.
PD4	13	I/O24t	PRINTER MODE: PD4 Parallel port data bus bit 4. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		INt	EXTENSION FDD MODE: $\overline{DSKCHG2}$ Drive select B for Extension FDD B; the function of this pin is the same as that of $\overline{DSKCHG}$ pin. This pin is pulled high internally.
		INt	EXTENSION 2FDD MODE: $\overline{DSKCHG2}$ This pin is for Extension FDD A and B; this function of this pin is the same as that of the $\overline{DSKCHG}$ pin. This pin is pulled high internally.
PD5	14	I/O24t I/O24t I/O24t	PRINTER MODE: PD5 Parallel port data bus bit 5. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: This pin is a tri-state output. EXTENSION 2FDD MODE: This pin is a tri-state output.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
PD6	16	I/O_{24t}	PRINTER MODE: PD6 Parallel port data bus bit 6. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: NC pin
		OD_{24}	EXTENSION. 2FDD MODE: $\overline{MOA2}$ This pin is for Extension FDD A; its function is the same as that of the $\overline{MOA}$ pin.
PD7	17	I/O_{24t}	PRINTER MODE: PD7 Parallel port data bus bit 7. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: NC pin
		OD_{24}	EXTENSION 2FDD MODE: $\overline{DSA2}$ This pin is for Extension FDD A; its function is the same as that of the $\overline{DSA}$ pin.

4.4 FDC Interface

SYMBOL	PIN	I/O	FUNCTION
$\overline{WE}$	85	OD_{24}	Write enable. An open drain output.
$\overline{DIR}$	89	OD_{24}	Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
$\overline{HEAD}$	88	OD_{24}	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
$\overline{RWC}$	87	OD_{24}	Reduced write current. This signal can be used on two-speed disk drives to select the transfer rate. An open drain output. Logic 0 = 250 Kb/s Logic 1 = 500 Kb/s When bit 5 of CR9 (EN3MODE) is set to high, the three-mode FDD function is enabled, and the pin will have a different definition. Refer to the EN3MODE bit in CR9.
$\overline{WD}$	86	OD_{24}	Write data. This logic low open drain writes precompensation serial data to the selected FDD. An open drain output.
$\overline{STEP}$	82	OD_{24}	Step output pulses. This active low open drain output produces a pulse to move the head to another track.

FDC Interface, continued

SYMBOL	PIN	I/O	FUNCTION
$\overline{\text{INDEX}}$	81	IN_{cs}	This schmitt input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN).
$\overline{\text{TRAK0}}$	78	IN_{cs}	Track 0. This schmitt input from the disk drive is active low when the head is positioned over the outermost track. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN).
$\overline{\text{WP}}$	77	IN_{cs}	Write protected. This active low schmitt input from the disk drive indicates that the diskette is write-protected. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN).
$\overline{\text{RDATA}}$	74	IN_{cs}	The read data input signal from the FDD. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN).
$\overline{\text{DSKCHG}}$	76	IN_{cs}	Diskette change. This signal is active low at power on and whenever the diskette is removed. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN).
$\overline{\text{MOA}}$	79	OD_{24}	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
$\overline{\text{MOB}}$	80	OD_{24}	Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output.
$\overline{\text{DSA}}$	83	OD_{24}	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
$\overline{\text{DSB}}$	84	OD_{24}	Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output.
VDD	15, 56		+5 power supply for the digital circuitry.
GND	25, 40 65, 90		Ground.

5. FDC FUNCTIONAL DESCRIPTION

5.1 W83877TF/TG FDC

The floppy disk controller of W83877TF/TG integrates all of the logic required for floppy disk control. The FDC implements a PC/AT or PS/2 solution. All programmable options default to compatible values. The FIFO provides better system performance in multi-master systems. The digital data separator supports up to data rate 1 M bits/sec. (2 M bits/sec for fast tape drive)

The FDC includes the following blocks: AT interface, Precompensation, Data Rate Selection, Digital Data Separator, FIFO, and FDC Core.

5.1.1 AT interface

The interface consists of the standard asynchronous signals: $\overline{RD}$, $\overline{WR}$, A0-A3, IRQ, DMA control, and a data bus. The address lines select between the configuration registers, the FIFO and control/status registers. This interface can be switched between PC/AT, Model 30, or PS/2 normal modes. The PS/2 register sets are a superset of the registers found in a PC/AT.

5.1.2 FIFO (Data)

The FIFO is 16 bytes in size and has programmable threshold values. All command parameter information and disk data transfers go through the FIFO. Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The FIFO defaults to disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the CONFIGURE command. The advantage of the FIFO is that it allows the system a larger DMA latency without causing disk errors. The following tables give several examples of the delays with a FIFO. The data are based upon the following formula:

THRESHOLD × (1/Data Rate) *8 - 1.5 μS = DELAY

FIFO THRESHOLD	MAXIMUM DELAY TO SERVICING AT 500K BPS
	Data Rate
1 Byte	1 × 16 μS - 1.5 μS = 14.5 μS
2 Byte	2 × 16 μS - 1.5 μS = 30.5 μS
8 Byte	8 × 16 μS - 1.5 μS = 6.5 μS
15 Byte	15 × 16 μS - 1.5 μS = 238.5 μS
FIFO THRESHOLD	**MAXIMUM DELAY TO SERVICING AT 1M BPS**
	Data Rate
1 Byte	1 × 8 μS - 1.5 μS = 6.5 μS
2 Byte	2 × 8 μS - 1.5 μS = 14.5 μS
8 Byte	8 × 8 μS - 1.5 μS = 62.5 μS
15 Byte	15 × 8 μS - 1.5 μS = 118.5 μS

At the start of a command the FIFO is always disabled and command parameters must be sent based upon the RQM and DIO bit settings in the main status register. When the FDC enters the command execution phase, it clears the FIFO of any data to ensure that invalid data are not transferred.

An overrun and underrun will terminate the current command and the data transfer. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

DMA transfers are enabled with the SPECIFY command and are initiated by the FDC by activating the DRQ pin during a data transfer command. The FIFO is enabled directly by asserting $\overline{\text{DACK}}$ and addresses need not be valid.

Note that if the DMA controller is programmed to function in verify mode a pseudo read is performed by the FDC based only on $\overline{\text{DACK}}$. This mode is only available when the FDC has been configured into byte mode (FIFO disabled) and is programmed to do a read. With the FIFO enabled the above operation is performed by using the new VERIFY command. No DMA operation is needed.

5.1.3 Data Separator

The function of the data separator is to lock onto the incoming serial read data. When a lock is achieved the serial front end logic of the chip is provided with a clock which is synchronized to the read data. The synchronized clock, called the Data Window, is used to internally sample the serial data portion of the bit cell, and the alternate state samples the clock portion. Serial to parallel conversion logic separates the read data into clock and data bytes.

The Digital Data Separator (DDS) has three parts: control logic, error adjustment, and speed tracking. The DDS circuit cycles once every 12 clock cycles ideally. Any data pulse input will be synchronized and then adjusted by immediate error adjustment. The control logic will generate RDD and RWD for every pulse input. During any cycle where no data pulse is present, the DDS cycles are based on speed. A digital integrator is used to keep track of the speed changes in the input data stream.

5.1.4 Write Precompensation

The write precompensation logic is used to minimize bit shifts in the RDDATA stream from the disk drive. Shifting of bits is a known phenomenon in magnetic media and is dependent on the disk media and the floppy drive.

The FDC monitors the bit stream that is being sent to the drive. The data patterns that require precompensation are well known. Depending upon the pattern, the bit is shifted either early or late relative to the surrounding bits.

5.1.5 Perpendicular Recording Mode

The FDC is also capable of interfacing directly to perpendicular recording floppy drives. Perpendicular recording differs from the traditional longitudinal method in that the magnetic bits are oriented vertically. This scheme packs more data bits into the same area.

FDCs with perpendicular recording drives can read standard 3.5" floppy disks and can read and write perpendicular media. Some manufacturers offer drives that can read and write standard and perpendicular media in a perpendicular media drive.

A single command puts the FDC into perpendicular mode. All other commands operate as they normally do. The perpendicular mode requires a 1 Mbps data rate for the FDC. At this data rate the FIFO eases the host interface bottleneck due to the speed of data transfer to or from the disk.

5.1.6 Tape Drive

The W83877TF/TG supports standard tape drives (1 Mbps, 500 Kbps, 250 Kbps) and new fast tape drive (2M bps).

5.1.7 FDC Core

The W83877TF/TG FDC is capable of performing twenty commands. Each command is initiated by a multi-byte transfer from the microprocessor. The result can also be a multi-byte transfer back to the microprocessor. Each command consists of three phases: command, execution, and result.

Command

The microprocessor issues all required information to the controller to perform a specific operation.

Execution

The controller performs the specified operation.

Result

After the operation is completed, status information and other housekeeping information is provided to the microprocessor.

5.1.8 FDC Commands

Command Symbol Descriptions:

C: Cylinder number 0 - 256
D: Data Pattern
DIR: Step Direction
DIR = 0, step out
DIR = 1, step in
DS0: Disk Drive Select 0
DS1: Disk Drive Select 1
DTL: Data Length
EC: Enable Count
EOT: End of Track
EFIFO: Enable FIFO
EIS: Enable Implied Seek
EOT: End of track
FIFOTHR: FIFO Threshold
GAP: Gap length selection
GPL: Gap Length
H: Head number
HDS: Head number select
HLT: Head Load Time
HUT: Head Unload Time
LOCK: Lock EFIFO, FIFOTHR, PTRTRK bits prevent affected by software reset
MFM: MFM or FM Mode

MT: Multitrack
N: The number of data bytes written in a sector
NCN: New Cylinder Number
ND: Non-DMA Mode
OW: Overwritten
PCN: Present Cylinder Number
POLL: Polling Disable
PRETRK: Precompensation Start Track Number
R: Record
RCN: Relative Cylinder Number
R/W: Read/Write
SC: Sector/per cylinder
SK: Skip deleted data address mark
SRT: Step Rate Time
ST0: Status Register 0
ST1: Status Register 1
ST2: Status Register 2
ST3: Status Register 3
WG: Write gate alters timing of WE

5.1.9 FDC Instruction Sets

(1) Read Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	0	1	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								