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W83977ATF

W83977ATG

WINBOND I/O

winbond

W83977ATF Data Sheet Revision History

	PAGES	DATES	VERSION	VERSION ON WEB	MAIN CONTENTS
1	n.a.	08/25/97	0.50		First published.
2	53,54,58,63,64,65 , 69,138.1,139	11/17/97	0.51		Register correction
3	1,2,3,20,45,53,63, 65,99,103,150	04/01/98	0.52	A1	Typo correction and data calibrated
4	112	05/14/98	0.53	A2	spec. revision; configuration register programming method.
5	192	09/22/98	0.54	A3	Modify ordering information and top marking.
6	n.a.	05/02/06	0.6		Add lead-free package version
7					
8					
9					
10					

Table of Contents-

1. GENERAL DESCRIPTION

W83977ATF/ATG is an evolving product from Winbond's most popular I/O chip W83877F --- which integrates the disk drive adapter, serial port (UART), IrDA 1.0 SIR, parallel port, configurable plug-and-play registers for the whole chip --- plus additional powerful features: **ACPI**, 8042 keyboard controller with PS/2 mouse support, 23 general purpose I/O ports, full 16-bit address decoding, OnNow keyboard wake-up, OnNow mouse wake-up, and OnNow CIR wake-up. In addition, W83977ATF/ATG provides IR functions: **IrDA 1.1** (**MIR** for 1.152M bps or **FIR** for 4M bps) and TV remote IR (**Consumer IR**, supporting NEC, RC-5, extended RC-5, and RECS-80 protocols).

The disk drive adapter functions of W83977ATF/ATG include a floppy disk drive controller compatible with the industry standard 82077/ 765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. The wide range of functions integrated onto W83977ATF/ATG greatly reduces the number of components required for interfacing with floppy disk drives. W83977ATF/ATG supports four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s,1 Mb/s, and 2 Mb/s.

W83977ATF/ATG provides two high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. Both UARTs provide legacy speed with baud rate up to 115.2k bps and also advanced speed with baud rates of **230k**, **460k**, or **921k bps** which support higher speed modems. W83977ATF/ATG provides independent **3rd UART**(32-byte FIFO) dedicated for the IR function.

W83977ATF/ATG supports one PC-compatible printer port (SPP), Bi-directional Printer port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). Through the printer port interface pins, also available are: Extension FDD Mode and Extension 2FDD Mode allowing one or two external floppy disk drives to be connected.

The configuration registers support mode selection, function enable/disable, and power down function selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature demand of Windows 95™, which makes system resource allocation more efficient than ever.

W83977ATF/ATG provides functions that comply with **ACPI** (*Advanced Configuration and Power Interface*), which includes support of legacy and ACPI power management through $\overline{\text{SMI}}$ or $\overline{\text{SCI}}$ function pins. W83977ATF/ATG also has auto power management to reduce power consumption.

The keyboard controller is based on 8042 compatible instruction set with a 2K Byte programmable ROM and a 256-Byte RAM bank. Keyboard BIOS firmware is available with optional AMIKEY™ -2, Phoenix MultiKey/42™, or customer code.

W83977ATF/ATG provides a set of flexible I/O control functions to the system designer through a set of General Purpose I/O ports. These GPIO ports may serve as simple I/O or may be individually configured to provide a predefined alternate function.

W83977ATF/ATG is made to fully comply with **Microsoft PC97 Hardware Design Guide**. IRQs, DMAs, and I/O space resource are flexible to adjust to meet ISA PnP requirement. Moreover, W83977ATF/ATG is made to meet the specification of PC97's requirement in the power management: **ACPI** and **DPM** (Device Power Management).

Another benefit is that W83977ATF/ATG has the same pin assignment as W83977AF, W83977F, and W83977TF. This makes the design very flexible.

2. FEATURES

General

- Plug & Play 1.0A compatible
- Support 13 IRQs, 4 DMA channels, full 16-bit address decoding
- Capable of ISA Bus IRQ Sharing
- Compliant with **Microsoft PC97** Hardware Design Guide
- Support **DPM** (Device Power Management), **ACPI**
- Report ACPI status interrupt by $\overline{SCI}$ signal issued from any of the 13 IQRs pins or GPIO xx
- Programmable configuration settings
- Single 24/48 Mhz clock input

FDC

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- Support vertical recording format
- DMA enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detects all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD write enable signal (write data signal was forced to be inactive)
- Support up to four 3.5-inch or 5.25-inch floppy disk drives
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support **3-mode FDD, and its Win95 driver**

UART

- Two high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs
- MIDI compatible
- Fully programmable serial-interface characteristics:
  --- 5, 6, 7 or 8-bit characters
  --- Even, odd or no parity bit generation/detection
  --- 1, 1.5 or 2 stop bits generation
- Internal diagnostic capabilities:
  --- Loop-back controls for communications link fault isolation
  --- Break, parity, overrun, framing error simulation
- Programmable baud generator allows division of 1.8461 Mhz and 24 Mhz by 1 to (2^{16}-1)
- Maximum baud rate up to **921k bps** for 14.769 Mhz and 1.5M bps for 24 Mhz

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps
- Support IrDA version 1.1 MIR (1.152M bps) and FIR (4M bps) protocol
  --- Single DMA channel for transmitter or receiver
  --- 3rd UART with 32-byte FIFO is supported in both TX/RX transmission
  --- 8-byte status FIFO is supported to store received frame status (such as overrun CRC error, etc.)
- Support auto-config SIR and FIR

Parallel Port

- Compatible with IBM parallel port
- Support PS/2 compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- Extension FDD mode supports disk drive B; and Extension 2FDD mode supports disk drives A and B through parallel port
- Enhanced printer port back-drive current protection

Keyboard Controller

- 8042 based with optional F/W from AMIKKEY™-2, Phoenix MultiKey/42™ or customer code with 2K bytes of programmable ROM, and 256 bytes of RAM
- Asynchronous Access to Two Data Registers and One status Register
- Software compatibility with the 8042 and PC87911 microcontrollers
- Support PS/2 mouse
- Support port 92
- Support both interrupt and polling modes
- **Fast Gate A20 and Hardware Keyboard Reset**
- 8 Bit Timer/ Counter
- Support binary and BCD arithmetic
- 6MHz, 8 MHz, 12 MHz, or 16 MHz operating frequency

General Purpose I/O Ports

- 23 programmable general purpose I/O ports; 1 dedicate, 22 optional
- General purpose I/O ports can serve as simple I/O ports, interrupt steering inputs, watching dog timer output, power LED output, infrared I/O pins, general purpose address decoder, KBC control I/O pins

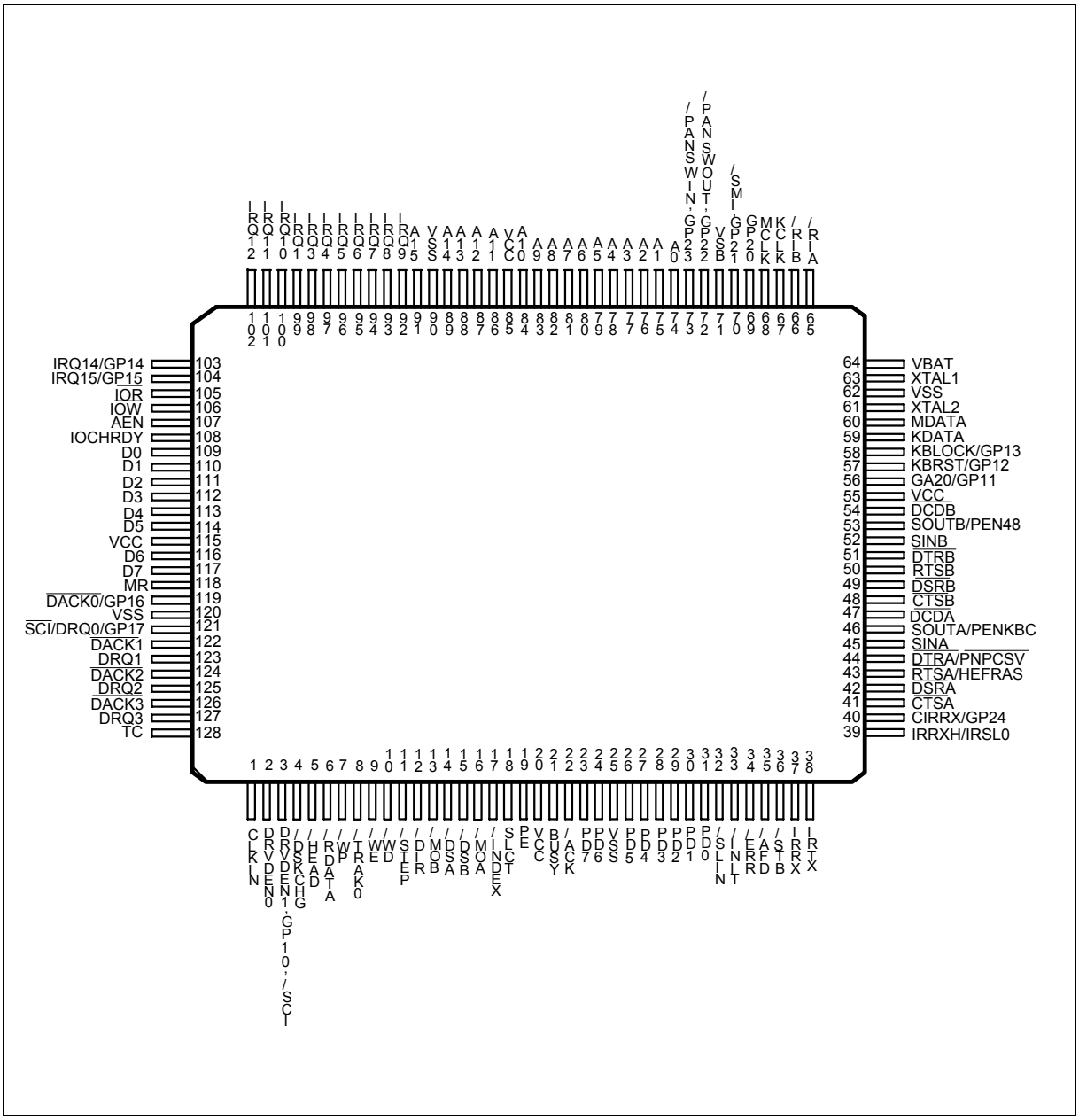
OnNow Funtions

- Keyboard wake-up by programmable keys (patent pending)
- Mouse wake-up by programmable buttons (patent pending)
- CIR wake-up by programmable keys (patent pending)

Package

- 128-pin PQFP

3. PIN CONFIGURATION



4. PIN DESCRIPTION

Note: Please refer to Section 12.2 DC CHARACTERISTICS for details.

I/O_{6t} - TTL level bi-directional pin with 6 mA source-sink capability

I/O_{8t} - TTL level bi-directional pin with 8 mA source-sink capability

I/O_{8} - CMOS level bi-directional pin with 8 mA source-sink capability

I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink capability

I/O_{12} - CMOS level bi-directional pin with 12 mA source-sink capability

I/O_{16u} - CMOS level bi-directional pin with 16 mA source-sink capability with internal pull-up resistor

I/OD_{16u} - CMOS level bi-directional pin open drain output with 16 mA sink capability with internal pull-up resistor

I/O_{24t} - TTL level bi-directional pin with 24 mA source-sink capability

OUT_{8t} - TTL level output pin with 8 mA source-sink capability

OUT_{12t} - TTL level output pin with 12 mA source-sink capability

OD_{12} - Open-drain output pin with 12 mA sink capability

OD_{24} - Open-drain output pin with 24 mA sink capability

IN_{t} - TTL level input pin

IN_{c} - CMOS level input pin

IN_{cu} - CMOS level input pin with internal pull-up resitor

IN_{cs} - CMOS level Schmitt-triggered input pin

IN_{ts} - TTL level Schmitt-triggered input pin

IN_{tsu} - TTL level Schmitt-triggered input pin with internal pull-up resistor

4.1 Host Interface

SYMBOL	PIN	I/O	FUNCTION
A0–A10	74-84	IN_t	System address bus bits 0-10.
A11-A14	86-89	IN_t	System address bus bits 11-14.
A15	91	IN_t	System address bus bit 15.
D0–D5	109-114	I/O_{12t}	System data bus bits 0-5.
D6–D7	116-117	I/O_{12t}	System data bus bits 6-7.
$\overline{IOR}$	105	IN_{ts}	CPU I/O read signal.
$\overline{IOW}$	106	IN_{ts}	CPU I/O write signal.
AEN	107	IN_{ts}	System address bus enable.
IOCHRDY	108	OD24	In EPP Mode, this pin is the IO Channel Ready output to extend the host read/write cycle.
MR	118	INts	Master Reset; Active high; MR is low during normal operations.

Host Interface, continued

SYMBOL	PIN	I/O	FUNCTION
$\overline{DACK0}$	119	IN_{tsu}	DMA Channel 0 Acknowledge signal. (CR2C bit 5_4 = 00, default)
GP16		I/O_{12t}	General purpose I/O port 1bit 6. (CR2C bit 5_4 = 01)
(WDTO)			Alternate function from GP16: Watch dog timer output.
P15		I/O_{12t}	KBC P15 I/O port. (CR2C bit 5_4 = 10)
DRQ0	121	OUT_{12t}	DMA Channel 0 request signal. (CR2C bit 7_6 = 00, default)
GP17		I/O_{12t}	General purpose I/O port 1bit 7. (CR2C bit 7_6 = 01)
(PLEDO)			Alternate Function from GP17: Power LED output.
P14		I/O_{12t}	KBC P14 I/O port. (CR2C bit 7_6 = 10)
$\overline{SCI}$		OD_{12}	System Control Interrupt.(CR2C bit 7_6 = 11)
			In the ACPI power management mode, $\overline{SCI}$ is driven low by the power management events.
$\overline{DACK1}$	122	IN_{ts}	DMA Channel 1 Acknowledge signal.
DRQ1	123	OUT_{12t}	DMA Channel 1 request signal.
$\overline{DACK2}$	124	IN_{ts}	DMA Channel 2 Acknowledge signal.
DRQ2	125	OUT_{12t}	DMA Channel 2 request signal.
$\overline{DACK3}$	126	IN_{ts}	DMA Channel 3 Acknowledge signal.
DRQ3	127	OUT_{12t}	DMA Channel 3 request signal.
TC	128	IN_{ts}	Terminal Count. When active, this pin indicates termination of a DMA transfer.
IRQ1	99	OUT_{12t}	Interrupt request 1. (Logical device 9, CRF1 bit 2 = 0)
IRQ1		I/O_{12t}	General purpose I/O port 3 bit 0.
			(Logical device 9, CRF1 bit 2 = 1)
IRQ3	98	OUT_{12t}	Interrupt request 3. (Logical device 9, CRF1 bit 2 = 0)
GP31		I/O_{12t}	General purpose I/O port 3 bit 1.
			(Logical device 9, CRF1 bit 2 = 1)
IRQ4	97	OUT12t	Interrupt request 4. (Logical device 9, CRF1 bit 2 = 0)
GP32		I/O12t	General purpose I/O port 3 bit 2.
			(Logical device 9, CRF1 bit 2 = 1)
IRQ5	96	OUT12t	Interrupt request 5. (Logical device 9, CRF1 bit 2 = 0)
GP33		I/O12t	General purpose I/O port 3 bit 3.
			(Logical device 9, CRF1 bit 2 = 1)
IRQ6	95	OUT12t	Interrupt request 6. (Logical device 9, CRF1 bit 2 = 0)
GP34		I/O12t	General purpose I/O port 3 bit 4.
			(Logical device 9, CRF1 bit 2 = 1)

Host Interface, continued

SYMBOL	PIN	I/O	FUNCTION
IRQ7 GP35	94	OUT_{12t} I/O_{12t}	Interrupt request 7. (Logical device 9, CRF1 bit 2 = 0) General purpose I/O port 3 bit 5. (Logical device 9, CRF1 bit 2 = 1)
IRQ8 GP36	93	OUT_{12t} I/O_{12t}	Interrupt request 8. (Logical device 9, CRF1 bit 2 = 0) General purpose I/O port 3 bit 6. (Logical device 9, CRF1 bit 2 = 1)
IRQ9 GP37	92	OUT_{12t} I/O_{12t}	Interrupt request 9. (Logical device 9, CRF1 bit 2 = 0) General purpose I/O port 3 bit 7. (Logical device 9, CRF1 bit 2 = 1)
IRQ10 SERIRQ	100	OUT_{12t} I/O_{12t}	Interrupt request 10. (Logical device 9, CRF1 bit 2 = 0) Serial IRQ input/output. (Logical device 9, CRF1 bit 2 = 1)
IRQ11 PCICLK	101	OUT_{12t} IN_t	Interrupt request 11. (Logical device 9, CRF1 bit 2 = 0) PCI clock input. (Logical device 9, CRF1 bit 2 = 1)
IRQ12 GP26	102	OUT_{12t} I/O_{12t}	Interrupt request 12. (Logical device 9, CRF1 bit 2 = 0) General purpose I/O port 2 bit 6. (Logical device 9, CRF1 bit 2 = 1)
IRQ14 GP14 ($\overline{\text{GPACS}}$) (P17) PLEDO	103	OUT_{12t} I/O_{12t} OUT_{12t}	Interrupt request 14. (CR2C bit 1_0 = 00, default) General purpose I/O port 1 bit 4. (CR2C bit 1_0 = 01) Alternate Function 1 from GP14: General purpose address decode output. Alternate Function 2 from GP14: KBC P17 I/O port. Power LED output. (CR2C bit 1_0 = 10)
IRQ15 GP15 ($\overline{\text{GPAWE}}$) (P12) WDT	104	OUT_{12t} I/O_{12t} OUT_{12t}	Interrupt request 15.(CR2C bit 3_2 = 00, default) General purpose I/O port 1 bit 5. (CR2C bit 3_2 = 01) Alternate Function 1 from GP15: General purpose address write enable output. Alternate Function 2 from GP15: KBC P12 I/O port. Watch-Dog timer output. (CR2C bit 3_2 = 10)
CLKIN	1	IN_t	24 or 48 MHz clock input, selectable through CR24 bit 6.

4.2 General Purpose I/O Port

SYMBOL	PIN	I/O	FUNCTION
GP20	69	I/O_{12t}	General purpose I/O port 2 bit 0.
(KBRST)			Alternate Function from GP20: Keyboard reset. (KBC P20)
$\overline{SMI}$	70	OD_{12}	System Management Interrupt. (CR2B bit 4_3 = 00, default)
			In the legacy power management mode, $\overline{SMI}$ is driven low by the power managenment events.
GP21		I/O_{12t}	General purpose I/O port 2 bit 1. (CR2B bit 4_3 = 01)
(P13)			Alternate Function from GP21: KBC P13 I/O port.
P16		I/O_{12t}	KBC P16 I/O port. (CR2B bit 4_3 = 10)
$\overline{PANSWOUT}$	72	OD_{12}	Panel Switch output. (CR2B bit 5 = 0, default)
GP22		I/O_{12t}	General purpose I/O port 2 bit 2. (CR2B bit 5 = 1)
(P14)			Alternate Function from GP22: KBC P14 I/O port.
$\overline{PANSWIN}$	73	IN_{12t}	Panel Switch input. (CR2B bit 7_6 = 00, default)
GP23		I/O_{12t}	General purpose I/O port 2 bit 3. (CR2B bit 7_6 = 01)
(P15)			Alternate Function from GP23: KBC P15 I/O port.
GP24	40	I/O_{12t}	General purpose I/O port 2 bit 4. (CR2A bit 5_4 = 01)
(P16)			Alternate Function from GP24: KBC P16 I/O port.
P13		I/O_{12t}	KBC P13 I/O port. (CR2A bit 5_4 = 10)
CIRRX		IN_t	Consumer IR receiving input. (CR2A bit 5_4 = 00)
GP25	39	I/O_{12}	General purpose I/O port 2 bit 5. (CR2A bit 3_2 = 10)
(GA20)			Alternate Function from GP25: GATE A20. (KBC P21)
IRRXH		IN_t	FIR receiving input. (CR2A bit 3_2 = 00)
IRSL0		OUT_{12t}	IR module select 0. (CR2A bit 3_2 = 01)

4.3 Serial Port Interface

SYMBOL	PIN	I/O	FUNCTION
$\overline{\text{CTSA}}$ $\overline{\text{CTSB}}$	41 48	IN_t	Clear To Send. This is the modem control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
$\overline{\text{DSRA}}$ $\overline{\text{DSRB}}$	42 49	IN_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
$\overline{\text{RTSA}}$ HEFRAS	43	I/O_{8t}	UART A Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. During power-on reset, this pin is pulled down internally and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). A 4.7 kΩ is recommended if intends to pull up. (select 370H as configuration I/O port's address)
$\overline{\text{RTSB}}$	50	I/O_{8t}	UART B Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
$\overline{\text{DTRA}}$ $\overline{\text{PNPCSV}}$	44	I/O_{8t}	UART A Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate. During power-on reset, this pin is pulled down internally and is defined as $\overline{\text{PNPCSV}}$, which provides the power-on value for CR24 bit 0 ($\overline{\text{PNPCSV}}$). A 4.7 kΩ is recommended if intends to pull up. (clear the default value of FDC, UARTs, and PRT)
$\overline{\text{DTRB}}$	51	I/O_{8t}	UART B Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
SINA SINB	45, 52	IN_t	Serial Input. It is used to receive serial data through the communication link.
SOUTA PENKBC	46	I/O_{8t}	UART A Serial Output. It is used to transmit serial data out to the communication link. During power-on reset, this pin is pulled down internally and is defined as PENKBC, which provides the power-on value for CR24 bit 2 (ENKBC). A 4.7 kΩ resistor is recommended if intends to pull up. (enable KBC)
SOUTB PEN48	53	I/O_{8t}	UART B Serial Output. During power-on reset, this pin is pulled down internally and is defined as PEN48, which provides the power-on value for CR24 bit 6 (EN48). A 4.7 kΩ resistor is recommended if intends to pull up.
$\overline{\text{DCDA}}$ $\overline{\text{DCDB}}$	47 54	IN_t	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
$\overline{\text{RIA}}$ $\overline{\text{RIB}}$	65 66	IN_t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.

4.4 Infrared Interface

SYMBOL	PIN	I/O	FUNCTION
IRRX	37	IN_{cs}	Infrared Receiver input.
IRTX	38	OUT_{12t}	Infrared Transmitter Output.

4.5 Multi-Mode Parallel Port

The following pins have alternate functions, which are controlled by CR28 and L3-CRF0.

SYMBOL	PIN	I/O	FUNCTION
SLCT	18	IN_t	PRINTER MODE: SLCT An active high input on this pin indicates that the printer is selected. This pin is pulled high internally. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{WE2}$ This pin is for Extension FDD B; its function is the same as the $\overline{WE}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{WE2}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{WE}$ pin of FDC.
PE	19	IN_t	PRINTER MODE: PE An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{WD2}$ This pin is for Extension FDD B; its function is the same as the $\overline{WD}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{WD2}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{WD}$ pin of FDC.
BUSY	21	INt	PRINTER MODE: BUSY An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
		OD12	EXTENSION FDD MODE: $\overline{MOB2}$ This pin is for Extension FDD B; its function is the same as the $\overline{MOB}$ pin of FDC.
		OD12	EXTENSION 2FDD MODE: $\overline{MOB2}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{MOB}$ pin of FDC.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
$\overline{ACK}$	22	IN_t	PRINTER MODE: $\overline{ACK}$ An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{DSB2}$ This pin is for the Extension FDD B; its functions is the same as the $\overline{DSB}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{DSB2}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{DSB}$ pin of FDC.
$\overline{ERR}$	34	IN_t	PRINTER MODE: $\overline{ERR}$ An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{HEAD2}$ This pin is for Extension FDD B; its function is the same as the $\overline{HEAD}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{HEAD2}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{HEAD}$ pin of FDC.
$\overline{SLIN}$	32	OD12	PRINTER MODE: $\overline{SLIN}$ Output line for detection of printer selection. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD12	EXTENSION FDD MODE: $\overline{STEP2}$ This pin is for Extension FDD B; its function is the same as the $\overline{STEP}$ pin of FDC.
		OD12	EXTENSION 2FDD MODE: $\overline{STEP2}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{STEP}$ pin of FDC.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
$\overline{INIT}$	33	OD_{12}	PRINTER MODE: $\overline{INIT}$ Output line for the printer initialization. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{DIR2}$ This pin is for Extension FDD B; its function is the same as the $\overline{DIR}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{DIR2}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{DIR}$ pin of FDC.
$\overline{AFD}$	35	OD_{12}	PRINTER MODE: $\overline{AFD}$ An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: DRVDEN0 This pin is for Extension FDD B; its function is the same as the DRVDEN0 pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: DRVDEN0 This pin is for Extension FDD A and B; its function is the same as the DRVDEN0 pin of FDC.
$\overline{STB}$	36	OD_{12}	PRINTER MODE: $\overline{STB}$ An active low output is used to latch the parallel data into the printer. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		-	EXTENSION 2FDD MODE: This pin is a tri-state output.
PD0	31	I/O24t	PRINTER MODE: PD0 Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		INt	EXTENSION FDD MODE: $\overline{INDEX2}$ This pin is for Extension FDD B; its function is the same as the $\overline{INDEX}$ pin of FDC. It is pulled high internally.
		INt	EXTENSION 2FDD MODE: $\overline{INDEX2}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{INDEX}$ pin of FDC. It is pulled high internally.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
PD1	30	I/O_{24t}	PRINTER MODE: PD1 Parallel port data bus bit 1. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: $\overline{TRAK02}$ This pin is for Extension FDD B; its function is the same as the $\overline{TRAK0}$ pin of FDC. It is pulled high internally.
		IN_t	EXTENSION. 2FDD MODE: $\overline{TRAK02}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{TRAK0}$ pin of FDC. It is pulled high internally.
PD2	29	I/O_{24t}	PRINTER MODE: PD2 Parallel port data bus bit 2. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: $\overline{WP2}$ This pin is for Extension FDD B; its function is the same as the $\overline{WP}$ pin of FDC. It is pulled high internally.
		IN_t	EXTENSION. 2FDD MODE: $\overline{WP2}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{WP}$ pin of FDC. It is pulled high internally.
PD3	28	I/O_{24t}	PRINTER MODE: PD3 Parallel port data bus bit 3. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: $\overline{RDATA2}$ This pin is for Extension FDD B; its function is the same as the $\overline{RDATA}$ pin of FDC. It is pulled high internally.
		IN_t	EXTENSION 2FDD MODE: $\overline{RDATA2}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{RDATA}$ pin of FDC. It is pulled high internally.
PD4	27	I/O24t	PRINTER MODE: PD4 Parallel port data bus bit 4. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		INt	EXTENSION FDD MODE: $\overline{DSKCHG2}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{DSKCHG}$ pin of FDC. It is pulled high internally.
		INt	EXTENSION 2FDD MODE: $\overline{DSKCHG2}$ This pin is for Extension FDD A and B; this function of this pin is the same as the $\overline{DSKCHG}$ pin of FDC. It is pulled high internally.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
PD5	26	I/O_{24t}	PRINTER MODE: PD5 Parallel port data bus bit 5. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		-	EXTENSION 2FDD MODE: This pin is a tri-state output.
PD6	24	I/O_{24t}	PRINTER MODE: PD6 Parallel port data bus bit 6. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		OD_{24}	EXTENSION. 2FDD MODE: $\overline{MOA2}$ This pin is for Extension FDD A; its function is the same as the $\overline{MOA}$ pin of FDC.
PD7	23	I/O_{24t}	PRINTER MODE: PD7 Parallel port data bus bit 7. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		OD_{24}	EXTENSION 2FDD MODE: $\overline{DSA2}$ This pin is for Extension FDD A; its function is the same as the $\overline{DSA}$ pin of FDC.

4.6 FDC Interface

SYMBOL	PIN	I/O	FUNCTION
DRVDEN0	2	OD_{24}	Drive Density Select bit 0.
DRVDEN1	3	OD_{24}	Drive Density Select bit 1. (CR2A bit 1_0 = 00, default)
GP10		IO_{24t}	General purpose I/O port 1 bit 0. (CR2A bit 1_0 = 01)
(IRQIN1)			Alternate Function from GP10: Interrupt channel input.
P12		IO_{24t}	KBC P12 I/O port. (CR2A bit 1_0 = 10)
$\overline{SCI}$		OD_{12}	System Control Interrupt. (CR2A bit 1_0 = 11) In the ACPI power management mode, $\overline{SCI}$ is driven low by the power management events.
$\overline{HEAD}$	5	OD_{24}	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
$\overline{WE}$	9	OD_{24}	Write enable. An open drain output.
$\overline{WD}$	10	OD_{24}	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.

FDC Interface, continued

SYMBOL	PIN	I/O	FUNCTION
$\overline{STEP}$	11	OD_{24}	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
$\overline{DIR}$	12	OD_{24}	Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
$\overline{MOB}$	13	OD_{24}	Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output.
$\overline{DSA}$	14	OD_{24}	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
$\overline{DSB}$	15	OD_{24}	Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output.
$\overline{MOA}$	16	OD_{24}	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
$\overline{DSKCHG}$	4	IN_{cs}	Diskette change. This signal is active low at power on and whenever the diskette is removed. This input pin is pulled up internally by a 1 K . resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
$\overline{RDATA}$	6	INcs	The read data input signal from the FDD. This input pin is pulled up internally by a 1 K resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
$\overline{WP}$	7	IN_{cs}	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin is pulled up internally by a 1 K resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
$\overline{TRAK0}$	8	IN_{cs}	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track. This input pin is pulled up internally by a 1 K resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
$\overline{INDEX}$	17	IN_{cs}	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin is pulled up internally by a 1 K resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).

4.7 KBC Interface

SYMBOL	PIN	I/O	FUNCTION
KDATA	59	I/O_{16u}	Keyboard Data.
MDATA	60	I/O_{16u}	PS2 Mouse Data.
KCLK	67	I/O_{16u}	Keyboard Clock.
MCLK	68	I/O_{16u}	PS2 Mouse Clock.
GA20 GP11 (IRQIN2)	56	I/O_{12t} I/O_{12t}	KBC GATE A20 (P21) Output. (CR2A bit 6 = 0, default) General purpose I/O port 1 bit 1. (CR2A bit 6 = 1) Alternate Function from GP11: Interrupt channel input.
KBRST GP12 (WDTO)	57	I/O_{12t} I/O_{12t}	W83C45 Keyboard Reset (P20) Output. (CR2A bit 7 = 0, default) General purpose I/O port 1 bit 2. (CR2A bit 7 = 1) Alternate Function 1 from GP12: Watchdog timer output.
KBLOCK GP13	58	IN_{ts} I/O_{16t}	W83C45 KINH (P17) Input. (CR2B bit 0 = 0, default) General purpose I/O port 1 bit 3. (CR2B bit 0 = 1)

4.8 POWER PINS

SYMBOL	PIN	FUNCTION
VCC	20, 55, 85, 115	+5V power supply for the digital circuitry.
VSB	71	+5V stand-by power supply for the digital circuitry.
GND	25, 62, 90, 120	Ground.

4.9 ACPI Interface

SYMBOL	PIN	I/O	FUNCTION
VBAT	64	NA	Battery voltage input.
XTAL1	63	IN_C	32.768Khz Clock Input.
XTAL2	61	O_{8t}	32.768Khz Clock Output.