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NUVOTON

ISA I/O

W83977EF-AW

W83977EG-AW

Publication Release Date: January, 2010
Revision 1.5

TABLES OF CONTENTS

1. GENERAL DESCRIPTION

W83977EF-AW/EG-AW is an evolving product from Winbond's most popular I/O chip W83877F --- which integrates the disk drive adapter, serial port (UART), IrDA 1.0 SIR, parallel port, configurable plug-and-play registers for the whole chip --- plus additional powerful features: **ACPI**, 8042 keyboard controller with PS/2 mouse support, 14 general purpose I/O ports, full 16-bit address decoding, OnNow keyboard Wake-Up, OnNow mouse Wake-Up.

The disk drive adapter functions of **W83977EF-AW/EG-AW** include a floppy disk drive controller compatible with the industry standard 82077/ 765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. The wide range of functions integrated onto the W83977EF-AW greatly reduces the number of components required for interfacing with floppy disk drives. The **W83977EF-AW/EG-AW** supports four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s,1 Mb/s, and 2 Mb/s.

W83977EF-AW/EG-AW provides two high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. Both UARTs provide legacy speed with baud rate up to 115.2k bps and also advanced speed with baud rates of **230k**, **460k**, or **921k bps** which support higher speed modems.

W83977EF-AW/EG-AW supports one PC-compatible printer port (SPP), Bi-directional Printer port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). Through the printer port interface pins, also available are: Extension FDD Mode and Extension 2FDD Mode allowing one or two external floppy disk drives to be connected.

The configuration registers support mode selection, function enable/disable, and power down function selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature demand of Windows 95™, which makes system resource allocation more efficient than ever.

W83977EF-AW/EG-AW provides functions that complies with **ACPI** (*Advanced Configuration and Power Interface*), which includes support of legacy and ACPI power management through $\overline{\text{SMI}}$ or $\overline{\text{SCI}}$ function pins. **W83977EF-AW/EG-AW** also has auto power management to reduce power consumption.

The keyboard controller is based on 8042 compatible instruction set with a 2K Byte programmable ROM and a 256-Byte RAM bank. Keyboard BIOS firmware are available with optional AMIKEY™-2, Phoenix MultiKey/42™, or customer code.

W83977EF-AW/EG-AW provides a set of flexible I/O control functions to the system designer through a set of General Purpose I/O ports. These GPIO ports may serve as simple I/O or may be individually configured to provide a predefined alternate function.

W83977EF-AW/EG-AW *also supports Power-loss control, and makes the system never miss to detect any Wake-Up event provided by the chipset such as INTEL PIIX4™.*

W83977EF-AW/EG-AW is made to fully comply with **Microsoft PC98 Hardware Design Guide**. IRQs, DMAs, and I/O space resource are flexible to adjust to meet ISA PnP requirement. Moreover **W83977EF-AW/EG-AW** is made to meet the specification of PC98's requirement in the power management: **ACPI** and **DPM** (Device Power Management).

Another benifit is that **W83977EF-AW/EG-AW** is of the same pin assignment of W83977AF, W83977F, W83977TF, W83977ATF. Thus makes the design very flexible.

2. FEATURES

General

- Plug & Play 1.0A compatible
- Support 12 IRQs, 4 DMA channels, full 16-bit address decoding
- Capable of ISA Bus IRQ Sharing
- Compliant with **Microsoft PC98** Hardware Design Guide
- Support **DPM** (Device Power Management), **ACPI**
- Report ACPI status interrupt by SCI# signal issued from any of the 12 IQRs pins or GPIO xx
- Programmable configuration settings
- single 24/48 Mhz clock input

FDC

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- Support vertical recording format
- DMA enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detects all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD write enable signal (write data signal was forced to be inactive)
- Support up to four 3.5-inch or 5.25-inch floppy disk drives
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support **3-mode FDD, and its Win95 driver**

UART

- Two high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs
- MIDI compatible
- Fully programmable serial-interface characteristics:
  --- 5, 6, 7 or 8-bit characters
  --- Even, odd or no parity bit generation/detection
  --- 1, 1.5 or 2 stop bits generation

- Internal diagnostic capabilities:
  --- Loop-back controls for communications link fault isolation
  --- Break, parity, overrun, framing error simulation
- Programmable baud generator allows division of 1.8461 Mhz and 24 Mhz by 1 to (2^{16}-1)
- Maximum baud rate up to **921k bps** for 14.769 Mhz and 1.5M bps for 24 Mhz

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps

Parallel Port

- Compatible with IBM parallel port
- Support PS/2 compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- Extension FDD mode supports disk drive B; and Extension 2FDD mode supports disk drives A and B through parallel port
- Enhanced printer port back-drive current protection

Keyboard Controller

- 8042 based with optional F/W from AMIKKEY™-2, Phoenix MultiKey/42™ or customer code
- With 2K bytes of programmable ROM, and 256 bytes of RAM
- Asynchronous Access to Two Data Registers and One status Register
- Software compatibility with the 8042 and PC87911 microcontrollers
- Support PS/2 mouse
- Support port 92
- Support both interrupt and polling modes
- **Fast Gate A20 and Hardware Keyboard Reset**
- 8 Bit Timer/ Counter
- Support binary and BCD arithmetic
- 6MHz, 8 MHz, 12 MHz, or 16 MHz operating frequency

General Purpose I/O Ports

- 14 programmable general purpose I/O ports; 6 dedicate, 8 optional
- General purpose I/O ports can serve as simple I/O ports, interrupt steering inputs, watching dog timer output, power LED output, infrared I/O pins, general purpose address decoder, KBC control I/O pins

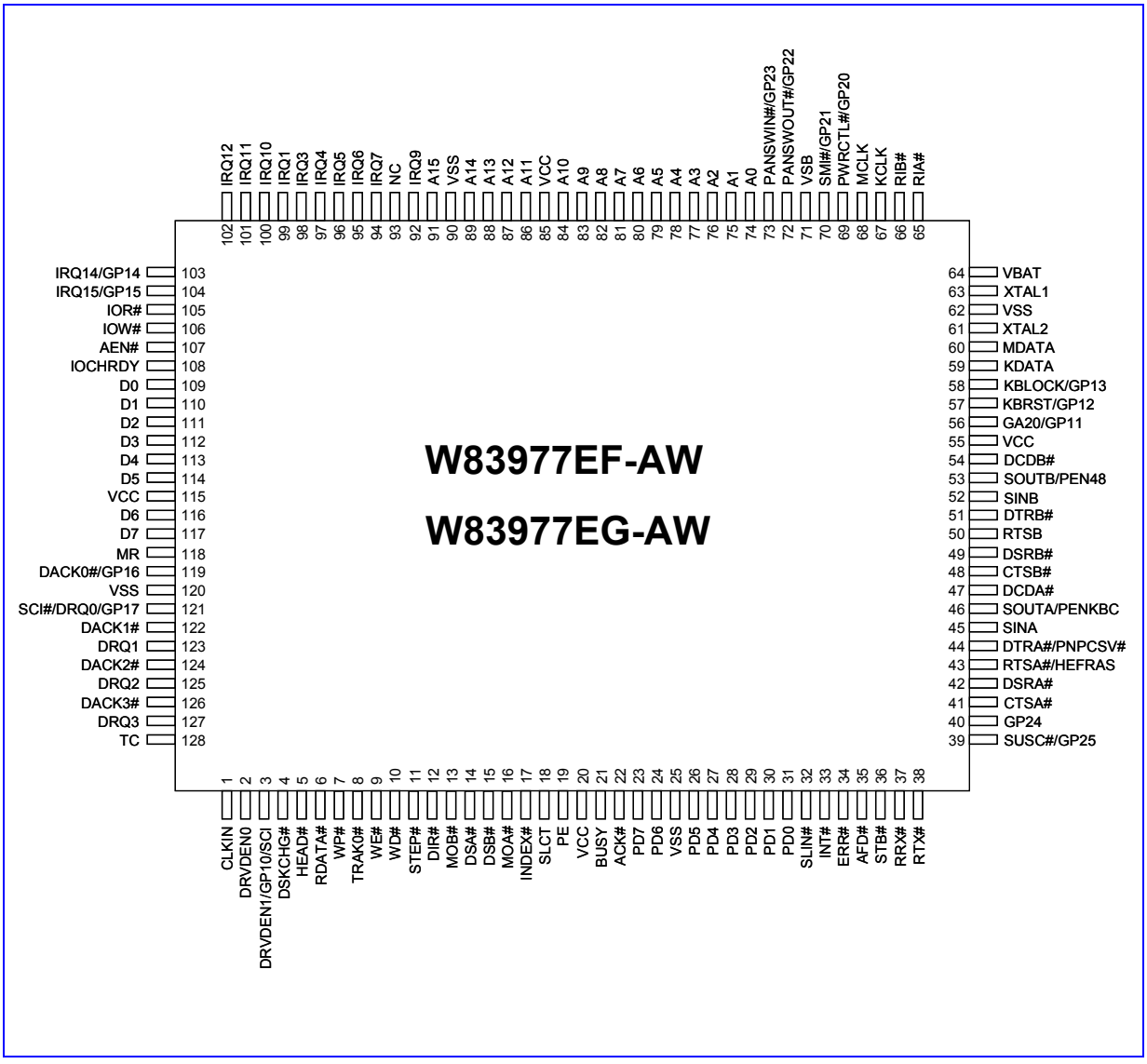
OnNow Funtions

- Keyboard Wake-Up by programmable keys
- Mouse Wake-Up by programmable buttons

Package

- 128-pin PQFP

3. PIN CONFIGURATION



4. PIN DESCRIPTION

Note: Please refer to Section 11.2 DC CHARACTERISTICS for details.

I/O_{6t} - TTL level bi-directional pin with 6 mA source-sink capability

I/O_{8t} - TTL level bi-directional pin with 8 mA source-sink capability

I/O_{8} - CMOS level bi-directional pin with 8 mA source-sink capability

I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink capability

I/O_{12} - CMOS level bi-directional pin with 12 mA source-sink capability

I/O_{16u} - CMOS level bi-directional pin with 16 mA source-sink capability with internal pull-up resistor

I/OD_{16u} - CMOS level bi-directional pin open drain output with 16 mA sink capability with internal pull-up resistor

I/O_{24t} - TTL level bi-directional pin with 24 mA source-sink capability

OUT_{8t} - TTL level output pin with 8 mA source-sink capability

OUT_{12t} - TTL level output pin with 12 mA source-sink capability

OD_{12} - Open-drain output pin with 12 mA sink capability

OD_{24} - Open-drain output pin with 24 mA sink capability

IN_{t} - TTL level input pin

IN_{C} - CMOS level input pin

IN_{cu} - CMOS level input pin with internal pull-up resitor

IN_{cs} - CMOS level Schmitt-triggered input pin

IN_{ts} - TTL level Schmitt-triggered input pin

IN_{tsu} - TTL level Schmitt-triggered input pin with internal pull-up resistor

4.1 Host Interface

SYMBOL	PIN	I/O	FUNCTION
A0–A10	74-84	IN_t	System address bus bits 0-10
A11-A14	86-89	IN_t	System address bus bits 11-14
A15	91	IN_t	System address bus bit 15
D0–D5	109-114	I/O_{12t}	System data bus bits 0-5
D6–D7	116-117	I/O_{12t}	System data bus bits 6-7
IOR#	105	IN_{ts}	CPU I/O read signal
IOW#	106	IN_{ts}	CPU I/O write signal
AEN#	107	IN_{ts}	System address bus enable
IOCHRDY	108	OD_{24}	In EPP Mode, this pin is the IO Channel Ready output to extend the host read/write cycle.
MR	118	IN_{ts}	Master Reset; Active high; MR is low during normal operations.

1.1 Host Interface, continued

SYMBOL	PIN	I/O	FUNCTION
DACK0#	119	IN_{tsu}	DMA Channel 0 Acknowledge signal. (CR2C bit 5_4 = 00, default)
GP16		I/O_{12t}	General purpose I/O port 1bit 6. (CR2C bit 5_4 = 01)
(WDTO)			Alternate function from GP16: Watch dog timer output
P15		I/O_{12t}	KBC P15 I/O port. (CR2C bit 5_4 = 10)
DRQ0	121	OUT_{12t}	DMA Channel 0 request signal. (CR2C bit 7_6 = 00, default)
GP17		I/O_{12t}	General purpose I/O port 1bit 7. (CR2C bit 7_6 = 01)
(PLEDO)			Alternate Function from GP17: Power LED output.
P14		I/O_{12t}	KBC P14 I/O port (CR2C bit 7_6 = 10)
SCI#		OUT_{12t}	System Control Interrupt (CR2C bit 7_6 = 11)
DACK1#	122	IN_{ts}	DMA Channel 1 Acknowledge signal
DRQ1	123	OUT_{12t}	DMA Channel 1 request signal
DACK2#	124	IN_{ts}	DMA Channel 2 Acknowledge signal
DRQ2	125	OUT_{12t}	DMA Channel 2 request signal
DACK3#	126	IN_{ts}	DMA Channel 3 Acknowledge signal
DRQ3	127	OUT_{12t}	DMA Channel 3 request signal
TC	128	IN_{ts}	Terminal Count. When active, this pin indicates termination of a DMA transfer.
IRQ1	99	OUT_{12t}	Interrupt request 1
IRQ3	98	OUT_{12t}	Interrupt request 3
IRQ4	97	OUT_{12t}	Interrupt request 4
IRQ5	96	OUT_{12t}	Interrupt request 5
IRQ6	95	OUT_{12t}	Interrupt request 6
IRQ7	94	OUT_{12t}	Interrupt request 7
IRQ9	92	OUT_{12t}	Interrupt request 9
IRQ10	100	OUT_{12t}	Interrupt request 10
IRQ11	101	OUT_{12t}	Interrupt request 11
IRQ12	102	OUT_{12t}	Interrupt request 12

1.1 Host Interface, continued

SYMBOL	PIN	I/O	FUNCTION
IRQ14	103	OUT_{12t}	Interrupt request 14. (CR2C bit 1_0 = 00, default)
GP14		I/O_{12t}	General purpose I/O port 1 bit 4. (CR2C bit 1_0 = 01)
(GPACS1#)			Alternate Function 1 from GP14: General purpose address decode output.
(P17)			Alternate Function 2 from GP14: KBC P17 I/O port.
PLEDO		OUT_{12t}	Power LED output. (CR2C bit 1_0 = 10)
IRQ15	104	OUT_{12t}	Interrupt request 15.(CR2C bit 3_2 = 00, default)
GP15		I/O_{12t}	General purpose I/O port 1 bit 5. (CR2C bit 3_2 = 01)
(GPACS2#)			Alternate Function 1 from GP15: General purpose address write enable output.
(P12)			Alternate Function 2 from GP15: KBC P12 I/O port.
WDT		OUT_{12t}	Watch-Dog timer output. (CR2C bit 3_2 = 10)
CLKIN	1	IN_t	24 or 48 MHz clock input, selectable through bit 5 of CR24.

4.2 General Purpose I/O Port

SYMBOL	PIN	I/O	FUNCTION
PWR_CTL#	69	OD_{16u}	Power supply control
GP20		I/O_{16tu}	General purpose I/O port 2 bit 0.
(KBRST)			Alternate Function from GP20: Keyboard reset (KBC P20)
SMI #	70	OD_{12t}	For the power management, the $\overline{SMI}$ is active low by the power management events, that generate and $\overline{SCI}$ in ACPI mode. (CR2B bit 4_3 = 00, default)
GP21		I/O_{12t}	General purpose I/O port 2 bit 1. (CR2B bit 4_3 = 01)
(P13)			Alternate Function from GP21: KBC P13 I/O port.
P16		I/O_{12t}	KBC P16 I/O port. (CR2B bit 4_3 = 10)
PANSWOUT#	72	OD_{12t}	Panel Switch output. (CR2B bit 5 = 0, default)
GP22		I/O_{12t}	General purpose I/O port 2 bit 2. (CR2B bit 5 = 1)
(P14)			Alternate Function from GP22: KBC P14 I/O port.

1.2 General Purpose I/O Port ,continued

SYMBOL	PIN	I/O	FUNCTION
PANSWIN# GP23 (P15)	73	IN_t I/O_{12t}	Panel Switch input. (CR2B bit 7_6 = 00, default) General purpose I/O port 2 bit 3. (CR2B bit 7_6 = 01) Alternate Function from GP23: KBC P15 I/O port
SUSC# (GA20) GP25	39	IN_{ts} I/O_{12}	Suspend C input Alternate Function from GP25: GATE A20 (KBC P21) General purpose I/O port 2 bit 5.
GP24	40	I/O_{12}	General purpose I/O port 2 bit 4.

4.3 Serial Port Interface

SYMBOL	PIN	I/O	FUNCTION
CTSA# CTSB#	41 48	IN_t	Clear To Send is the modem control input. The function of these pins can be tested by reading Bit 4 of the handshake status register.
DSRA# DSRB#	42 49	IN_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
RTSA# HEFRAS	43	I/O_{8t}	UART A Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. During power-on reset, this pin is pulled down internally and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). A 4.7 kΩ is recommended if intends to pull up. (select 370H as configuration I/O port's address)
RTSB#	50	I/O_{8t}	UART B Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.

1.3 Serial Port Interface, continued

SYMBOL	PIN	I/O	FUNCTION
DTRA# PNPCSV#	44	I/O_{8t}	UART A Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate. During power-on reset, this pin is pulled down internally and is defined as PNPCSV#, which provides the power-on value for CR24 bit 0 (PNPCSV#). A 4.7 kΩ is recommended if intends to pull up. (clear the default value of FDC, UARTs, and PRT)
DTRB#	51	I/O_{8t}	UART B Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
SINA SINB	45, 52	IN_t	Serial Input. Used to receive serial data through the communication link.
SOUTA PENKBC	46	I/O_{8t}	UART A Serial Output. Used to transmit serial data out to the communication link. During power-on reset, this pin is pulled down internally and is defined as PENKBC, which provides the power-on value for CR24 bit 2 (ENKBC). A 4.7 kΩ resistor is recommended if intends to pull up. (enable KBC)
SOUTB PEN48	53	I/O_{8t}	UART B Serial Output. During power-on reset, this pin is pulled down internally and is defined as PEN48, which provides the power-on value for CR24 bit 6 (EN48). A 4.7 kΩ resistor is recommended if intends to pull up.
DCDA# DCDB#	47 54	IN_t	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
RIA# RIB#	65 66	IN_t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.

4.4 Infrared Interface

SYMBOL	PIN	I/O	FUNCTION
IRRX	37	IN_{cs}	Infrared Receiver input.
IRTX	38	OUT_{12t}	Infrared Transmitter Output.

4.5 Multi-Mode Parallel Port

The following pins have alternate functions, which are controlled by CR28 and L3-CRF0.

SYMBOL	PIN	I/O	FUNCTION
SLCT	18	IN_t	PRINTER MODE: SLCT An active high input on this pin indicates that the printer is selected. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: WE2# This pin is for Extension FDD B; its function is the same as the WE# pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: WE2# This pin is for Extension FDD A and B; it function is the same as the WE# pin of FDC.
PE	19	IN_t	PRINTER MODE: PE An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: WD2# This pin is for Extension FDD B; its function is the same as the WD# pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: WD2# This pin is for Extension FDD A and B; its function is the same as the WD# pin of FDC.

1.5 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
BUSY	21	IN_t	PRINTER MODE: BUSY An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: MOB2# This pin is for Extension FDD B; the function of this pin is the same as the MOB# pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE:MOB2# This pin is for Extension FDD A and B; the function of this pin is the same as the MOB# pin of FDC.
ACK#	22	IN_t	PRINTER MODE: ACK# An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: DSB2# This pin is for the Extension FDD B; its functions is the same as the DSB# pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: DSB2# This pin is for Extension FDD A and B; it functions is the same as the DSB# pin of FDC.
ERR#	34	IN_t	PRINTER MODE: ERR# An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: HEAD2# This pin is for Extension FDD B; its function is the same as the HEAD#pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: HEAD2# This pin is for Extension FDD A and B; its function is the same as the HEAD# pin of FDC.

1.5 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
SLIN#	32	OD_{12}	PRINTER MODE: SLIN# Output line for detection of printer selection. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE:STEP2# This pin is for Extension FDD B; its function is the same as the STEP# pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: STEP2# This pin is for Extension FDD A and B; its function is the same as the STEP# pin of FDC.
INIT#	33	OD_{12}	PRINTER MODE: INIT# Output line for the printer initialization. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: DIR2# This pin is for Extension FDD B; its function is the same as the DIR# pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: DIR2# This pin is for Extension FDD A and B; its function is the same as the DIR# pin of FDC.
AFD#	35	OD_{12}	PRINTER MODE: AFD# An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: DRVDEN0 This pin is for Extension FDD B; its function is the same as the DRVDEN0 pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: DRVDEN0 This pin is for Extension FDD A and B; its function is the same as the DRVDEN0 pin of FDC.

1.5 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
STB#	36	OD_{12}	PRINTER MODE: STB# An active low output is used to latch the parallel data into the printer. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		-	EXTENSION 2FDD MODE: This pin is a tri-state output.
PD0	31	I/O_{24t}	PRINTER MODE: PD0 Parallel port data bus bit 0. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: INDEX2# This pin is for Extension FDD B; the function of this pin is the same as the INDEX# pin of FDC. It is pulled high internally.
		IN_t	EXTENSION 2FDD MODE: INDEX2# This pin is for Extension FDD A and B; the function of this pin is the same as the INDEX# pin of FDC. It is pulled high internally.
PD1	30	I/O_{24t}	PRINTER MODE: PD1 Parallel port data bus bit 1. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: TRAK02# This pin is for Extension FDD B; the function of this pin is the same as the TRAK0# pin of FDC. It is pulled high internally.
		IN_t	EXTENSION. 2FDD MODE: TRAK02# This pin is for Extension FDD A and B; the function of this pin is the same as the TRAK0# pin of FDC. It is pulled high internally.
PD2	29	I/O_{24t}	PRINTER MODE: PD2 Parallel port data bus bit 2. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: WP2# This pin is for Extension FDD B; the function of this pin is the same as the WP# pin of FDC. It is pulled high internally.
		IN_t	EXTENSION. 2FDD MODE: WP2# This pin is for Extension FDD A and B; the function of this pin is the same as the WP# pin of FDC. It is pulled high internally.

1.5 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
PD3	28	I/O_{24t}	PRINTER MODE: PD3 Parallel port data bus bit 3. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: RDATA2# This pin is for Extension FDD B; the function of this pin is the same as the RDATA# pin of FDC. It is pulled high internally.
		IN_t	EXTENSION 2FDD MODE: RDATA2# This pin is for Extension FDD A and B; this function of this pin is the same as the RDATA# pin of FDC. It is pulled high internally.
PD4	27	I/O_{24t}	PRINTER MODE: PD4 Parallel port data bus bit 4. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: DSKCHG2# This pin is for Extension FDD B; the function of this pin is the same as the DSKCHG# pin of FDC. It is pulled high internally.
		IN_t	EXTENSION 2FDD MODE: DSKCHG2# This pin is for Extension FDD A and B; this function of this pin is the same as the DSKCHG# pin of FDC. It is pulled high internally.
PD5	26	I/O_{24t}	PRINTER MODE: PD5 Parallel port data bus bit 5. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		-	EXTENSION 2FDD MODE: This pin is a tri-state output.
PD6	24	I/O_{24t}	PRINTER MODE: PD6 Parallel port data bus bit 6. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		OD_{24}	EXTENSION. 2FDD MODE: MOA2# This pin is for Extension FDD A; its function is the same as the MOA# pin of FDC.

1.5 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
PD7	23	I/O_{24t}	PRINTER MODE: PD7 Parallel port data bus bit 7. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		OD_{24}	EXTENSION 2FDD MODE: DSA2# This pin is for Extension FDD A; its function is the same as the DSA# pin of FDC.

4.6 FDC Interface

SYMBOL	PIN	I/O	FUNCTION
DRVDEN0	2	OD_{24}	Drive Density Select bit 0.
DRVDEN1	3	OD_{24}	Drive Density Select bit 1. (CR2A bit 1_0 = 00, default)
GP10		IO_{24t}	General purpose I/O port 1 bit 0. (CR2A bit 1_0 = 01)
(IRQIN1)			Alternate Function from GP10: Interrupt channel input.
P12		IO_{24t}	KBC P12 I/O port. (CR2A bit 1_0 = 10)
SCI#		OUT_{12t}	System Control Interrupt (CR2A bit 1_0 = 11)
HEAD#	5	OD_{24}	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
WE#	9	OD_{24}	Write enable. An open drain output.
WD#	10	OD_{24}	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
STEP#	11	OD_{24}	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
DIR#	12	OD_{24}	Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
MOB#	13	OD_{24}	Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output.

1.6 FDC Interface, continued

SYMBOL	PIN	I/O	FUNCTION
DSA#	14	OD_{24}	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
DSB#	15	OD_{24}	Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output.
MOA#	16	OD_{24}	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
DSKCHG#	4	IN_{cs}	Diskette change. This signal is active low at power on and whenever the diskette is removed. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
RDATA#	6	IN_{cs}	The read data input signal from the FDD. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
WP#	7	IN_{cs}	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
TRAK0#	8	IN_{cs}	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
INDEX#	17	IN_{cs}	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).

4.7 KBC Interface

SYMBOL	PIN	I/O	FUNCTION
KDATA	59	I/O_{16u}	Keyboard Data
MDATA	60	I/O_{16u}	PS2 Mouse Data
KCLK	67	I/O_{16u}	Keyboard Clock
MCLK	68	I/O_{16u}	PS2 Mouse Clock
GA20 GP11 (IRQIN2)	56	I/O_{12t} I/O_{12t}	KBC GATE A20 (P21) Output. (CR2A bit 6 = 0, default) General purpose I/O port 1 bit 1. (CR2A bit 6 = 1) Alternate Function from GP11: Interrupt channel input.
KBRST GP12 (WDTO)	57	I/O_{12t} I/O_{12t}	W83C45 Keyboard Reset (P20) Output. (CR2A bit 7 = 0, default) General purpose I/O port 1 bit 2. (CR2A bit 7 = 1) Alternate Function 1 from GP12 : Watchdog timer output.
KBLOCK GP13	58	IN_{ts} I/O_{16t}	W83C45 KINH (P17) Input. (CR2B bit 0 = 0, default) General purpose I/O port 1 bit 3. (CR2B bit 0 = 1)

4.8 POWER PINS

SYMBOL	PIN	FUNCTION
VCC	20, 55, 85, 115	+5V power supply for the digital circuitry
VSB	71	+5V stand-by power supply for the digital circuitry
GND	25, 62, 90, 120	Ground

4.9 ACPI Interface

SYMBOL	PIN	I/O	FUNCTION
VBAT	64	NA	battery voltage input
XTAL1	63	IN_C	32.768Khz Clock Input
XTAL2	61	O_{8t}	32.768Khz Clock Output

5. FDC FUNCTIONAL DESCRIPTION

5.1 W83977EF-AW/EG FDC

The floppy disk controller of W83977EF-AW/EG integrates all of the logic required for floppy disk control. The FDC implements a PC/AT or PS/2 solution. All programmable options default to compatible values. The FIFO provides better system performance in multi-master systems. The digital data separator supports up to 2 M bits/sec data rate.

The FDC includes the following blocks: AT interface, Precompensation, Data Rate Selection, Digital Data Separator, FIFO, and FDC Core.

5.1.1 AT interface

The interface consists of the standard asynchronous signals:RD#, WR#, A0-A3, IRQ, DMA control, and a data bus. The address lines select between the configuration registers, the FIFO and control/status registers. This interface can be switched between PC/AT, Model 30, or PS/2 normal modes. The PS/2 register sets are a superset of the registers found in a PC/AT.

5.1.2 FIFO (Data)

The FIFO is 16 bytes in size and has programmable threshold values. All command parameter information and disk data transfers go through the FIFO. Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The FIFO defaults to disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the CONFIGURE command. The advantage of the FIFO is that it allows the system a larger DMA latency without causing disk errors. The following tables give several examples of the delays with a FIFO. The data are based upon the following formula:

THRESHOLD # $\times$ (1/DATA/RATE) *8 - 1.5 μS = DELAY

FIFO THRESHOLD	MAXIMUM DELAY TO SERVICING AT 500K BPS
	Data Rate
1 Byte	1 $\times$ 16 μS - 1.5 μS = 14.5 μS
2 Byte	2 $\times$ 16 μS - 1.5 μS = 30.5 μS
8 Byte	8 $\times$ 16 μS - 1.5 μS = 6.5 μS
15 Byte	15 $\times$ 16 μS - 1.5 μS = 238.5 μS
FIFO THRESHOLD	**MAXIMUM DELAY TO SERVICING AT 1M BPS**
	Data Rate
1 Byte	1 $\times$ 8 μS - 1.5 μS = 6.5 μS
2 Byte	2 $\times$ 8 μS - 1.5 μS = 14.5 μS
8 Byte	8 $\times$ 8 μS - 1.5 μS = 62.5 μS
15 Byte	15 $\times$ 8 μS - 1.5 μS = 118.5 μS