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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
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WINBOND I/O
W83977F-A/W83977G-A
&
W83977AF-A/W83977AG-A

W83977F/ AF Data Sheet Revision History

	PAGES	DATES	VERSION	VERSION ON WEB	MAIN CONTENTS
1	n.a.	01/20/97	0.50		First publication
2	2,3,6,8,9,10, 122,126,128-132,134,138,168	01/27/97	0.51		Spec. Correction; typo correction
3	117-125,127	01/30/97	0.52		Register Correction; pages rearranging.
4	9,10,120-122	02/13/97	0.53		Spec. Correction; typo correction
5	127,135,136,169	03/03/97	0.54		Spec. Correction; typo correction
6	VIII,IX,166-169	05/24/97	0.55		Add section 15.0; pages rearranging.
7	P118	7/15/97	0.56		CR24: Pin 22→Pin1
8	53,54,58,61,62, 63,65,124,125	11/17/97	0.57		Register Correction
9	1,3,11,52,91,105, 109,110,111,113, 114,115,119,124, 130,131,148	03/10/98	0.58		Typo correction and data calibrated
10	n.a.	05/02/06	0.6		Add lead-free package version

Table of Contents-

1. GENERAL DESCRIPTION

This data sheet covers two products: W83977F/G, and W83977AF/AG whose pin assignment, and most of the functions are the same. W83977AF/AG is an advanced version of W83977F/G featuring the FIR function.

W83977F/G, W83977AF/AG are evolving products from Winbond's most popular I/O chip W83877F ---- which integrates the disk drive adapter, serial port (UART), IrDA 1.0 SIR, parallel port, configurable plug-and-play registers in one chip --- plus additional powerful features: **ACPI**, 8042 keyboard controller with PS/2 mouse support, Real Time Clock, 14 general purpose I/O ports, full 16-bit address decoding, TV remote IR (Consumer IR, supporting NEC, RC-5, extended RC-5, and RECS-80 protocols). In addition, W83977AF/AG provides the functions of **IrDA 1.1** (MIR for 1.152M bps or FIR for 4M bps).

The disk drive adapter functions of W83977F/G, W83977AF/AG include a floppy disk drive controller compatible with the industry standard 82077/ 765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt/ DMA logic. The wide range of functions integrated onto the W83977F/G, W83977AF/AG greatly reduces the number of components required for interfacing with floppy disk drives. The W83977F/G, W83977AF/AG supports up to four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s,1 Mb/s, and 2 Mb/s.

The W83977F/G, W83977AF/AG provide two high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. Both UARTs provide legacy speed with baud rate 115.2k and provide advanced speed with baud rate **230k**, **460k**, and **921k bps** which support higher speed modems. W83977AF/AG alone provides independent **3rd UART** (32-byte FIFO) dedicated for IR function.

The W83977F/G, W83977AF/AG supports one PC-compatible printer port (SPP), Bi-directional Printer port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). Through the printer port interface pins, also available are: Extension FDD Mode and Extension 2FDD Mode allowing one or two external floppy disk drives to be connected.

The configuration registers support mode selection, function enable/disable, and power down function selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature demand of Windows 95™, which makes system resource allocation more efficient than ever.

W83977F/G, W83977AF/AG provides functions that comply with **ACPI** (*Advanced Configuration and Power Interface*), which includes support of legacy and ACPI power management through SMI or SCI function pins. W83977F/G, W83977AF/AG also has auto power management to reduce power consumption.

The keyboard controller is based on 8042 compatible instruction set with a 2K Byte programmable ROM and a 256-Byte RAM bank. Keyboard BIOS firmware is available with optional AMIKEY™ -2, Phoenix MultiKey/42™, or customer code.

The W83977F/G, W83977AF/AG provides a set of flexible I/O control functions to the system designer through a set of General Purpose I/O ports. These GPIO ports may serve as simple I/O or may be individually configured to provide a pre-defined alternate function.

W83977F/G, W83977AF/AG is made to fully comply with **Microsoft™ PC97 Hardware Design Guide**. IRQs, DMAs, and I/O space resource are flexible to adjust to meet ISA PnP requirement. Full 16-bit address decoding is also provided. Moreover W83977F/G, W83977AF/AG is made to meet the specification of PC97's requirement in the power management: **ACPI** and **DPM** (Device Power Management).

2. FEATURES

General

- Plug & Play 1.0A Compliant
- Support 13 IRQs, 4 DMA channels, full 16-bit addresses decoding
- Capable of ISA Bus IRQ Sharing
- Compliant with Microsoft PC97 Hardware Design Guide
- Support DPM (Device Power Management), ACPI
- Programmable configuration settings
- 24 or 14.318 Mhz clock input

FDC

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- Support vertical recording format
- DMA enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detects all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD write enable signal (write data signal was forced to be inactive)
- Support up to four 3.5-inch or 5.25-inch floppy disk drives
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support **3-mode FDD, and its Win95 driver**

UART

- Two high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs
- 3rd UART with 32-byte send/receive FIFO is supported for IR function [W83977AF/AG only]
- MIDI compatible
- Fully programmable serial-interface characteristics:
  - --- 5, 6, 7 or 8-bit characters
  - --- Even, odd or no parity bit generation/detection
  - --- 1, 1.5 or 2 stop bits generation
- Internal diagnostic capabilities:
  - --- Loop-back controls for communications link fault isolation
  - --- Break, parity, overrun, framing error simulation
- Programmable baud generator allows division of 1.8461 Mhz and 24 Mhz by 1 to (216-1)
- Maximum baud rate up to **921k bps** for 14.769 Mhz and 1.5M bps for 24 Mhz

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps
- Support IrDA version 1.1 MIR (1.152M bps) and FIR (4M bps) protocol *[W83977AF/AG only]*

--- Single DMA channel for transmitter or receiver

--- 3rd UART with 32-byte FIFO is supported in both TX/RX transmission *[W83977AF/AG only]*

--- 8-byte status FIFO is supported to store received frame status (such as overrun CRC error, etc.)

- Support auto-config SIR and FIR *[W83977AF/AG only]*

Parallel Port

- Compatible with IBM parallel port
- Support PS/2 compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- Extension FDD mode supports disk drive B; and Extension 2FDD mode supports disk drives A and B through parallel port
- Enhanced printer port back-drive current protection

Advanced Power Management (APM) Controlling

- Power turned on when RTC reaches a preset date and time
- Power turned on when a ring pulse or pulse train is detected on the PHRI, or when a high to low transition on PWAKIN1, or PWAKIN2 input signals
- Power turned on when PANSW input signal indicates a switch on event
- Power turned off when PANSW input signal indicates a switch off event
- Power turned off when a fail-safe event occurs (power-save mode detected but system is hung up)
- Power turned off when software issues a power off command

Keyboard Controller

- 8042 based with optional F/W from AMIKKEY™-2, Phoenix MultiKey/42™ or customer code
- with 2K bytes of programmable ROM, and 256 bytes of RAM
- Asynchronous Access to Two Data Registers and One status Register
- Software compatibility with the 8042 and PC87911 microcontrollers
- Support PS/2 mouse
- Support port 92
- Support both interrupt and polling modes
- **Fast Gate A20 and Hardware Keyboard Reset**
- 8 Bit Timer/ Counter; support binary and BCD arithmetic
- 6, 8, 12, or 16 Mhz operating frequency (16 Mhz available only if input clock rate = 14.318 Mhz)

Real Time Clock

- 27 bytes of clock, **On-Now**, and control/status register (14 bytes in Bank 0 and 13 bytes in Bank 2); 242 bytes of general purpose RAM
- BCD or Binary representation of time, calendar, and alarm registers
- Counts seconds, minutes, hours, days of week, days of month, month, year, and century
- 12-hour/ 24-hour clock with AM/PM in 12-hour mode
- Daylight saving time option; automatic leap-year adjustment
- Dedicated alarm (Alarm B) for **On-Now** function
- Programmable delay-time between panel switch off and power supply control
- Software control power-off; various and maskable events to activate system Power-On
- System Management Interrupt ($\overline{\text{SMI}}$) for panel switch power-off event

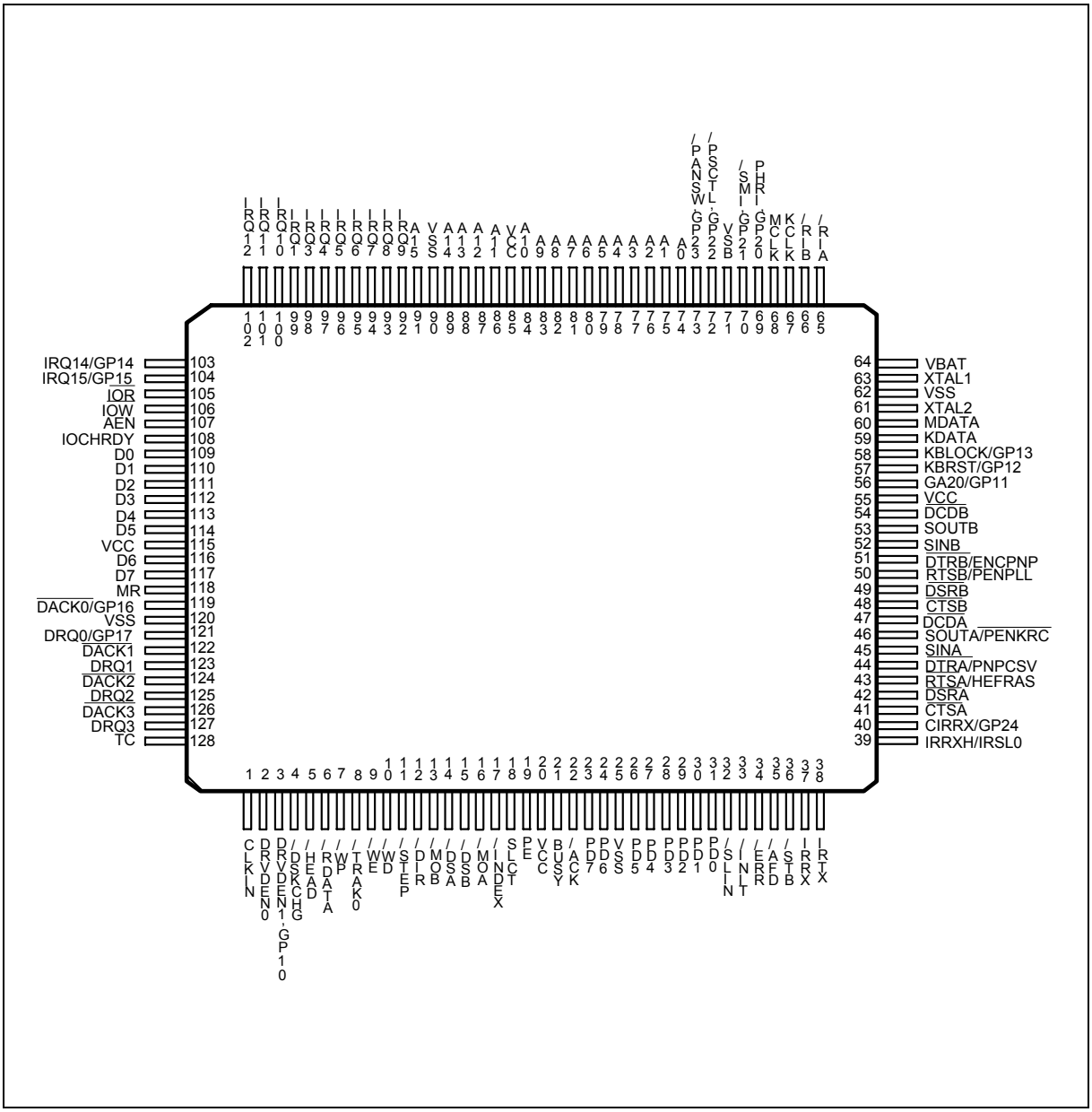
General Purpose I/O Ports

- 14 programmable general purpose I/O ports; 6 dedicate, 8 optional
- General purpose I/O ports can serve as simple I/O ports, interrupt steering inputs, watching dog timer output, power LED output, infrared I/O pins, general purpose address decoder, KBC control I/O pins.

Package

- 128-pin PQFP

3. PIN CONFIGURATION



4. PIN DESCRIPTION

Note: Please refer to Section 11.2 DC CHARACTERISTICS for details.

I/O6t - TTL level bi-directional pin with 6 mA source-sink capability

I/O8t - TTL level bi-directional pin with 8 mA source-sink capability

I/O8 - CMOS level bi-directional pin with 8 mA source-sink capability

I/O12t - TTL level bi-directional pin with 12 mA source-sink capability

I/O12 - CMOS level bi-directional pin with 12 mA source-sink capability

I/O16u - CMOS level bi-directional pin with 16 mA source-sink capability with internal pull-up resistor

I/OD16u - CMOS level bi-directional pin open drain output with 16 mA sink capability with internal pull-up resistor

I/O24t - TTL level bi-directional pin with 24 mA source-sink capability

OUT8t - TTL level output pin with 8 mA source-sink capability

OUT12t - TTL level output pin with 12 mA source-sink capability

OD12 - Open-drain output pin with 12 mA sink capability

OD24 - Open-drain output pin with 24 mA sink capability

INt - TTL level input pin

INc - CMOS level input pin

INcu - CMOS level input pin with internal pull-up resitor

INcs - CMOS level Schmitt-triggered input pin

INts - TTL level Schmitt-triggered input pin

INtsu - TTL level Schmitt-triggered input pin with internal pull-up resistor

4.1 Host Interface

SYMBOL	PIN	I/O	FUNCTION
A0–A10	74-84	IN_t	System address bus bits 0-10
A11-A14	86-89	IN_t	System address bus bits 11-14
A15	91	IN_t	System address bus bit 15
D0–D5	109-114	I/O_{12t}	System data bus bits 0-5
D6–D7	116-117	I/O_{12t}	System data bus bits 6-7
$\overline{IOR}$	105	IN_{ts}	CPU I/O read signal
$\overline{IOW}$	106	IN_{ts}	CPU I/O write signal
AEN	107	IN_t	System address bus enable
IOCHRDY	108	OD_{24}	In EPP Mode, this pin is the IO Channel Ready output to extend the host read/write cycle.
MR	118	IN_{ts}	Master Reset. Active high. MR is low during normal operations.

Host Interface, continued.

SYMBOL	PIN	I/O	FUNCTION
$\overline{\text{DACK0}}$ GP16 (WDTO) P15 $\overline{\text{RTSC}}$	119	IN_{ts} I/O_{12t} I/O_{12t} OUT_{12t}	CR2C bit5, 4= 00 (default): DMA Channel 0 Acknowledge signal. CR2C bit5, 4= 01: General purpose I/O port 1 bit 6. It can be configured as a watchdog timer output. CR2C bit5, 4= 10: Keyboard P15 I/O port. CR2C bit5, 4= 11: $\overline{\text{RTS}}$ output of UART C. *[W83977AF only]*
DRQ0 GP17 (PLEDO) P14 $\overline{\text{DTRC}}$	121	OUT_{12t} I/O_{12t} I/O_{12t} OUT_{12t}	CR2C bit7, 6= 00 (default): DMA Channel 0 request signal. CR2C bit7, 6= 01: General purpose I/O port 1, bit 7. It can be configured as power LED output. CR2C bit7, 6= 10: Keyboard P14 I/O port. CR2C bit7, 6= 11: $\overline{\text{DTR}}$ output of UART C. *[W83977AF only]*
$\overline{\text{DACK1}}$	122	IN_{ts}	DMA Channel 1 Acknowledge signal
DRQ1	123	OUT_{12t}	DMA Channel 1 request signal
$\overline{\text{DACK2}}$	124	IN_{ts}	DMA Channel 2 Acknowledge signal
DRQ2	125	OUT_{12t}	DMA Channel 2 request signal
$\overline{\text{DACK3}}$	126	IN_{ts}	DMA Channel 3 Acknowledge signal
DRQ3	127	OUT_{12t}	DMA Channel 3 request signal
TC	128	IN_{ts}	Terminal Count. When active, this pin indicates termination of a DMA transfer.
IRQ1	99	OUT_{12t}	Interrupt request 1
IRQ3	98	OUT_{12t}	Interrupt request 3
IRQ4	97	OUT_{12t}	Interrupt request 4
IRQ5	96	OUT_{12t}	Interrupt request 5
IRQ6	95	OUT_{12t}	Interrupt request 6
IRQ7	94	OUT_{12t}	Interrupt request 7
IRQ8/ nIRQ8	93	OUT_{12t}	Interrupt request 8; default is nIRQ8 for RTC
IRQ9	92	OUT_{12t}	Interrupt request 9
IRQ10	100	OUT_{12t}	Interrupt request 10
IRQ11	101	OUT_{12t}	Interrupt request 11
IRQ12	102	OUT_{12t}	Interrupt request 12

Host Interface, continued.

SYMBOL	PIN	I/O	FUNCTION
IRQ14 GP14 ($\overline{\text{GPACS}}$) PLED IRSL1	103	OUT_{12t} I/O_{12t} OUT_{12t} OUT_{12t}	CR2C bit1, 0= 00 (default): Interrupt request 14 CR2C bit1, 0= 01: General purpose I/O port 1, bit 4. It can be configured as a general purpose address decode output. CR2C bit1, 0= 10: Power LED output. CR2C bit1, 0= 11: IR module select signal 1. *[W83977AF only]*
IRQ15 GP15 ($\overline{\text{GPAWE}}$) WDT IRSL2	104	OUT_{12t} I/O_{12t} OUT_{12t} OUT_{12t}	CR2C bit3, 2= 00 (default): Interrupt request 15 CR2C bit3, 2= 01: General purpose I/O port 1, bit 5. It can be configured as a general purpose address write enable output. CR2C bit3, 2= 10: Watch-Dog timer output. CR2C bit3, 2= 11: IR module select signal 2. *[W83977AF only]*
CLKIN	1	IN_t	14.318/ 24 Mhz clock input, selectable through bit 5 of CR24.

4.2 Advanced Power Management

SYMBOL	PIN	I/O	FUNCTION
PHRI GP20 (KBRST)	69	IN_t I/O_{12t}	CR2B bit2, 1=00 (default): Advanced Power Management (APM) phone ring indicator. Detection of an active PHRI pulse or pulse train activates the $\overline{\text{PSCTL}}$ signal. CR2B bit2, 1=01: General purpose I/O port 2, bit 0. It can be configured as keyboard reset (Keyboard P20).
POFIRQ GP21 (P13) P16 $\overline{\text{RIC}}$	70	OUT_{12t} I/O_{12t} I/O_{12t} IN_t	CR2B bit4, 3=00 (default): Advanced Power Management (APM) power off interrupt request. CR2B bit4, 3=01: General purpose I/O port 2, bit 1. It can be configured as Keyboard P13 I/O port. CR2B bit4, 3=10: Keyboard P16 I/O port. CR2B bit4, 3=11: $\overline{\text{RI}}$ input of UART C. *[W83977AF only]*
VSB	71	-	Advanced Power Management (APM) standby current source
$\overline{\text{PSCTL}}$ GP22 (P14)	72	OUT_{12t} I/O_{12t}	CR2B bit5=0 (default): On/Off control for Advanced Power Management (APM). This signal tells the main power supply whether power should be turned on. CR2B bit5=1: General purpose I/O port 2, bit 2. It can be configured as Keyboard P14 I/O port.
$\overline{\text{PANSW}}$	73	IN_t	CR2B bit7, 6=00 (default): On/Off switch for Advanced Power Management (APM). This signal indicates a request to switch the power on or off. When the VDD of the chip is disrupted, a high to low transition on this pin indicates a switch on request. When VDD returns, a high to low transition on this pin indicates a switch off request.

Advanced Power Management, continued.

SYMBOL	PIN	I/O	FUNCTION
GP23 (P15)		I/O_{12t}	CR2B bit7, 6=01: General purpose I/O port 2, bit 3. It can be configured as Keyboard P15 I/O port.
$\overline{DCDC}$		IN_t	CR2B bit7, 6=11: $\overline{DCD}$ input of UART C. *[W83977AF only]*

4.3 Serial Port Interface

SYMBOL	PIN	I/O	FUNCTION
$\overline{CTSA}$ $\overline{CTSB}$	41 48	IN_t	Clear To Send is the modem control input. The function of these pins can be tested by reading Bit 4 of the handshake status register.
$\overline{DSRA}$ $\overline{DSRB}$	42 49	IN_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
$\overline{RTSA}$ HEFRAS	43	I/O_{8t}	UART A Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. During power-on reset, this pin is pulled down internally and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). A 4.7 kΩ is recommended if intends to pull up. (select 370H as configuration I/O port address)
$\overline{RTSB}$ nPENPLL	50	I/O_{8t}	UART B Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. During power-on reset, this pin is pulled down internally and is defined as nPENPLL, which provides the power-on value for CR24 bit 5 (ENPLL) and bit 6. A 4.7 kΩ is recommended if intends to pull up. (PLL is disabled)
$\overline{DTRA}$ $\overline{PNPCSV}$	44	I/O_{8t}	UART A Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate. During power-on reset, this pin is pulled down internally and is defined as $\overline{PNPCSV}$, which provides the power-on value for CR24 bit 0 ($\overline{PNPCSV}$). A 4.7 kΩ is recommended if intends to pull up. (clear the default value of FDC, UARTs, and PTR)
$\overline{DTRB}$ ENCPNP	51	I/O_{8t}	UART B Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate. During power-on reset, this pin is pulled down internally and is defined as ENCPNP, which provides the power-on value for CR24 bit 1 (ENPNP). A 4.7 kΩ is recommended if intends to pull up. (enable comply PnP mode)
SINA SINB	45, 52	IN_t	Serial Input. Used to receive serial data through the communication link.

Serial Port Interface, continued.

SYMBOL	PIN	I/O	FUNCTION
SOUTA PENKRC	46	I/O_{8t}	UART A Serial Output. Used to transmit serial data out to the communication link. During power-on reset, this pin is pulled down internally and is defined as PENKRC, which provides the power-on value for CR24 bit 2 (ENKBRTC). A 4.7 kΩ is recommended if intends to pull up. (enable KBC and RTC)
SOUTB	53	I/O_{8t}	UART B Serial Output. Used to transmit serial data out to the communication link.
$\overline{DCDA}$ $\overline{DCDB}$	47 54	IN_t	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
$\overline{RIA}$ $\overline{RIB}$	65 66	IN_t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.

4.4 Infrared Interface

SYMBOL	PIN	I/O	FUNCTION
IRRX (SINC)	37	IN_{cs}	Infrared Receiver input. It functions as SIN input if UART C is configured as a simple serial port. *[W83977AF only]*
IRTX (SOUTC)	38	OUT_{12t}	Infrared Transmitter Output. It functions as SOUT output if UART C is configured as a simple serial port. *[W83977AF only]*
IRRXH IRSL0 GP25 (GA20) $\overline{CTSC}$	39	I/O_{12t} OUT_{12t} I/O_{12t} IN_t	CR2A bit3, 2=00 (default): High speed IR receiving terminal. CR2A bit3, 2=01: IR module select 0. CR2A bit3, 2=10: General purpose I/O port 2, bit 5. It can be configured as GATE A20 (Keyboard P21). CR2A bit3, 2=11: $\overline{CTS}$ input of UART C. *[W83977AF only]*
CIRRX GP24 (P16) P13	40	IN_t I/O_{12t} I/O_{12t}	CR2A bit5, 4=00 (default): Consumer IR receiving terminal. CR2A bit5, 4=01: General purpose I/O port 2, bit 4. It can be configured as Keyboard P16 I/O port. CR2A bit5, 4=10: Keyboard P13 I/O

4.5 Multi-Mode Parallel Port

The following pins have alternate functions, which are controlled by CR28 and L3-CRF0.

SYMBOL	PIN	I/O	FUNCTION
SLCT	18	IN_t	PRINTER MODE: SLCT An active high input on this pin indicates that the printer is selected. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{WE2}$ This pin is for Extension FDD B; its function is the same as the $\overline{WE}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{WE2}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{WE}$ pin of FDC.
PE	19	IN_t	PRINTER MODE: PE An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{WD2}$ This pin is for Extension FDD B; its function is the same as the $\overline{WD}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{WD2}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{WD}$ pin of FDC.
BUSY	21	IN_t	PRINTER MODE: BUSY An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{MOB2}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{MOB}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{MOB2}$ This pin is for Extension FDD A and B; the function of this pin is the same as the $\overline{MOB}$ pin of FDC.

Multi-Mode Parallel Port, continued.

SYMBOL	PIN	I/O	FUNCTION
$\overline{ACK}$	22	IN_t	PRINTER MODE: $\overline{ACK}$ An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{DSB2}$ This pin is for the Extension FDD B; its functions is the same as the $\overline{DSB}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{DSB2}$ This pin is for Extension FDD A and B; it functions is the same as the $\overline{DSB}$ pin of FDC.
$\overline{ERR}$	34	IN_t	PRINTER MODE: $\overline{ERR}$ An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{HEAD2}$ This pin is for Extension FDD B; its function is the same as the $\overline{HEAD}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{HEAD2}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{HEAD}$ pin of FDC.
$\overline{SLIN}$	32	OD_{12}	PRINTER MODE: $\overline{SLIN}$ Output line for detection of printer selection. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{STEP2}$ This pin is for Extension FDD B; its function is the same as the $\overline{STEP}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{STEP2}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{STEP}$ pin of FDC.
$\overline{INIT}$	33	OD_{12}	PRINTER MODE: $\overline{INIT}$ Output line for the printer initialization. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: $\overline{DIR2}$ This pin is for Extension FDD B; its function is the same as the $\overline{DIR}$ pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: $\overline{DIR2}$ This pin is for Extension FDD A and B; its function is the same as the $\overline{DIR}$ pin of FDC.

Multi-Mode Parallel Port, continued.

SYMBOL	PIN	I/O	FUNCTION
$\overline{AFD}$	35	OD_{12}	PRINTER MODE: $\overline{AFD}$ An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: DRVDEN0 This pin is for Extension FDD B; its function is the same as the DRVDEN0 pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: DRVDEN0 This pin is for Extension FDD A and B; its function is the same as the DRVDEN0 pin of FDC.
$\overline{STB}$	36	OD_{12}	PRINTER MODE: $\overline{STB}$ An active low output is used to latch the parallel data into the printer. This pin is pulled high internally. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		-	EXTENSION 2FDD MODE: This pin is a tri-state output.
PD0	31	I/O_{24t}	PRINTER MODE: PD0 Parallel port data bus bit 0. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: $\overline{INDEX2}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{INDEX}$ pin of FDC. It is pulled high internally.
		IN_t	EXTENSION 2FDD MODE: $\overline{INDEX2}$ This pin is for Extension FDD A and B; the function of this pin is the same as the $\overline{INDEX}$ pin of FDC. It is pulled high internally.
PD1	30	I/O_{24t}	PRINTER MODE: PD1 Parallel port data bus bit 1. Refer to description of the parallel port for definition of this pin in ECP and EPP mode. .
		IN_t	EXTENSION FDD MODE: $\overline{TRAK02}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{TRAK0}$ pin of FDC. It is pulled high internally..
		IN_t	EXTENSION. 2FDD MODE: $\overline{TRAK02}$ This pin is for Extension FDD A and B; the function of this pin is the same as the $\overline{TRAK0}$ pin of FDC. It is pulled high internally.
PD2	29	I/O_{24t}	PRINTER MODE: PD2 Parallel port data bus bit 2. Refer to description of the parallel port for definition of this pin in ECP and EPP mode..
		IN_t	EXTENSION FDD MODE: $\overline{WP2}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{WP}$ pin of FDC. It is pulled high internally.
		IN_t	EXTENSION. 2FDD MODE: $\overline{WP2}$ This pin is for Extension FDD A and B; the function of this pin is the same as the $\overline{WP}$ pin of FDC. It is pulled high internally.

Multi-Mode Parallel Port, continued.

SYMBOL	PIN	I/O	FUNCTION
PD3	28	I/O_{24t}	PRINTER MODE: PD3 Parallel port data bus bit 3. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: $\overline{RDATA2}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{RDATA}$ pin of FDC. It is pulled high internally.
		IN_t	EXTENSION 2FDD MODE: $\overline{RDATA2}$ This pin is for Extension FDD A and B; this function of this pin is the same as the $\overline{RDATA}$ pin of FDC. It is pulled high internally.
PD4	27	I/O_{24t}	PRINTER MODE: PD4 Parallel port data bus bit 4. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: $\overline{DSKCHG2}$ This pin is for Extension FDD B; the function of this pin is the same as the $\overline{DSKCHG}$ pin of FDC. It is pulled high internally.
		IN_t	EXTENSION 2FDD MODE: $\overline{DSKCHG2}$ This pin is for Extension FDD A and B; this function of this pin is the same as the $\overline{DSKCHG}$ pin of FDC. It is pulled high internally.
PD5	26	I/O_{24t}	PRINTER MODE: PD5 Parallel port data bus bit 5. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		-	EXTENSION 2FDD MODE: This pin is a tri-state output.
PD6	24	I/O_{24t}	PRINTER MODE: PD6 Parallel port data bus bit 6. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		OD_{24}	EXTENSION. 2FDD MODE: $\overline{MOA2}$ This pin is for Extension FDD A; its function is the same as the $\overline{MOA}$ pin of FDC.
PD7	23	I/O_{24t}	PRINTER MODE: PD7 Parallel port data bus bit 7. Refer to description of the parallel port for definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		OD_{24}	EXTENSION 2FDD MODE: $\overline{DSA2}$ This pin is for Extension FDD A; its function is the same as the $\overline{DSA}$ pin of FDC.

4.6 FDC Interface

SYMBOL	PIN	I/O	FUNCTION
DRVDEN0	2	OD_{24}	Drive Density Select bit 0.
DRVDEN1 GP10 (IRQIN1) P12 $\overline{DSRC}$	3	OD_{24}	Drive Density Select bit 1. Alternate Function 1: General purpose I/O port 1, bit 0. It can be configured as an interrupt channel. Alternate Function 2: Keyboard P12 I/O port. Alternate Function 3: $\overline{DSR}$ input of UART C *[W83977AF only]*
$\overline{HEAD}$	5	OD_{24}	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0; Logic 0 = side 1
$\overline{WE}$	9	OD_{24}	Write enable. An open drain output.
$\overline{WD}$	10	OD_{24}	Write data. This logic low open drain writes precompensation serial data to the selected FDD. An open drain output.
$\overline{STEP}$	11	OD_{24}	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
$\overline{DIR}$	12	OD_{24}	Direction of the head step motor. An open drain output. Logic 1 = outward motion; Logic 0 = inward motion
$\overline{MOB}$	13	OD_{24}	Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output.
$\overline{DSA}$	14	OD_{24}	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
$\overline{DSB}$	15	OD_{24}	Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output.
$\overline{MOA}$	16	OD_{24}	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
$\overline{DSKCHG}$	4	IN_{cs}	Diskette change. This signal is active low at power on and when the diskette is removed. This input pin is pulled up internally by a 1 K . resistor, which can can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
$\overline{RDATA}$	6	IN_{cs}	The read data input signal from the FDD. This input pin is pulled up internally by a 1 K resistor, which can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
$\overline{WP}$	7	IN_{cs}	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin is pulled up internally by a 1 K resistor, which can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
$\overline{TRAK0}$	8	IN_{cs}	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track. This input pin is pulled up internally by a 1 K resistor, which can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
$\overline{INDEX}$	17	IN_{cs}	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin is pulled up internally by a 1 K resistor, which can be disabled by bit 7 of L0-CRF0 (FIPURDWN).

4.7 KBC Interface

SYMBOL	PIN	I/O	FUNCTION
KDATA	59	I/OD_{16u}	Keyboard Data
MDATA	60	I/OD_{16u}	PS2 Mouse Data
KCLK	67	I/OD_{16u}	Keyboard Clock
MCLK	68	I/OD_{16u}	PS2 Mouse Clock
GA20 GP11 (IRQIN2)	56	OUT_{12t} I/O_{12t}	CR2A bit6= 0 (default): Keyboard GATE A20 (P21) Output. CR2A bit6= 1: General purpose I/O port 1, bit 1. It can be configured as an interrupt channel.
KBRST GP12 (WDTO, IRRX)	57	OUT_{12t} I/O_{12t}	CR2A bit7= 0 (default): Keyboard Reset (P20) Output. CR2A bit7= 1: General purpose I/O port 1, bit 2. It can be configured as watchdog timer output or IRRX (SINC if UART C is used as a simple serial port *[W83977AF only]*) input.
KBLOCK GP13 (PLEDO, IRTX)	58	IN_{16tu} I/O_{16tu}	CR2B bit0= 0 (default): Keyboard KINH (P17) Input. CR2B bit0= 1: General purpose I/O port 1, bit 3. It can be configured as watchdog timer output or IRTX (SOUTC if UART C is used as a simple serial port *[W83977AF only]*) output.

4.8 RTC Interface

SYMBOL	PIN	I/O	FUNCTION
VBAT	64		RTC battery voltage input
XTAL1	63	IN_C	RTC 32.768Khz Clock Input
XTAL2	61	O_{8t}	RTC 32.768Khz Clock Output

4.9 POWER PINS

VCC	20,55, 85,115	+5V power supply for the digital circuitry
GND	25,62, 90,120	Ground

5. FDC FUNCTIONAL DESCRIPTION

5.1 W83977F/G and W83977AF/AG FDC

The floppy disk controller of the W83977F/G, W83977AF/AG integrates all of the logic required for floppy disk control. The FDC implements a PC/AT or PS/2 solution. All programmable options default to compatible values. The FIFO provides better system performance in multi-master systems. The digital data separator supports up to 2 M bits/sec data rate.

The FDC includes the following blocks: AT interface, Precompensation, Data Rate Selection, Digital Data Separator, FIFO, and FDC Core.

5.1.1 AT interface

The interface consists of the standard asynchronous signals: $\overline{RD}$, $\overline{WR}$, A0-A3, IRQ, DMA control, and a data bus. The address lines select between the configuration registers, the FIFO and control/status registers. This interface can be switched between PC/AT, Model 30, or PS/2 normal modes. The PS/2 register sets are a superset of the registers found in a PC/AT.

5.1.2 FIFO (Data)

The FIFO is 16 bytes in size and has programmable threshold values. All command parameter information and disk data transfers go through the FIFO. Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The FIFO defaults to disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the CONFIGURE command. The advantage of the FIFO is that it allows the system a larger DMA latency without causing disk errors. The following tables give several examples of the delays with a FIFO. The data are based upon the following formula:

THRESHOLD # × (1/DATA/RATE) *8 - 1.5 μS = DELAY

FIFO THRESHOLD	MAXIMUM DELAY TO SERVICING AT 500K BPS
	Data Rate
1 Byte	1 × 16 μS - 1.5 μS = 14.5 μS
2 Byte	2 × 16 μS - 1.5 μS = 30.5 μS
8 Byte	8 × 16 μS - 1.5 μS = 6.5 μS
15 Byte	15 × 16 μS - 1.5 μS = 238.5 μS
FIFO THRESHOLD	**MAXIMUM DELAY TO SERVICING AT 1M BPS**
	Data Rate
1 Byte	1 × 8 μS - 1.5 μS = 6.5 μS
2 Byte	2 × 8 μS - 1.5 μS = 14.5 μS
8 Byte	8 × 8 μS - 1.5 μS = 62.5 μS
15 Byte	15 × 8 μS - 1.5 μS = 118.5 μS